SOLENNA$_{(3)}$: The ultimate simplification of bifacial silicon technology, at a competitive cost/Wp

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ABSTRACT

The c-Si PV industry has been historically dominated by the conventional full Al-BSF cell architecture, applied to p-type silicon, because it has so far always yielded the lowest cost at the module level (€/Wp). At the system level (€/kWh), on the other hand, bifacial PV and related reference bifacial n-PERT technology seems to be a better option for cost reduction, but additional cell processing steps (and related costs) are inhibiting bifacial PV growth. This paper first introduces INES' reference 20%-PERT technology 'SOLENN', which is based on a conventional gaseous diffusion process. Passivating/anti-reflective/doping SiO_xN_y:B and SiN_x:P layers have been developed at INES, and the properties of these multifunctional layers are described in detail. Two process simplifications are introduced which provide devices that are both 20%-efficient and co-diffused, and which use to advantage, in the first instance, just the doping properties of the layers. By then capitalizing on the passivating and optical properties of the multifunctional layers, INES' so-called 'SOLENNA$_{(3)}$' technology is presented. This ultimately simplified technology provides large-area (243cm²), LID-free, 19.8%-efficient n-PERT cells in only seven processing steps. To the authors' knowledge, this is so far the simplest n-PERT process to be introduced with such a level of performance. Finally, the cost calculation based on a 100MW line capacity and on a comparison of SOLENNA$_{(3)}$ with reference technologies (such as Al-BSF, PERC and BBr_3 PERT) was completed, without considering the potential gain from the bifacial properties. Because of its simplicity, SOLENNA$_{(3)}$ technology is shown to be clearly competitive with the classical Al-BSF technology in terms of cost per watt at the module level.

Introduction

Since the c-Si PV industry scaled up to mass production, it has been dominated by the conventional full Al back-surface field (Al-BSF) cell architecture, implemented with p-type silicon. Al-BSF device performance has indeed been steadily improved (with up to 19.5% efficiency achieved for p-type solar cells [1]) and remains today the most suitable option in terms of €/Wp. In the current PV module manufacturing industry, cost reduction and process upgrade are privileged, small modifications of existing production lines being preferred to new investment. As a result, passivated emitter rear contact (PERC) architecture is gaining ground, providing p-type devices with 20–21% efficiency [2] using only a few additional steps (chemical surface preparation, deposition of passivating dielectric layer, local opening of this layer).

On the other hand, the bifacial photovoltaics (bifi-PV) market is soaring, with the passivated emitter, rear totally diffused (PERT) architecture providing 20%-efficient n-type devices that demonstrate no light-induced degradation (LID), but are fabricated using more-complex cell process flows. The PV community is becoming more and more convinced that the use of bifaciality for future generations of PV systems will allow a significant reduction in the levelized cost of electricity (LCOE). Some direct issues (bankability) are currently being addressed through the installation of large (>1MWp) PV bifacial fields [3] and through the formation of standardization groups.

There is another issue concerning the additional cost incurred in the production of bifacial modules, primarily related to the additional processing steps at the cell level. Indeed, the fabrication of the so-called PERT cell, suitable for bifaciality, meets different specifications, such as single-sided p^+ and n^+ diffusion, B emitter specific passivation and double-sided SiN coating. Over the last few years, academics and manufacturers have made significant R&D efforts in finding ways to simplify the process flow [4]. The use of a hybrid approach combining P-implantation and BBr_3 diffusion is one example of such process simplification [5]. The full implantation process is also very attractive, since the formation of the doped layers can be performed at the same time as the annealing step [6,7]. Finally, the co-diffusion approach involves single-sided deposited doped layers [8,9].

Most of these concepts have in recent years led to solar cells with conversion efficiencies of over 20.0%. Nevertheless, the growth in the production of bifacial cells remains limited, mostly because the economic interest only occurs at the system level (LCOE) when the bifacial gain is considered. The authors believe that a faster growth of bifacial PV requires an even more simplified bifacial cell manufacturing process in order to reduce the initial CAPEX investment, and thus the cost per Wp.

> "A faster growth of bifacial PV requires an even more simplified bifacial cell manufacturing process."

Doping properties of SiO_xN_y:B and SiN_x:P layers

Among the alternative doping techniques considered for simplifying the fabrication of the $p^+/n/n^+$ structure, dielectric doped layers are of primary interest, since they open the door to co-diffusion (the formation of the emitter and the BSF in a single step [10–12]). In recent years, the annealing

of boron silicate glass (BSG) during $POCl_3$ diffusion has led to co-diffused n-PERT devices with 20% efficiency [13]. In this approach, the BSG layer (which is a SiO_x:B-based material) shows both doping properties and a barrier property with regard to phosphorus diffusion. The quality of doping has already been demonstrated at INES, as well as by other teams, with satisfactory doping uniformities (<5%) for a relevant sheet resistance (R_{sheet}) window of 50–100Ω/sq. Since the doping activation is facilitated in the case of boron dopant, it is possible to measure (using a WCT 120 Sinton Lifetime tester) satisfactory B-emitter saturation current densities (J_{0e} < 90fA/cm² for 70Ω/sq.) on 239cm² Cz textured samples ($p^+/n/p^+$ structure passivated by thermal SiO_2/SiN stack). In the literature, even lower saturation current density values can be found on polished samples and/or with a higher emitter R_{sheet} domain, and/or using an AlO_x/SiN passivating stack [14], offering further evidence of the quality of BSG as a doping source.

At INES, the BSG layer is more precisely a SiO_xN_y:B material, deposited by low-frequency plasma-enhanced chemical vapour deposition (PECVD), using a mixture of SiH_4 and N_2O, and H_2-diluted B_2H_6 as a boron precursor. For this work, various thicknesses of SiO_xN_y:B were coated on 239cm² Cz(n) wafers (1–4Ω·cm) and then annealed at 940°C (< 1h) under N_2. The resulting B-emitter R_{sheet} values are plotted in Fig. 1 as a function of SiO_xN_y:B thickness; it is demonstrated here that the thickness of the layer is not the primary determinant of the final sheet resistance of the emitter. Once the minimum thickness (here 19nm) satisfying the resistance (<100Ω/sq.) and the uniformity (<5%) is reached, any further increase in the thickness of the layer only improves the doping uniformity (< 2%), with no impact on the average sheet resistance value. This quasi-independency of R_{sheet} with respect to doping layer thickness is in agreement with studies [15,16] showing stronger dependency on the SiH_4/B2H$_6$ ratio. In this case, the gas ratio was chosen below 4%, in order to promote high doping from significantly thinner SiO_xN_y:B layers (<20nm) than what is usually reported in the literature.

Dielectric doped layers as an alternative n^+ doping technique to conventional $POCl_3$ diffusion are also considered. Here, the aim is to use such a doping layer for the n^+ BSF of the n-PERT solar cells. PECVD-deposited PSG (phosphorus silicate glass) layers have been considered as an option for many years [17,18]. Despite the promising results obtained with PSG on p-type devices [19], no clear benefit of such P-doping sources has been demonstrated up to now. Aside from this most commonly studied P-doped SiO_x material, it was preferred to focus on the development of hydrogenated SiN_x:P layers, with the aim of combining doping and passivating properties in one layer.

The use of SiN:P as a phosphorus doping source has been investigated in the past for laser-doped selective emitter p-type solar cells fabrication [20], but has yielded high emitter contact resistance. In the present work, the SiN:P was deposited by low-frequency PECVD, using a mixture of SiH_4, NH_3 and H_2-diluted PH_3 as a phosphorus precursor. Various thicknesses of SiN_x:P were coated on 239cm² Cz(p) wafers (2Ω·cm), which were then annealed at 940°C (<1h) under N_2. The resulting n^+ region sheet resistance is plotted in Fig. 2 as a function of SiN_x:P thickness; the R_{sheet} of the n^+ BSF increases steadily as the SiN_x:P thickness decreases. The doping behaviour is consistent with a finite source: the thinner the layer, the higher the R_{sheet}. It should be noted that there is no dramatic degradation of doping uniformity (<8%), even for the thinner layer (12nm).

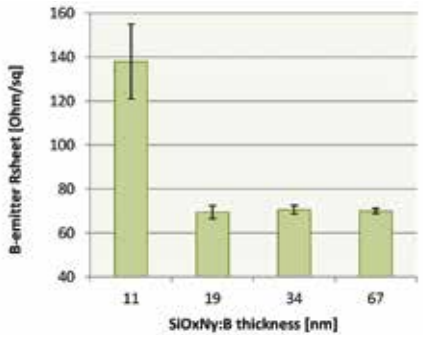

Figure 1. Variation in R_{sheet} of the p^+ emitter for different SiO_xN_y:B layer thicknesses after the anneal (940°C; <1h).

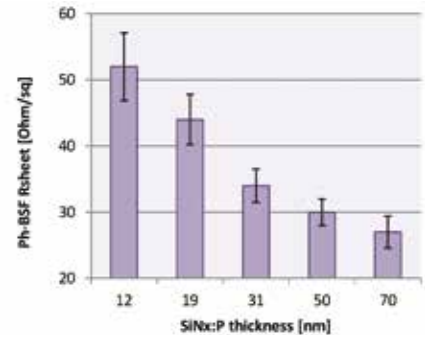

Figure 2. Variation in R_{sheet} of the n^+ BSF for different SiN_x:P layer thicknesses after the anneal (940°C; <1h).

Moderately simplified n-PERT solar devices

A first integration of the boron and phosphorus doping layers was performed on 239cm² n-PERT solar cells. As a reference, INES' baseline PERT process was used, which is based on two separate gaseous diffusions. This process is then referred to as the *SOLENN process* (**SOL**ar **EN**hanced **N**-type).

SOLENN process

The processing sequence for SOLENN solar cells includes alkaline texturing of Cz(n) wafers surfaces, BCl_3 boron diffusion (940°C) and $POCl_3$ phosphorus diffusion (840°C). PECVD-deposited SiO_x barriers are coated on the opposite side of the wafer, prior to each diffusion, and removed (by HF-dip + RCA clean) after each diffusion. Once the p+/n/n+ structure is obtained, both sides are passivated by thermal oxidation, leading to SiO_2 growth of less than 10nm in thickness. PECVD deposition of anti-reflective hydrogenated SiN is then carried out on both sides. A Ag/Al grid is screen printed on the front, while a Ag grid is

printed on the rear, for contacting the p^+ emitter and the n^+ BSF respectively; the actual contacting is done during the subsequent co-firing step in an IR belt furnace.

1st simplified approach

The first way to make the n-PERT process flow shorter is to use the SiO_xN_y:B layer as a boron doping source, and benefit from the $POCl_3$ diffusion step to promote formation of the B emitter: such a co-diffusion combining solid and gaseous doping sources has been widely studied in the literature [21,22], and will therefore not be expanded on too much here. It is just worth recalling the requirement of the B-doped layer to act as a barrier to $POCl_3$ diffusion. In order to do so, the use of a thick (>100nm) BSG, including optional surface-capping layers, is often reported; for instance, Rothhardt et al. [9] use a ~180nm BSG/SiO_x stack deposited by APCVD for their 19.9% CoBiN n-PERT cell. Similarly, the aforementioned SiO_xN_y:B would not alone ensure good barrier properties, and so SiN_x was used as a capping layer.

The processing sequence for 'SOLENNA$_{(1)}$' devices (i.e. the 1st simplified SOLENN approach) is the following. After alkaline texturing, the wafer front side is coated by the low-frequency PECVD stack (a 30nm-thick SiO_xN_y:B capped by 50nm of SiN_x) prior to the co-diffusion cycle (involving a first plateau at 940°C under N_2, followed by the $POCl_3$ injection at a lower temperature). The $POCl_3$-induced glass (rear) and B-doped stack (front) are then HF removed, and the wafers surfaces are RCA cleaned. The subsequent passivation and metallization sequence is identical to INES' reference process (SOLENN).

2nd simplified approach

The second way of simplifying n-PERT technology is to co-anneal solid sources only. Solid sources have been studied for decades [23,24]; Das et al. [25], for instance, demonstrated the high potential of B-doped spin-on glass by fabricating 20%-efficient 4cm^2 devices incorporating it. Nevertheless, the significant bifacial cell results obtained so far have always combined one solid doping source with a more conventional technique (ion implantation or gaseous diffusion). More precisely, what are referred to here as 'SOLENNA$_{(2)}$' devices (i.e. 2nd simplified SOLENN approach devices) combine the SiO_xN_y:B and SiN_x:P layers for the p^+ emitter and n^+ BSF formation.

The processing sequence for SOLENNA$_{(2)}$ solar cells includes, as always, the alkaline texturing, followed by SiO_xN_y:B (front) and SiN_x:P (rear) deposition. Samples are then co-annealed in a quartz tube furnace (940°C; <1h) under a N_2 atmosphere. Note that the use of a solid P-doped layer instead of $POCl_3$ allows thin (<40nm) uncapped SiO_xN_y:B layers to be employed. Doped dielectrics are then HF removed, and the wafers surfaces are RCA cleaned. The subsequent steps are identical to the previously described processes (see SOLENN and SOLENNA$_{(1)}$).

Cell results

The different process flows described so far are depicted in Fig. 3. Batches of 239cm^2 Cz n-type wafers (2–3Ω·cm) were processed into n-PERT screen-printed solar cells, following these different approaches. The best *I–V* parameters measured on these batches (in a class A solar simulator, under standard testing conditions – STC) are listed in Table 1.

The poorer FF/PFF values exhibited by SOLENNA$_{(1)}$ solar cells are attributed to localized parasitic P diffusion through SiO_xN_y:B/SiN porosities; as a result, a lower shunt resistance value (R_p < 2kΩ·cm^2) is reached (50kΩ·cm^2 for the reference process). The SOLENNA$_{(2)}$ devices are logically excluded from such an R_p limitation, since they are made via a pure dielectric co-diffusion route.

Both the 1st and 2nd simplifications of the SOLENN process made it possible to obtain 20%-efficiency n-PERT bifacial solar cells, using a reduced number of processing steps compared with the reference process. Both SOLENNA$_{(1)}$ and SOLENNA$_{(2)}$ processes have also demonstrated good compatibility with industrial n-type mono-like silicon [13]. Nevertheless, further simplification of n-PERT technology would be possible if the doping PECVD layers could also provide proper passivating and optical properties.

From doping to multifunctional layers

Different ways of integrating multifunctional dielectric layers into solar devices are proposed in the

Figure 3. The n-PERT process flow simplifications: gaseous diffusion route (SOLENN), co-diffusion SiO_xN_y:B/$POCl_3$ route (SOLENNA$_{(1)}$) and full dielectric co-diffusion route (SOLENNA$_{(2)}$).

	Size [cm^2]	J_{sc} [mA/cm^2]	V_{oc} [mV]	*FF* [%]	η [%]	*PFF* [%]
SOLENN	239	39.3	647	79.9	20.3	83.5
SOLENNA$_{(1)}$	239	39.7	648	77.8	20.0	82.3
SOLENNA$_{(2)}$	239	39.0	648	79.2	20.0	83.5

Table 1. Best *I–V* results for n-PERT screen-printed solar cells (measured under STC: 25°C; AM1.5G; 1,000W/m^2).

	SiO_xN_y:B/SiN passivated $p^+/n/p^+$ structure			SiN_x:P/SiN passivated $n^+/n/n^+$ structure		
Successive tuning	*Initial*	Plasma	Anneal	*Initial*	Plasma	Anneal
J_0 (fA/cm²)	*1443*	120	85	*337*	247	180
1sun-iV_{oc} (mV)	*595*	649	667	*646*	654	658

Table 2. J_0 and 1sun-iV_{oc} values, measured on textured Cz symmetrical structures after successive tuning of the plasma parameters and the co-anneal process.

few papers that can be found in the literature. The PassDop approach uses SiN_x:P for playing alternatively the role of P-reservoir for laser doping (beneath the contacted regions) and the role of passivating layer between the heavily-doped regions. Reported PassDop n-PERL cell performance is outstanding [26,27], but SiN_x:P doping and passivating properties are never exploited concurrently in one specific region of the devices.

The quality of passivation offered by existing doped layers has also been reported in the literature. For instance, the passivation of n^+ regions by phosphorus- or boron-doped nitride layers (SiN_x:P/B) was studied by Gall et al. [28]: in both cases, the introduction of a thermal SiO_2 interfacial layer was required in order to obtain satisfying J_{0e}/iV_{oc} values. More recently, the passivating potential of 100nm thick SiN_x-capped BSG layers was reported by Engelhardt et al. [14] with a 1sun-iV_{oc} of 675mV obtained on $p^+/n/p^+$ FZ samples, with a 60Ω/sq. emitter. Nevertheless, no integration of such a stack in an actual solar device has so far been reported.

Multi-purpose PECVD stacks have been developed, in which each layer ensures one function (anti-reflective, passivating or doping). For instance, 120nm thick PSG/SiN stacks have been reported to provide good n^+ doping and subsequent passivation (65Ω/sq.; 118fA/cm²) on shiny-etched FZ [29]. In addition to this, a 300nm-thick dielectric stack made of Al_2O_3, capped by an oxidized a-Si:B layer, was used by Seiffe et al. [30] on the back side of LFC solar cells, for p^+ doping (>250Ω/sq.), passivation and optics. Those authors subsequently measured a conversion efficiency of 18.3% on 50mm × 50mm Cz(p) substrates.

At CEA Tech-INES, as suggested previously, PECVD layers were developed with a high doping property, even for thin layers. For instance, as can be seen in Figs. 1 and 2, 20nm-thick SiO_xN_y:B and SiN_x:P layers are sufficient for achieving decent doping targets (in this case, p^+ emitter < 80Ω/sq.; n^+ BSF < 50Ω/sq.). From an optical point of view, the integration of the layers on both the front and the rear sides of solar devices is thus facilitated. In addition, the decision was taken to develop an hydrogenated nitride layer (SiN_x:P) to boost the passivating ability of the layer itself, instead of using a SiO_x:P layer combined with some additional passivating layer.

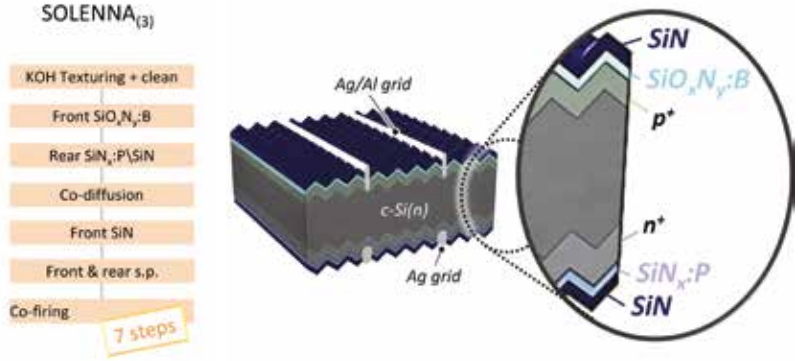

Figure 4. The ultra-simplified process flow and corresponding cell structure of SOLENNA(3).

The passivating properties of the SiO_xN_y:B and SiN_x:P layers were evaluated by means of QSSPC J_0 measurements, on $p^+/n/p^+$ and $n^+/n/n^+$ sample structures respectively. The thermal budget for the annealing of the layers and the related diffusion of the dopants is still 940°C, for a duration of less than one hour. These samples were created from Cz(n) 4Ω·cm wafers that had previously been alkaline textured, RCA cleaned and double-side coated with the layers under consideration.

The improvement of the initially poor passivating properties of the SiO_xN_y:B layer was investigated by capping it first with a typical anti-reflective (and H_2-reservoir) SiN layer. No significant enhancement of the passivating level was observed (J_{0p+} > 1,400fA/cm²). Similarly, the initial SiN_x:P layer was found to exhibit only moderate passivation (J_{0n+} > 370fA/cm²). Only a marginal improvement was observed when the SiN capping (J_{0n+}=337fA/cm²) was introduced, but such capping was used as a barrier to out-diffusion of phosphorus.

An enhancement of the passivation features of the doped layers was made possible by tuning of the plasma deposition conditions as well as of the subsequent co-annealing step. The resulting J_0/iV_{oc} values after firing (800°C) of the samples are given Table 2. The optical indexes (n;k) of the final layers have been measured by ellipsometry. SiO_xN_y:B was found to compare quite favourably with stoichiometric silicon oxide (refraction index n < 148 at λ = 633nm), and exhibits decent transparency in the higher wavelength domain (k < 0.0013). At present, further optical tuning is required for SiN_x:P in order to reduce the high optical indexes caused by a relatively Si-rich stoichiometry.

Ultra-simplified n-PERT solar devices

Process flow and cell results

A batch of 243cm² Cz n-type wafers (2Ω·cm) was processed using an ultra-simplified n-PERT approach, in which the doped layers are maintained. With the final front- and rear-surface passivation here being provided by SiO_xN_y:B/SiN and SiN_x:P, it was possible to avoid thermal oxidation as well as chemical removal of the doped layer and subsequent cleaning. Furthermore, the rear PECVD SiN deposition layer was integrated (because of out-diffusion concerns) as

	Size [cm²]	J_{sc} [mA/cm²]	V_{oc} [mV]	*FF* [%]	η [%]	*PFF* [%]
Average	243	38.6	644	79.1	19.7	82.9
Best cell		38.5	645	79.6	19.8	82.7

Table 3. *I–V* results for SOLENNA$_{(3)}$ n-PERT screen-printed solar cells (measured under STC: 25°C; AM1.5G; 1,000W/m²). A batch of 10 cells was used.

capping in the SiN_x:P recipe.

As a consequence, the processing sequence for 'SOLENNA$_{(3)}$' devices (i.e. the 3rd simplified SOLENN approach) is reduced to seven steps, as depicted in Fig. 4. After alkaline texturing and RCA cleaning of the wafer (1), the SiO_xN_y:B layer (2) and the SiN_x:P/SiN stack (3) are deposited on the front and rear sides. The samples are co-annealed (940°C; <1h) (4), leading to a 70Ω/sq. B emitter and a 35Ω/sq. P BSF. PECVD ARC SiN is deposited on the front (5). The front and rear silver-based grid contacts are screen printed (6) and then co-fired (7).

The average and best *I–V* parameters measured on this batch are listed in Table 3. The J_{sc} value is slightly lower for SOLENNA$_{(3)}$ solar cells (<38.8mA/cm²), because of the non-optimized transparency of the doped layers, and also because of the heavily doped n^+ BSF. A comparison of SOLENN and SOLENNA$_{(3)}$ spectral responses revealed an average loss of 3%$_{rel.}$ in the short wavelength IQE (λ < 500nm), but a more pronounced loss (4.5%$_{rel.}$) in the long wavelength domain (λ > 950nm). The other cell parameters are all competitive with INES' reference n-PERT devices. The shunt resistance is similar to what was observed for SOLENNA$_{(2)}$ devices.

"Conversion efficiencies of up to 19.8% were obtained on large-area Cz(n) wafers processed into n-PERT devices using only seven steps."

Conversion efficiencies of up to 19.8% were obtained on large-area Cz(n) wafers processed into n-PERT devices using only seven steps. To the authors' knowledge, this is the simplest n-PERT process ever introduced with such a level of performance. As the resulting cell architecture involves layers with high concentrations of dopant impurities, it needs to be verified that no related LID could occur that might alter the cell behaviour.

An initial evaluation of the long-term stability of SOLENNA$_{(3)}$ performance has been carried out: no efficiency degradation occurs after prolonged light exposure (>120h; 0.3sun; 50°C). The cell behaviour under reverse bias was also monitored and compared with that of reference n-PERT cells. Both reverse *I–V* curves and ReBEL mappings were compared in order to qualify the ultra-simplified SOLENNA$_{(3)}$ device as a candidate for PV module integration. As can be seen in Fig. 5, the typical ReBEL mappings obtained under a reverse bias of 10V are quite different, depending on the process flow involved. For each technology, corresponding batches of five solar cells had their reverse *I–V* curves measured in order to extract average values of: 1) breakdown voltage (V_{bd}), defined by the abscissa of the maximal curvature point; and 2) leakage current slope (d*I*/d*V*) in the 'hard breakdown' domain (i.e. for $|V| > V_{bd}$).

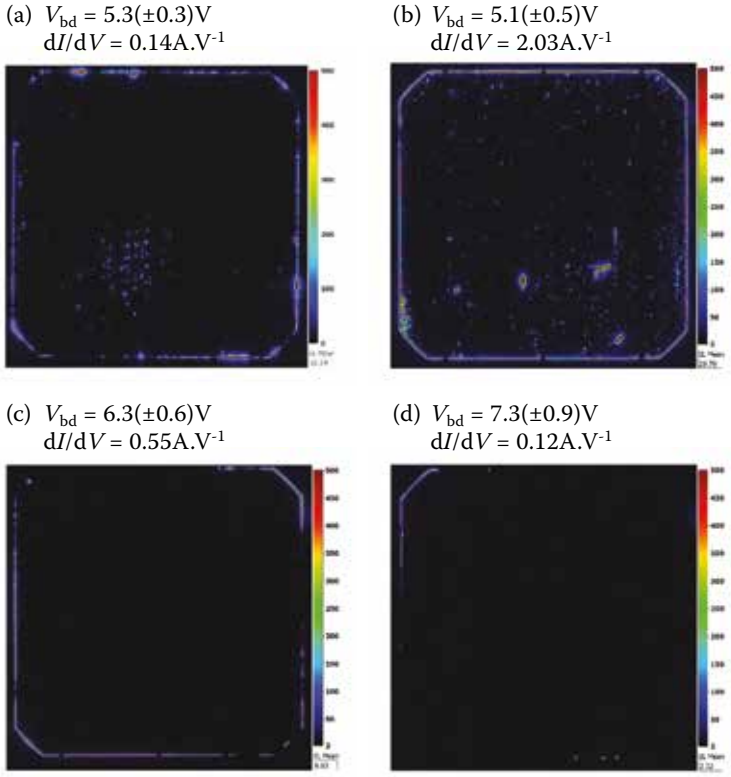

Figure 5. Reverse bias electroluminescence mappings for (a) reference SOLENN, (b) SOLENNA$_{(1)}$, (c) SOLENNA$_{(2)}$, (d) SOLENNA$_{(3)}$ n-PERT cells. For completeness, V_{bd} and d*I*/d*V* average values are given in each case.

The reference SOLENN and the SOLENNA$_{(1)}$ technologies, which involve at least one gaseous diffusion, exhibit both edge and surface defect signatures (see Fig. 5(a) and (b)). Reference SOLENN surface defectiveness is mainly caused by handling (the impact of which is accentuated by process flows involving many steps) [31]. The surface defect signature is nonetheless much more obvious in the case of SOLENNA$_{(1)}$ and is related to the aforementioned microporosity of SiO_xN_y:B/SiN to $POCl_3$, which leads to noticeable micro-shunts spread over the entire wafer surface. The corresponding cell electrical behaviour is degraded under reverse bias, as evidenced by a much steeper d*I*/d*V* slope (>2A.V^{-1}) compared with the average value obtained for SOLENN cells. On the other hand, SOLENNA$_{(2)}$ and SOLENNA$_{(3)}$ devices (Fig. 5(c) and (d)), which exploit exclusively dielectric layer doping sources, show only edge defectiveness and a slightly improved V_{bd}. Of course,

Technology	Wafer	Status	Average efficiency [%]	No. of processing steps
Al-BSF	Cz	Standard technology	19.0	5
PERC	Cz	Next p-type generation	20.0	8–9
Industrial PERT	Cz	In production – BBr_3	20.0	8–11
$SOLENNA_{(3)}$	Cz	Lab scale	20.0	7

Table 4. Summary of the cell technologies considered for the cost study.

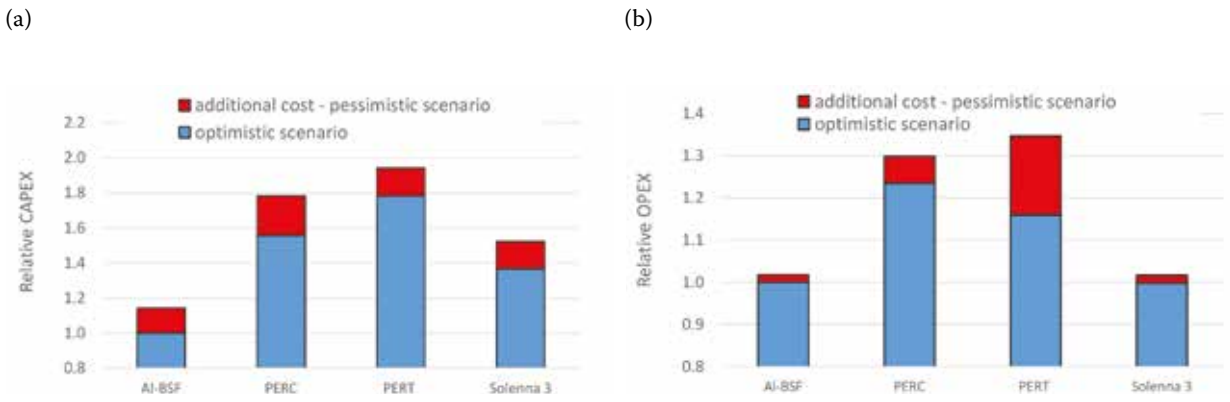

Figure 6. CAPEX (a) and OPEX (b) for PERC, PERT and $SOLENNA_{(3)}$, compared with the Al-BSF process.

the edge defect contribution can be removed by conventional laser edge junction opening. Such edge isolation is required in the case of the n-PERT cell architecture in order to meet PV module requirements (I < 1A at –12V).

Cost calculation

A cost study was performed to assess the economic advantage of $SOLENNA_{(3)}$ technology over the reference technologies listed in Table 4. The calculation addresses the cell process cost (CAPEX and OPEX), as well as the total cost of ownership (CoO) in €/Wp, including wafer and module contributions. The scenario of a production line in Europe with an annual capacity of 100MW was used. Parameters such as yield, uptime, manpower, building and facilities were adjusted with the number of process steps. Depreciations of 5 years for the equipment, 10 years for the facilities and 20 years for the building were fixed. No bifacial gain was considered in the study.

All the investigated processes were based on two scenarios: optimistic and pessimistic. This variation depends on the process complexity (number of steps) or on the characteristics of the equipment (throughput and cost). For the PERC process, additional steps – such as Al_2O_3 and rear SiN deposition, and laser opening – were added to the standard Al-BSF. Although this technology currently sets lab records of close to 22%, an average production efficiency of 20%, including possible LID losses, was considered for this study.

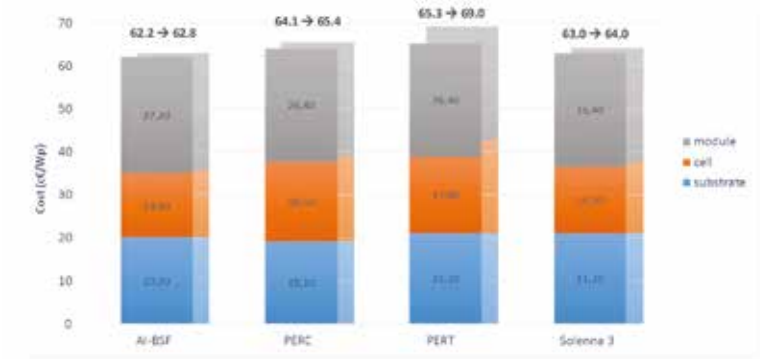

Figure 7. Contribution of wafer (blue), cell (orange) and module (grey) to the total CoOs, including optimistic (dark shades) and pessimistic (light shades) scenarios, and assuming a 10% higher price for n-type wafers. Total technology CoO ranges are indicated at the top of each bar.

The PERT BBr_3-based process can be performed in different ways, resulting in the number of processing steps ranging from 8 (so-called *PERT+*) to 11 (so-called *PERT-*). At the very least, the PERT process requires additional equipment, such as a BBr_3 tube furnace, wet bench for glass removal, and PECVD tool for the rear SiN layer.

The relative CAPEX for a standard Al-BSF production line is given in Fig. 6(a). For all the high-efficiency technologies investigated, a higher initial investment is required. PERC and PERT technologies show similar CAPEX ranges, corresponding to, in the best case, between 1.6 and 1.8 times the cost of a standard Al-BSF line. The pessimistic scenario of the PERT gaseous approach shows a more pronounced investment, because of the use of a diffusion barrier and specific emitter passivation by thermal oxide.

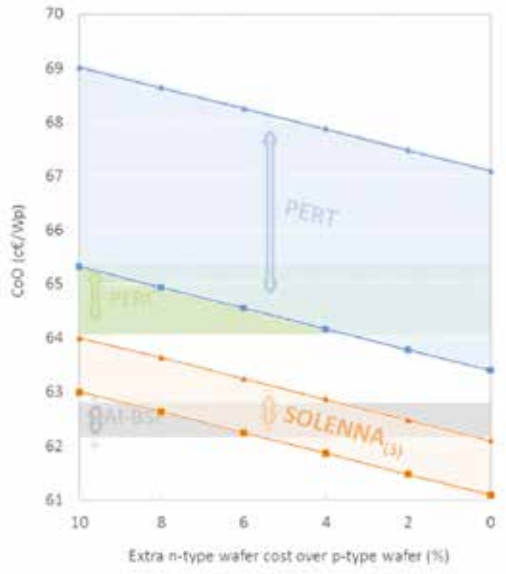

Figure 8. Total CoO ranges (€ct/Wp) as a function of the n-type wafer additional cost relative to p-type, for the various cell technologies under consideration ('+' and '-' refer to the optimistic and pessimistic scenarios respectively).

As expected, the required CAPEX for SOLENNA$_{(3)}$ is more favourable (about 1.4 times the cost of an Al-BSF line), because of the process simplicity. As regards the OPEX, presented in Fig. 6(b), SOLENNA$_{(3)}$ technology clearly outperforms PERC and gaseous PERT technologies, and is even equivalent to Al-BSF for both the optimistic and pessimistic scenarios. This is also explained by the reduced number of processing steps.

The CoO at the module level is shown Fig. 7 for the optimistic and the pessimistic scenarios. Both of the n-type technologies (PERT and SOLENNA$_{(3)}$) are penalized by the additional cost of the n wafer (considered here to be 10% higher than p-type), which leads to a more expensive PERT gaseous process than in the case of Al-BSF and PERC. Nevertheless, the very low cell process cost of SOLENNA$_{(3)}$ compensates for this weakness, thus allowing a very competitive technology at the module level. Indeed, the corresponding CoO remains slightly higher than that for Al-BSF, but clearly outperforms both PERC and gaseous PERT.

A comparison of the CoOs was then made, taking into consideration a reduction of 10% to 0% in the extra cost of n-type wafers compared with p-type wafers (Fig. 8). The validity of such an assumption increases with n-type market volume. Assuming the cost of n-type wafers is the same as p-type wafers, the CoO cost of 20%-efficient SOLENNA$_{(3)}$ technology would be in a range of 61.1–62.1€ct/Wp; this is even cheaper than 19%-efficient Al-BSF technology (62.2€ct/Wp).

Conclusion

The potential of dielectric doping layers for simplifying the manufacture of PERT solar cells was discussed, and the doping properties of the PECVD-deposited SiO_xN_y:B and SiN_x:P layers were presented. The status of the recent developments made at CEA-INES in 20%-efficient n-PERT was given via a description of following approaches: SOLENN (corresponding to INES' lab reference process based on BCl_3 and $POCl_3$ gaseous diffusions), SOLENNA$_{(1)}$ (mixing SiO_xN_y:B with $POCl_3$), SOLENNA$_{(2)}$ (pure dielectric co-diffusion route).

Finally, SOLENNA$_{(3)}$ technology was introduced for a simplified fabrication of n-type bifacial PERT cells in seven steps. This technology relies on the opportunity to combine doping, passivating and optical properties in the SiO_xN_y:B and SiN_x:P layers, which allows these layers to be retained in the final device architecture, with no detrimental effect on conversion efficiency: SOLENNA$_{(3)}$ devices achieving 19.8% efficiency have already been obtained on 243cm^2 Cz(n) wafers. Further improvements regarding cell efficiency (new generation of pastes, five to six busbars, passivation improvements) could collectively lead to a very high-efficiency, low-cost technology.

> "On the basis of possible n-type wafer cost reductions, SOLENNA$_{(3)}$ could become the most competitive technology."

At an industrial level, the cost study indicates that SOLENNA$_{(3)}$ technology can clearly compete with the classical Al-BSF technology in terms of cost per watt. A particular feature is that only a limited initial investment for new production lines, or additional investment for upgrading production lines, is necessary. Furthermore, the SOLENNA$_{(3)}$ processing sequence requires only one chemical (texturing) step, thus opening the door to significant reductions in facility costs, which is of interest in both economic and environmental terms. In addition, the potential extra power output (linked to device bifaciality) was not taken into account in this study. At the module level (CoO), SOLENNA$_{(3)}$ outperforms PERC, even with the higher wafer cost. On the basis of possible n-type wafer cost reductions, SOLENNA$_{(3)}$ could become the most competitive technology.

References

[1] SEMI PV Group Europe 2015, "International technology roadmap for photovoltaic (ITRPV): 2014 results", 6th edn (Apr.) [http://www.itrpv.net/Reports/Downloads/].

[2] Metz, A. et al. 2014, "Industrial high performance crystalline silicon solar cells and modules based on rear surface passivation technology", *Solar Energy Materials & Solar Cells*, Vol. 120, pp. 417–425.

[3] Kopeček, R. et al. 2014, "Bifaciality: One small step for technology, one giant leap for kWh cost reduction", *Photovoltaics International*, 26th edn.

[4] Lim, B. et al. 2014, "Simplifying the fabrication process flow of n-type PERT solar cells: Recent progress at ISFH", *Photovoltaics International*, 26th edn.

[5] Wang, J. et al. 2015, "Modeling and mass-production high efficiency n-type solar cells with ion-implanted selective back surface field", *Proc. 31st EU PVSEC*, Hamburg, Germany.

[6] Böscke, T.S. et al. 2014, "Fully ion implanted and coactivated

industrial n-type cells with 20.5% efficiency", *IEEE J. Photovolt.*, Vol. 4.
[7] Rothard, P. et al. 2014, "Characterization of $POCl_3$-based codiffusion processes for bifacial n-type solar cells", *IEEE J. Photovolt.*, Vol. 4, No. 3.
[8] Blévin, T. et al. 2014, "Development of industrial processes for the fabrication of high efficiency n-type PERT cells", *Sol. Energy Mater. Sol. Cells*, Vol. 131, pp. 24–29.
[9] Rothhardt, P. et al. 2014, "19.9 % efficient bifacial n-type solar cell produced by co-diffusion-CoBiN", *Proc. 29th EU PVSEC*, Amsterdam, The Netherlands, pp. 653–655.
[10] Cabal, R. et al. 2009, "Investigation of the potential of boron doped oxide deposited by PECVD – Application to advanced solar cells fabrication processes", *Proc. 24th EU PVSEC*, Hamburg, Germany, pp. 1605–1608.
[11] Blévin, T. et al. 2014, "Development of industrial processes for the fabrication of high efficiency n-type PERT cells", *Sol. Energy Mater. Sol. Cells* [http://dx.doi.org/10.1016/j.solmat.2014.06.022i].
[12] Frey, A. et al. 2014, "n-type bi-facial solar cells with boron emitters from doped PECVD layers", *Proc. 29th EU PVSEC*, Amsterdam, The Netherlands, pp. 656–660.
[13] Cabal, R. et al. 2014, "20% PERT technology adapted to n-type mono-like silicon: Simplified process and narrowed cell efficiency distribution", *Proc. 29th EU PVSEC*, Amsterdam, The Netherlands, pp. 648–652.
[14] Engelhardt, J. et al. 2015, "Passivating boron silicate glasses for co-diffused high-efficiency n-type silicon solar cell application", *Appl. Phys. Lett.*, Vol. 107, p. 042102.
[15] Keding, R. et al. 2012, "Silicon doping performed by different diffusion sources aiming codiffusion", *Proc. 27th EU PVSEC*, Frankfurt, Germany, pp. 1906–1911.
[16] Wehmeier, N. et al. 2015, "21.0%-efficient co-diffused screen printed n-type silicon solar cell with rear-side boron emitter", *physica status solidi (RRL)*, Vol. 1–5.
[17] Keding, R. et al. 2011, "Diffusion and characterization of doped patterns in silicon from prepatterned boron- and phosphorus-doped silicate glass", *Proc. 26th EU PVSEC*, Hamburg, Germany, pp. 1385–1389.
[18] Fallisch, A. et al. 2012, "Analysis of phosphorus doped silicon oxide layers deposited by means of PECVD as a dopant source in diffusion processes", *IEEE J. Photovolt.*
[19] Benick, J. et al. 2006, "PECVD PSG as a dopant source for industrial solar cells", *Proc. 21st EU PVSEC*, Dresden, Germany, pp. 1012–1015.
[20] Paviet-Salomon, B. et al. 2011, "Laser doping using phosphorus-doped silicon nitrides", *Energy Procedia*, Vol. 8, pp. 700–705.
[21] Wehmeier, N. et al. 2013, "Boron-doped PECVD silicon oxides as diffusion sources for simplified high-efficiency solar cell fabrication", *Proc. 28th EU PVSEC*, Paris, France, pp. 1980–1984.
[22] Engelhardt, J. et al. 2014, "Boron emitters from doped PECVD layers for n-type crystalline silicon solar cells with LCO", *Energy Procedia*, Vol. 55, pp. 235–240.
[23] Lachiq, A. et al. 1996, "Simultaneous dopant diffusion and surface passivation in a single rapid thermal cycle", *Prog. Photovolt. Res. Appl.*, Vol. 4, pp. 329–339.
[24] Barth, S. et al. 2014, "19.4 efficient bifacial solar cell with spin-on boron diffusion", *Energy Procedia*, Vol. 38, pp. 410–415.
[25] Das, A., Ryu, K. & Rohatgi, A. 2011, "20% efficient screen-printed n-type solar cells using a spin-on source and thermal oxide/silicon nitride passivation", *IEEE J. Photovolt.*, Vol. 1, No. 2.
[26] Barsch, J. et al. 2014, "21.8% efficient n-type solar cells with industrially feasible plated metallization", Presented at 4th SiliconPV 2014, *Energy Procedia*, Vol. 55, pp. 400–409.
[27] Jäger, U. et al. 2015, "Industrial n-type PERL cells with screen-printed front side electrodes approaching 21% efficiency", *Proc. 31st EU PVSEC*, Hamburg, Germany, pp. 390–393, 2015.
[28] Gall, S. et al. 2012, "High quality passivation scheme combined with laser doping from SiNx(P) and SiNx(B) layer for silicon solar cell", *Energy Procedia*, Vol. 27, pp. 467–473.
[29] Trogus, D. et al. 2011, "Phosphoric anti-reflective coatings as dopant source and front-side passivation for industrial silicon solar cell manufacturing", *Proc. 26th EU PVSEC*, Hamburg, Germany, pp. 1361–1364.
[30] Seiffe, J. et al. 2013, "Multifunctional PECVD layers: Dopant source", *IEEE J. Photovolt.*, Vol. 3, No. 1, pp. 224–229.
[31] Dauzou, F. et al. 2012, "Electrical behaviour of n-type silicon solar cells under reverse bias: Influence of the manufacturing process", *Sol. Energy Mater. Sol. Cells*, Vol. 104, pp. 175–179.

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