The use of silicon epitaxy in advanced n-type PERT and IBC silicon solar cell designs

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ABSTRACT

This paper gives an overview of the application of silicon epitaxy as a doping technology in bulk crystalline silicon solar cells. The large degree of flexibility in designing a doped profile in one process step, and the elegant way of locally creating doped regions, or simply achieving single-side doping by selective epitaxy, are presented. Other advantages – such as the absence of subsequent steps to drive in the doped region, to activate the dopants and to heal any damage or remove glassy layers – position the technology as a strong alternative to classical diffusion. Silicon epitaxy is possible on the flat and textured surfaces of solar material, and is compatible with cleaning sequences suited to industrial implementation. The integration of epitaxial layers in solar cells is capable of providing not only high efficiencies but also simplifications of the cell fabrication process, and, therefore, reductions in the cell cost of ownership (CoO). The proof of concept at the cell level has been demonstrated by the integration of boron-doped epitaxial emitters in n-type IBC and PERT solar cells: 22.8% efficiency for IBC (4cm^2) and 21.9% for PERT (238.9cm^2) devices have been obtained.

Introduction

The epitaxial growth of silicon on crystalline material consists of the regularly oriented growth of a crystalline silicon layer upon the substrate surface, where the substrate acts as a template for the growing layer [1–2]. Silicon epitaxy is possible not only on monocrystalline but also on polycrystalline material [3]. Moreover, the process is not restricted to mirror-polished surfaces, but is also applicable on typical Czochralski (Cz) material used in solar cell fabrication after saw-damage removal (SDR) or anisotropic texturing [4].

The doping of the epitaxial layer takes place by in situ incorporation of the dopant source during growth. In fact, epitaxy enables a high degree of flexibility in designing a doped profile in one process step, as both the dopant concentration and the thickness of the layer can be decoupled. In addition, after epitaxy there is no need for subsequent steps to drive in the doped region, activate the dopants, heal any damage or remove glassy layers.

The selective epitaxial growth of silicon can further reduce the complexity of cell fabrication when it is applied to locally create doped regions or to simply achieve single-side doping. In selective epitaxy, the process conditions are such that the net outcome of the silicon growth is the result of a balance between silicon deposition and silicon etching upon substrates where part of the surface is 'masked' with a dielectric/dielectrics, while the rest is 'free' of dielectric(s) [5]. The overall result is the growth of a

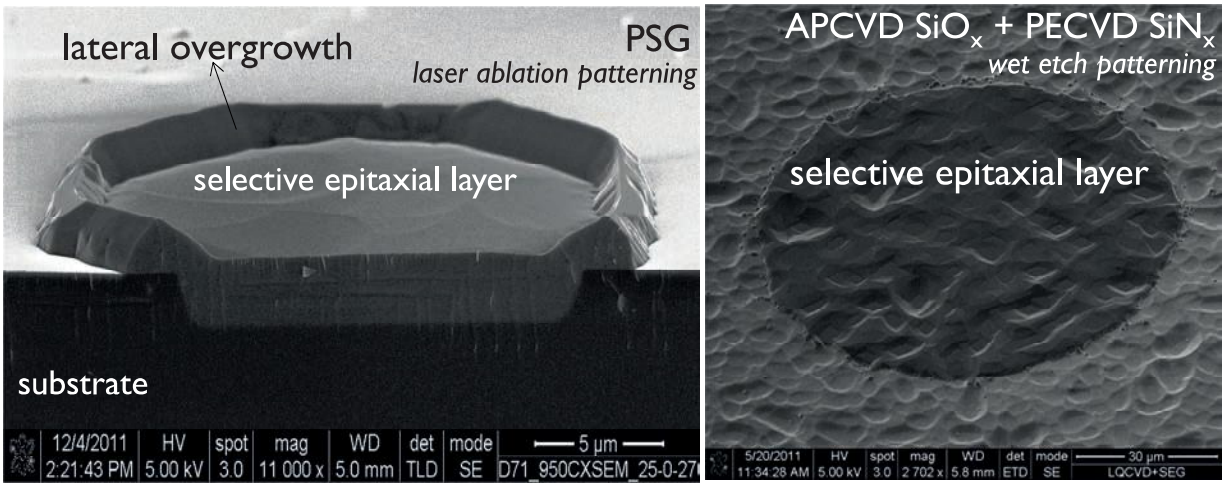

Figure 1. SEM images: examples of selective epitaxial growth on Cz silicon solar wafers using different dielectrics.

silicon layer solely on the areas 'free' of dielectric (Fig. 1). The dielectric can be kept after epitaxy for passivation and optical purposes, or can even serve as an additional dopant source [6].

"Silicon epitaxy is capable of realizing not only high efficiencies but also simplifications of the cell fabrication process."

In sum, the aforementioned benefits place epitaxy as a strong alternative technology to classical diffusion for creating the doped regions of bulk crystalline silicon solar cells. This paper first gives an overview of the application of epitaxy to bulk crystalline silicon technology; then a proof of concept at the device level is demonstrated for solar cell concepts, such as n-type passivated emitter and rear totally diffused (PERT) and interdigitated back contact (IBC). The integration of boron-doped epitaxial emitters on the rear side of these devices demonstrates that silicon epitaxy is capable of realizing not only high efficiencies but also simplifications of the cell fabrication process, and, thus, reductions in the cell cost of ownership (CoO).

Epitaxy on solar silicon wafers

This section begins by giving a general insight into silicon epitaxial technology; it then continues with a discussion of the impact of the substrate surface morphology, the cleaning prior to epitaxial deposition, the properties of the dielectrics used as a 'mask' during the selective deposition of silicon, and the doping profile capability of silicon epitaxy. The performance of boron-doped epitaxial emitters, used in cell concepts such as n-type IBC and PERT cells, is compared with that of reference boron-doped diffused emitters.

While not within the scope of this paper, the study is equally applicable to phosphorus-doped epitaxial layers.

Silicon epitaxy

In this work, the epitaxial growth of silicon is realized by chemical vapour deposition (CVD): the deposition of the silicon layer takes place by means of chemical reactions and surface absorption through a gaseous phase [1–2]. The process described herein takes place at a reduced pressure (<100Torr) and a temperature between 850 and 950°C. Dichlorosilane (SiH_2Cl_2) is used as the silicon source and hydrogen (H_2) as the carrier gas; however, it is also possible to use other precursors, such as silane or higher-order silanes (disilane, neopentasilane, etc.), or even organic precursors (triethoxysilane, tetramethylorthosilicate, etc.), if a lower process temperature (≤700°C) is required [7]. Diborane (B_2H_6) is employed as the dopant source, but other p-type and n-type sources are also available (BCl_3, PH_3, AsH_3, etc.).

Hydrogen chloride (HCl), which is a silicon-etching agent, is formed as a by-product of the deposition from SiH_2Cl_2. In the selective epitaxial growth of silicon, which is a balance between a simultaneous silicon deposition and etching, the HCl resulting from the SiH_2Cl_2 decomposition may be sufficient to maintain selectivity; on occasion, however, additional HCl needs to be supplied to the main stream for a selective growth [5] to take place. The growth rate for a selective epitaxial process is lower than that for a non-selective process, where no silicon etching occurs and a blanket silicon layer is deposited over the entire exposed surface.

The basic steps of an epitaxial process are temperature ramp-up, hydrogen bake, silicon deposition and cool-down. The hydrogen bake, taking place before the actual deposition step, is a critical step which assists overall in the growth of a high-quality epitaxial layer. One of the main goals of the hydrogen bake is to remove native oxide from the substrate surface by hydrogen reduction. If the native oxide were not removed, the deposition would lead to a highly defective epitaxial layer or a polycrystalline layer, or, in the case of selective growth, little or no deposition. In addition to the native oxide removal, the bake can also assist in annealing crystal damage and cause a desirable surface reconstruction, providing a region near the silicon surface which is free of oxygen [1–2]. There is a suitable trade-off between bake temperature, pressure and time in order to achieve a reduced surface defectiveness. The bake temperature has a key role, and, typically, higher bake temperatures result in lower defect densities. A process occurring at a reduced pressure also tends to provide a lower crystal defect component than a process at atmospheric pressure. The specific conditions also depend on the oxygen and moisture levels inside the reaction chamber [8].

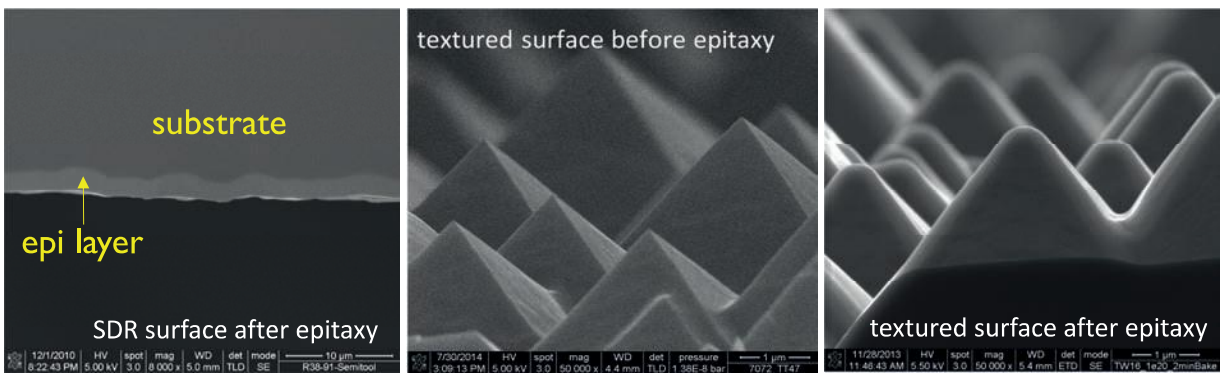

Figure 2. SEM images: (a) epitaxial layer grown on a KOH-SDR (saw-damage removal) silicon surface; (b) KOH-textured surface before epitaxy; (c) epitaxial layer grown on a KOH-textured surface.

The boron-doped epitaxial emitters described here have doping levels in the range 10^{18}–10^{20}cm^{-3} and thicknesses of ≤1µm. The growth rate for these layers ranges between 30 and 750nm/min, which depends not only on the process temperature but also on the possibility of performing a blanket or selective deposition.

Substrate surface morphology

The growth of epitaxial emitters can be realized on the rough surfaces resulting from an SDR process and on the random pyramidal surfaces following an anisotropic texturing process (Fig. 2). The growth of epitaxial layers on those surfaces requires an optimization of the growth conditions and, in a very particular way, an optimization of the bake conditions prior to the actual deposition step.

At the reduced pressure (<100Torr) and the temperature range (850–950°C) normally used to grow these boron-doped epitaxial emitters, a hydrogen bake of at least 2–5min is recommended in order to achieve a sufficient epitaxial quality on both flat and textured surfaces (Fig. 2). In those conditions, a measured total defect density of less than 10^4 defects/cm^2 in the boron-doped epitaxial emitters is confirmed to be sufficient for good performance at the solar cell level.

An investigation [9] of the influence of the substrate surface morphology (Fig. 3) demonstrates that an inline single-side chemical etching process based on HF:HNO_3 chemistry and realized on KOH-based textured surfaces can lead to values of dark-saturation current density (J_0) as low as those measured on surfaces resulting from an SDR process based on TMAH (14µm Si removal/side). In addition, the epitaxial emitters on textured surfaces produce J_0 values even lower than those using boron diffusion (see Fig. 3).

The better performance of the epitaxial emitter can be attributed to the rounding of the pyramid tips as a result of differences in crystal orientation between the pyramid planes and the peaks and valleys. The pyramid planes have a (111) crystal orientation, while at the peaks and valleys the orientation may be (100) or (110). The {111} planes present the highest packing density, which causes a slower growth rate during silicon epitaxy than on the other planes. The consequence is a thicker emitter on the pyramid tips and, therefore, a rounding of that surface compared with the pyramid planes (see Fig. 2). In the scenario where very thick epitaxial layers are grown, these differences

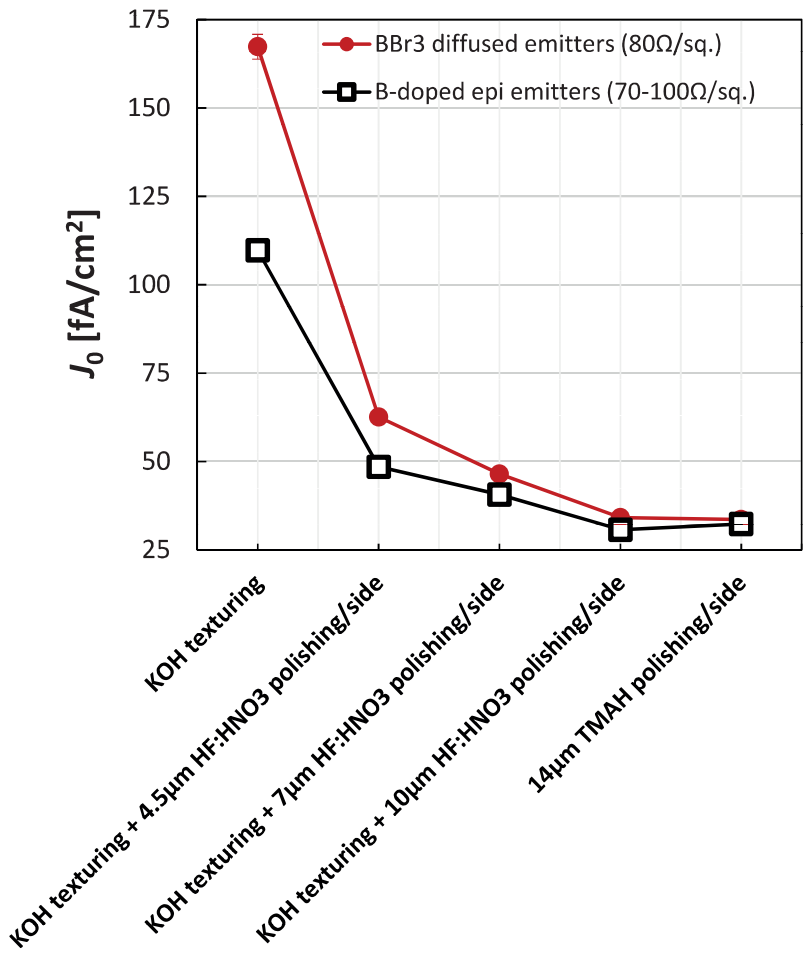

Figure 3. J_0 (extracted at 10^{16}cm^{-3}) for boron-doped epitaxial emitters and BBr_3-diffused emitters passivated with wet oxide ($\rho_{n\text{-type}}$ = 3.1Ω·cm) as a function of the substrate surface morphology.

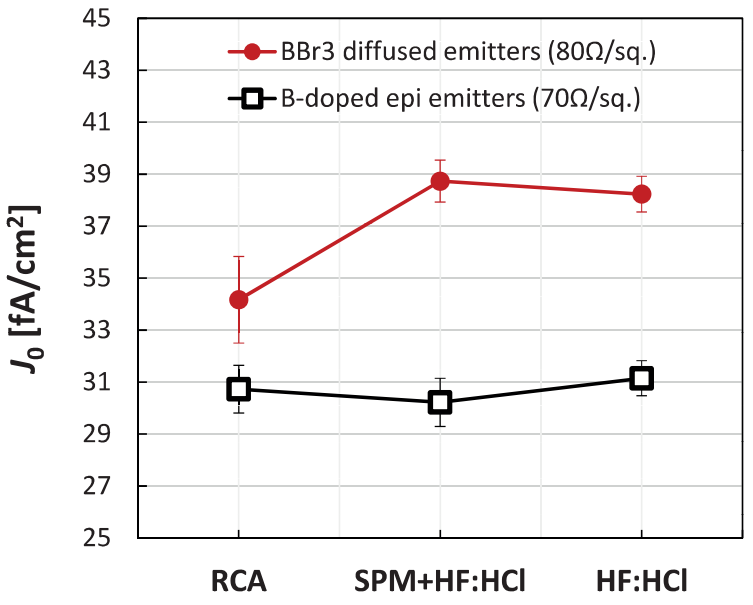

Figure 4. J_0 (extracted at 10^{16}cm^{-3}) for boron-doped epitaxial emitters and BBr_3-diffused emitters passivated with wet oxide ($\rho_{n\text{-type}}$ = 3.1Ω·cm) as a function of the cleaning method prior to doping.

could lead to a planarization of the original pyramidal surfaces.

Ex situ cleaning

As with diffusion, the growth of high-quality epitaxial emitters requires the removal of any particles and organic and metallic contamination from the silicon surface prior to the doping process. Wet chemical processes are normally used for the ex situ cleaning. A J_0 study [9] of the performance of the boron-doped epitaxial layers revealed that the technology is compatible with cleaning sequences suited to industrial implementation in PV, such as a simple HF:HCl sequence. J_0 values of around 30fA/cm^2 were measured (Fig. 4) for boron-doped epitaxial emitters (~70Ω/sq.) passivated with a thermally grown oxide, irrespective of the type of cleaning (RCA, SPM+HF:HCl and HF:HCl only) prior to the investigated doping process. The BBr_3 diffused emitter (~80Ω/sq.) also included in this investigation did not perform as well as the epitaxial emitter. In view of these results, 'new' cleaning chemistries – such as those based on the use of ozone as the main oxidizer – have also been successfully implemented and adopted as the reference process. With this line of approach, equivalent J_0 values have been measured when SOM (H_2SO_4:O_3 mixture) is used instead of SPM (H_2SO_4:H_2O_2 mixture).

Dielectrics and selective epitaxy

The selective deposition of silicon on Cz solar silicon wafers can be realized using a 'mask' consisting of a dielectric, or a stack of dielectrics which are of interest in PV applications: chemical vapour deposition (CVD) $SiO_x/SiO_xN_y/SiN_x$, atomic layer deposition (ALD) Al_2O_3, phosphosilicate glass (PSG), borosilicate glass (BSG) or thermal SiO_2. The patterning of those dielectrics prior to selective epitaxy can be performed using laser etching as well as wet or dry etching processes (see Fig. 1) [9]. Selective epitaxy provides an elegant approach to obtaining locally doped features or single-side doping, since those layers used as a 'mask' to guarantee selective growth can be retained after epitaxy for optical and passivation purposes.

> "Selective epitaxy provides an elegant approach to obtaining locally doped features or single-side doping."

Dielectrics such as plasma-enhanced chemical vapour deposition (PECVD) SiO_x exhibit excellent passivating properties directly after emitter formation by selective epitaxy (Table 1); this results from a post-deposition annealing of the dielectric layer taking place during emitter formation by selective epitaxy. This annealing increases the structural order of

After PECVD SiO_x deposition		T epitaxy [°C]	After epitaxy	
τ_{eff} [µs]	J_0 [fA/cm^2]		τ_{eff} [µs]	J_0 [fA/cm^2]
~10	–	850	1360	9.3
		950	1750	11.6

Table 1. Effective lifetime τ_{eff} (at 10^{15}cm^{-3}) and dark-saturation current density J_0 (at 10^{16}cm^{-3}) for a symmetric structure: PECVD SiO_x (19nm)/n-type diffused region (310Ω/sq.)/n-type Cz wafer (KOH-texturing, 3.9Ω·cm)/n-type diffused region (310Ω/sq.)/PECVD SiO_x (19nm).

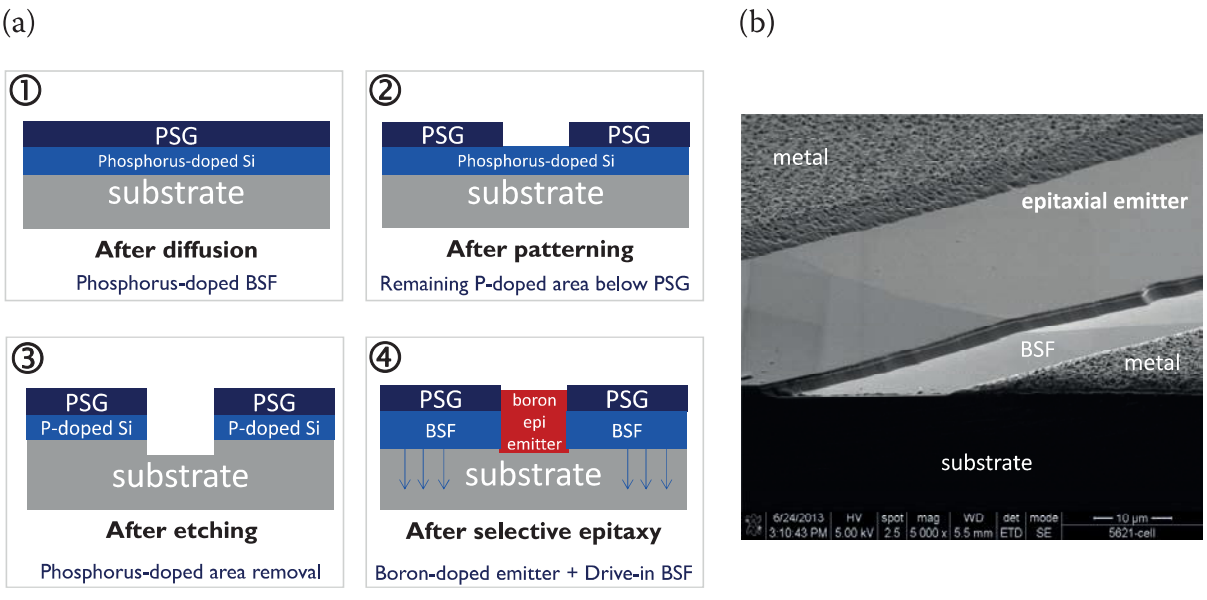

Figure 5. (a) Schematics of the approach used to form the interdigitated junction in an IBC cell using boron-doped selective epitaxy to PSG. (b) SEM image of the final layout of the interdigitated junction in an IBC cell created using this approach.

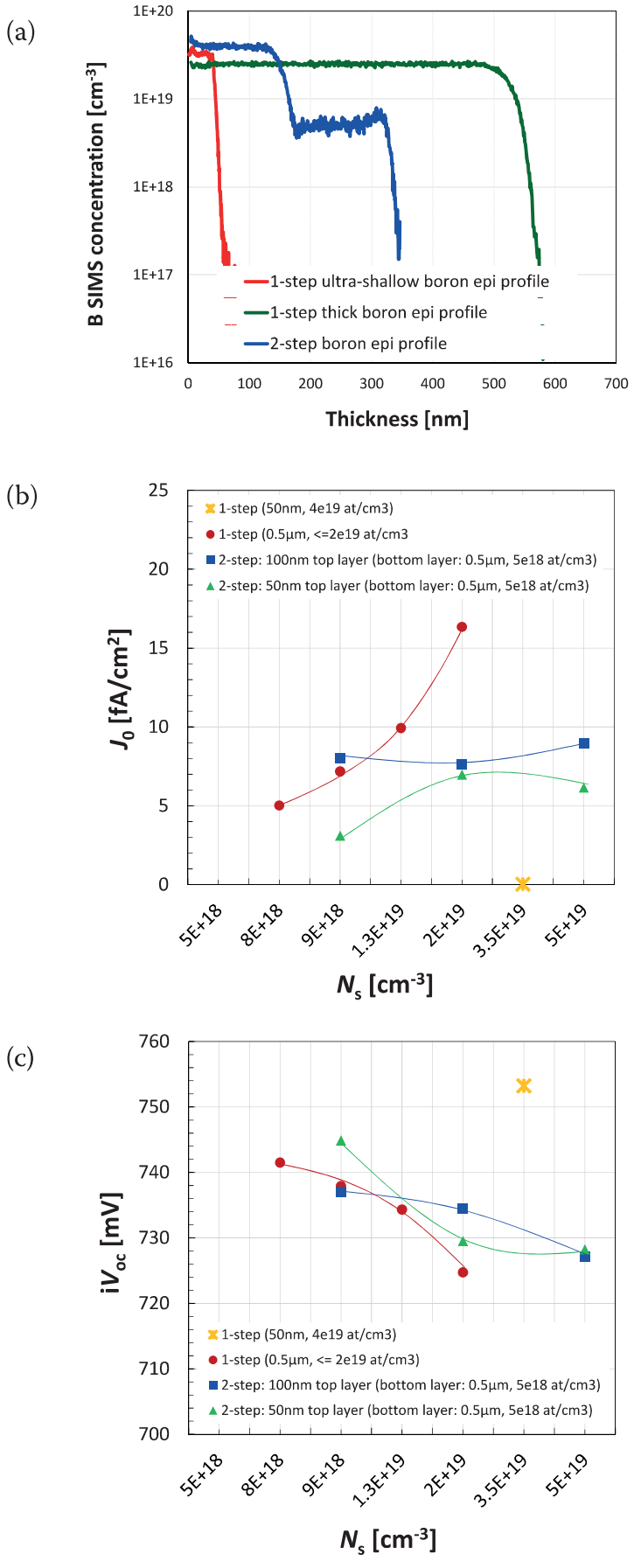

Figure 6. (a) Examples of one-step and two-step boron-doped epitaxial profiles. (b) $J_{0,pass}$ (extracted at $10^{16}cm^{-3}$) for boron-doped epitaxial profiles. (c) iV_{oc} for boron-doped epitaxial profiles.

the dielectric layer and therefore its quality, as observed by IR spectroscopy [10–11] and lifetime measurements by PL-QSSPC (Table 1).

During selective epitaxy, doped dielectrics can be used as a 'mask' too. The advantage here is that the thermal budget associated with the epitaxial process can drive the dopant source into the silicon regions 'masked' by the doped dielectric, while the growth of an epitaxial layer takes place simultaneously in the areas 'free' of dielectric [6]. A specific case of this application has been developed to create the interdigitated rear junction of an IBC cell [9]. Here, a short, low-temperature $POCl_3$ diffusion was carried out to create an approximately 20nm-thick PSG layer, which, after patterning, was used as a 'mask' for the selective growth of the boron-doped epitaxial emitter in the areas 'free' of PSG. While the emitter growth is taking place, a further phosphorus drive-in from the PSG creates the final back-surface field (BSF) profile, with the interdigitated junction of these IBC cells being formed after the selective epitaxial step (Fig. 5).

Advanced doping profiles

The doping flexibility of epitaxy in a single process step brings the possibility of creating doped regions with a wide variety of uniform box-type profiles by changing the gas flows, modifying the precursors, or adapting the deposition time, temperature and pressure. Ultra-shallow (≤100nm) and thick (≥500nm) one-step as well as two-step boron-doped profiles, passivated with the stack ALD Al_2O_3 (10nm)/PECVD SiO_x (120nm), and with a sufficient surface concentration (N_s) for good ohmic contact with sputtered AlSi 1%, have demonstrated high performance in terms of recombination losses (Fig. 6) [11]. Several one-step and two-step profiles of around 500nm have provided J_0 values and implied V_{oc} values at 1 Sun (iV_{oc}) in the range 4–10fA/cm² and 725–745mV respectively [11]. Values of J_0 < 1fA/cm² and iV_{oc} = 754mV have also been measured for an ultra-shallow and very heavily doped layer (50nm, $4 \cdot 10^{19} cm^{-3}$), where the field-effect passivation is the dominant mechanism [12].

N-type cells with a boron-doped epitaxial emitter

IBC cells

In a first approach, represented in Fig. 7(c) as 'Route A', selective epitaxy was implemented to create

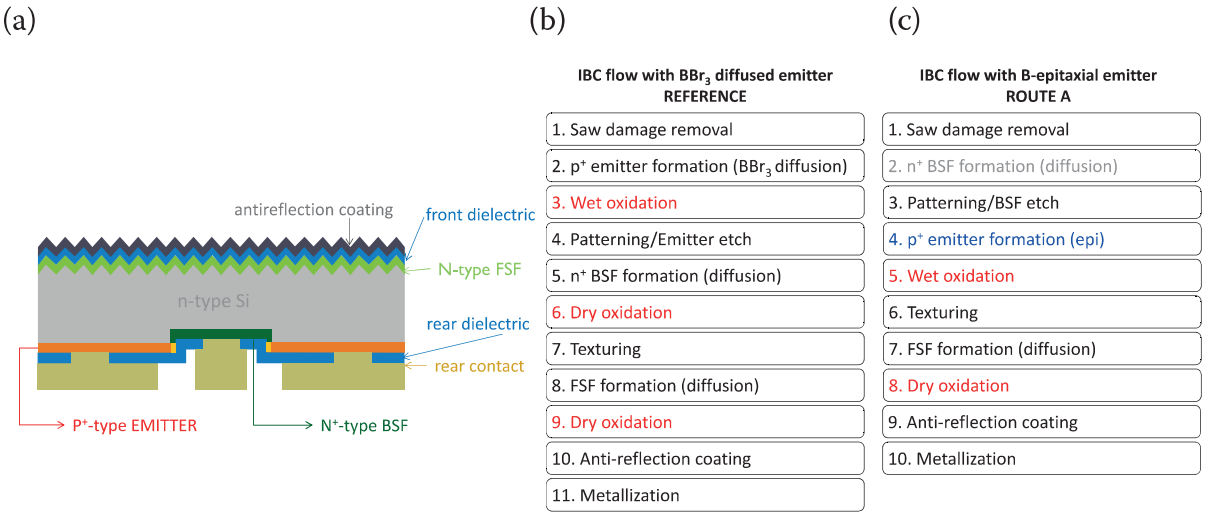

Figure 7. (a) Schematic of an IBC cell. (b) Reference IBC flow with a BBr_3-diffused emitter. (c) IBC flow ('Route A') with a boron-doped emitter grown by selective epitaxy to PSG.

		J_{sc} [mA/cm^2]	V_{oc} [mV]	*FF* [%]	η [%]
Diffused baseline flow (reference)	Average	41.5 ± 0.3	684 ± 3	80.3 ± 0.5	22.8 ± 0.4
	Best	41.7	686	80.7	23.1
Flow with epi emitter ('Route A')	Average	41.8 ± 0.1	684 ± 1	79.1 ± 0.6	22.6 ± 0.2
	Best	41.9	686	79.5	22.8

Table 2. Light *I–V* results for IBC cells (4cm^2) fabricated using the reference flow (Fig. 7(b)) and 'Route A' with an epitaxial emitter (Fig. 7(c)).

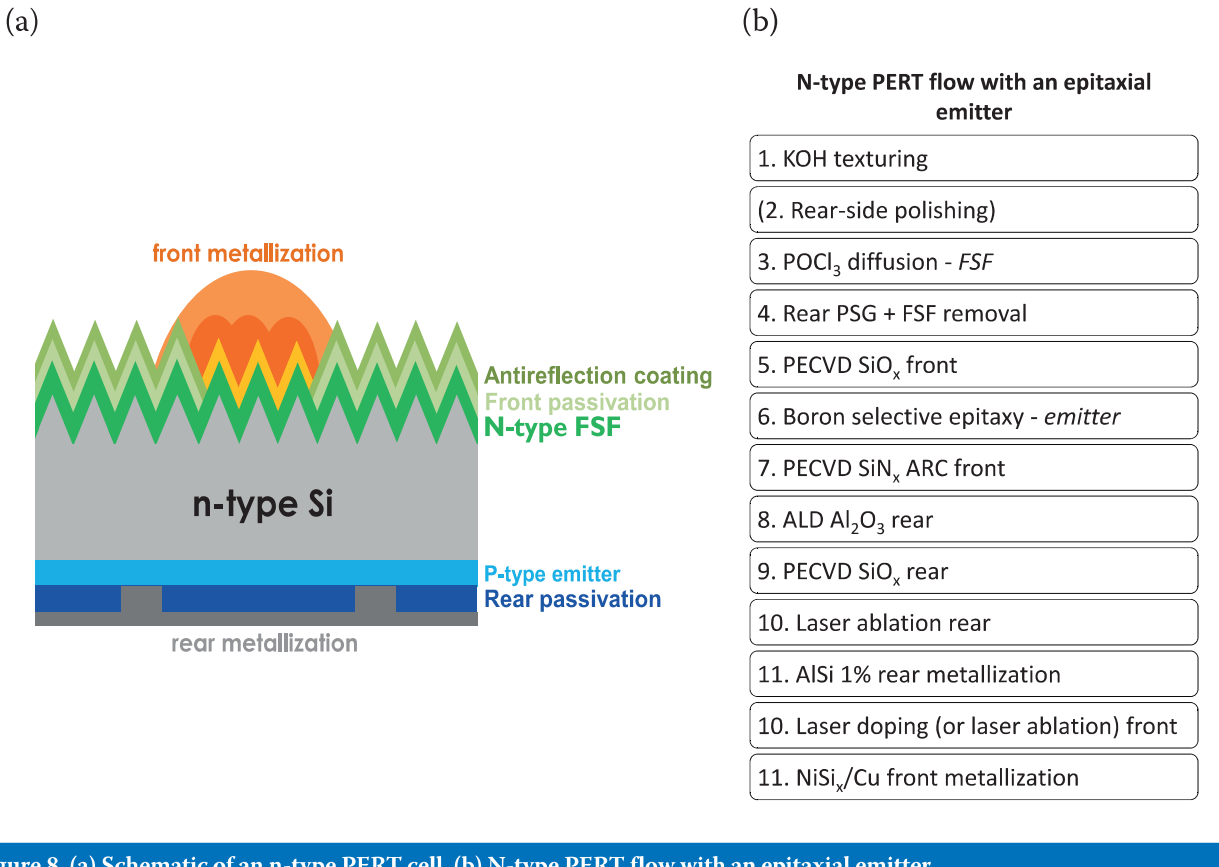

Figure 8. (a) Schematic of an n-type PERT cell. (b) N-type PERT flow with an epitaxial emitter.

Epitaxial emitter		J_{sc} [mA/cm^2]	V_{oc} [mV]	*FF* [%]	η [%]
@ 850°C, 500nm, 9·10^{18}cm^{-3}	Average	39.7 ± 0.1	685 ± 1.6	78.9 ± 0.8	21.5 ± 0.3
	Best	39.7	687	80.1	21.9

Table 3. Light *I–V* results for the n-type PERT cells (238.9cm^2) fabricated using the flow in Fig. 8(b) with an epitaxial emitter grown on a flat rear surface. Front side: shallow (280nm) diffused FSF below the dielectric, and deep (~2µm) laser-doped region below the metal contact.

		J_{sc} [mA/cm^2]	V_{oc} [mV]	*FF* [%]	η [%]
Rear flat	Average	39.2 ± 0.1	664 ± 1	79.8 ± 0.2	20.8 ± 0.1
	Best	39.1	666	80.1	20.9
Rear textured	Average	39.3 ± 0.1	660 ± 0	79.3 ± 0.4	20.6 ± 0.2
	Best	39.5	661	79.9	20.8

Table 4. Light *I–V* results for the n-type PERT cells (238.9cm^2) fabricated using the flow in Fig. 8(b) with an epitaxial emitter (500nm, 2·10^{19}cm^{-3}) grown on flat and textured surfaces. Front side: non-optimized, homogeneous diffused FSF (400nm) below the dielectric and the metal contact (contact patterning by laser ablation).

the interdigitated junction of n-type IBC cells (Fig. 7(a)) using the PSG formed during the $POCl_3$ diffusion of the BSF as a 'mask' in the selective deposition of the emitter (Fig. 5) [9]. This route, with an epitaxial emitter, directly simplifies the fully diffused reference flow (Fig. 7(b)) by enabling a 40% reduction in the total diffusion and oxidation processing time as well as by omitting some cleaning steps. The main *I–V* results of the first 4cm^2 IBC cells manufactured on 156cm^2 Cz silicon solar wafers are summarized in Table 2. The results confirm best cell efficiencies of up to 22.8% for the IBC flow with a selective epitaxial emitter; this value is close to the efficiency of 23.1% for the more complex reference flow with a diffused emitter.

> "The results confirm best cell efficiencies of up to 22.8% for the IBC flow with a selective epitaxial emitter."

The high potential of selective epitaxy to simplify the IBC flow while keeping a high-efficiency performance opens up new possibilities for redefining a simpler fabrication sequence for this type of device and, hence, for reducing the cell CoO [13].

PERT cells

The route for fabricating n-type PERT cells with a boron-doped epitaxial emitter (Fig. 8) relies on single-side processing for the rear-emitter formation by selective epitaxy, and on the dielectric deposition of a PECVD SiO_x/SiN_x stack on the front side and an ALD Al_2O_3/PECVD SiO_x stack on the rear. This approach allows a single-side rear emitter, as selectivity is ensured by the presence of the PECVD SiO_x on the front side. After emitter formation, the PECVD SiO_x can be used as an excellent passivating layer of the n-type front-surface field (FSF) of these devices (see Table 1) [4,11,14].

The *I–V* results for the first n-type PERT cells fabricated using a half-micron-thick epitaxial emitter and a laser-doped front-side metallization scheme are summarized in Table 3. Best cell efficiencies of up to 21.9% (238.9cm^2) were measured for an emitter with a uniform doping of 9·10^{18}cm^{-3}.

Although the main focus has been the proof of concept for an n-type PERT solar cell with a flat rear side, epitaxy can also be applied to textured surfaces [4]. The fabrication of n-type PERT solar cells with both flat and textured rear sides, a non-optimized homogeneous diffused FSF and a laser-ablated front metallization scheme [14] confirms the high potential of the approach with an epitaxial emitter on textured surfaces. Both flat and textured surfaces yield comparable cell efficiencies – for the latter, they are 0.1–0.2% abs. lower (Table 4). This difference is due mainly to a drop in V_{oc} of around 5mV. In-house cell CoO calculations confirm that the slightly higher efficiency for a flat rear surface does not offset the reduction in CoO resulting from the omission of the rear-side polishing.

Epitaxial reactor

The growth of the epitaxial layers in this work was accomplished in a single-wafer batch reactor, which, although sufficient for R&D purposes, is not a satisfactory solution for a production line. Actually, the tool concept which would deliver the required industrial throughput for the growth of thin epitaxial layers for PV applications is a *tubular hot-wall reactor* [15–17], for which there are designs capable of realizing the loading of 1200 solar wafers per process chamber [18]. With these systems the CVD process is normally performed at a reduced pressure and at a temperature ranging between 400 and 900°C. In these conditions, the operation is in the kinetically limited regime, where the growth rate is exponentially dependent upon the temperature, which is very accurately controlled.

At the reduced pressure, the gas diffusivity is significantly increased compared with the values at atmospheric pressure. The net effect is a greater than one order of magnitude increase in the gas-phase transfer of reactants to, and by-products from, the substrate surface. Systems operating at reduced pressure can therefore benefit from the following aspects: 1) surface kinetic control is readily achieved; 2) wafers can be vertically stacked and packed very close together; 3) little or no carrier gas is required; 4) epitaxially grown layers feature a better step coverage, conformality and a lower defect density; and 5) deposits

on the hot-wall reactors adhere very well and tend not to flake off.

In theory, there are no differences in process and performance between horizontal and vertical hot-wall reactors. Nevertheless, experience has proved the superiority of the vertical design because of practical reasons, such as its more compact layout; therefore the technological improvements have been historically first designed for, and implemented in, vertical furnaces.

With respect to the CoO for the tool, not enough experience has so far been gained in PV to have clear figures for a system dedicated to growing thin epitaxial layers (≤1µm) for bulk crystalline silicon solar cells. Epitaxy is not a technology currently employed in the PV industry, and most of the existing knowledge has been acquired from microelectronics.

The CoO calculations for an epitaxial reactor will depend on the specific tool design, the process conditions (including deposition temperature), the precursors and the carrier gas. All these variables will also determine the final load per batch as well as the growth rate. Compared with a BBr_3 diffusion process, for which the CoO is typically in the range €0.05–0.07/wafer, the CoO for a furnace dedicated to the growth of boron-doped thin epitaxial layers could be in the range €0.08–0.13/wafer. The difference arises mainly from a larger investment cost (CAPEX) for an epitaxial furnace.

The data used in the CoO calculations for an epitaxial furnace have their main origin in a microelectronics setting, where the specifications are more stringent than in PV, because of the need to work in a cleanroom environment and the micro- and nanoscale dimension of the devices in this field. A reduction in the investment costs for a system dedicated to PV could therefore be envisaged, as this system could be designed in more relaxed terms than one for microelectronics. Furthermore, it should also be taken into account that with epitaxy there is no need for subsequent steps, such as BSG removal or the usual boron drive-in, which engender a reduction in the cell CoO. In general, once the first tool exists, and taking into consideration the learning curve, a tendency towards lower figures should be expected for the CoO of an epitaxial PV furnace. Experience should bring down the costs, as long as the process becomes as mature and developed as the well-established diffusion process.

Conclusions

This paper has presented an overview of the application of silicon epitaxy as a doping technology in bulk crystalline silicon solar cells. A general picture was first given of the process conditions for the growth of epitaxial layers on the typical flat and textured surfaces used in solar cells fabrication, as well as of the cleaning before epitaxy. This was followed by a description of the advantages in terms of performance and simplifications associated with the large degree of flexibility in designing a broad range of doping profiles, and with the use of selective epitaxy to create locally doped regions.

> "Epitaxy technology is a powerful alternative to classical diffusion for creating the doped regions of bulk crystalline silicon solar cells."

Finally, the proof of concept at cell level was demonstrated by the growth of boron-doped epitaxial emitters in n-type IBC and PERT solar cells: 22.8% efficiency for IBC (4cm^2) and 21.9% for PERT (238.9cm^2) solar cells with a 0.5µm boron-doped epitaxial emitter have been achieved. These results prove that epitaxy technology is a powerful alternative to classical diffusion for creating the doped regions of bulk crystalline silicon solar cells.

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