# When capacity buys are not an option: Technical trends in c-Si cell manufacturing and their implications

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ABSTRACT

Economics will always play a crucial role in the way PV technology advances. However, the current generation of products is facing substantial business challenges in the attempt to scale the product technologies. This paper is the fifth in a series covering business analysis for PV processes. The methods applied in these papers fall into two categories: cost of ownership (COO) modelling and cost and resource modelling. Both methods examine the business considerations associated with the adoption of new processes, tools or materials. This is more critical than ever. Near-term issues – in some cases the survival of the business – heavily influence today's decision processes. This paper tries to identify the areas that it is thought will produce the largest near-term paybacks. The areas identified are n-type wafers, $Al_2O_3$ passivation and copper metallization.

## Solar cell production outlined

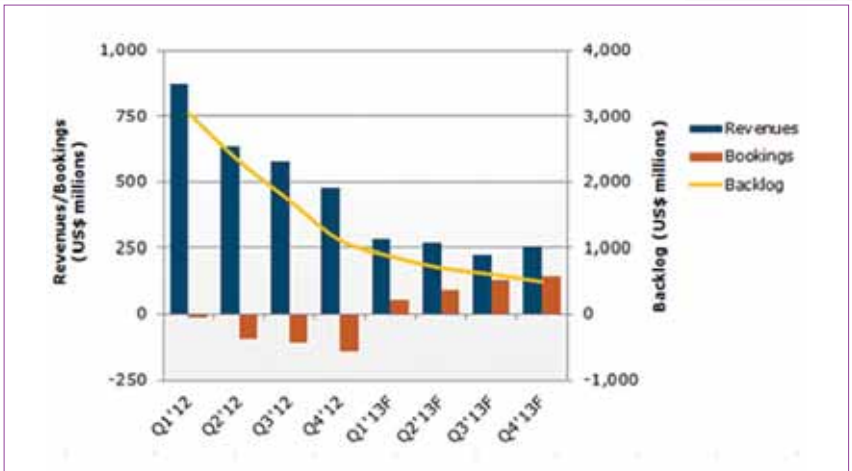
Any discussion of technical changes to any steps in crystal silicon (c-Si) PV manufacturing must take into consideration the entire solar cell production flow. Therefore, before the processes of interest are described, it is worth first outlining the baseline process through which the silicon wafer travels on its way to becoming a fully-fledged solar cell.

The silicon wafer is sliced from a monocrystalline or multicrystalline silicon ingot. This step can be carried out either directly at the silicon foundry or by the solar cell manufacturer. The sliced wafer then goes through several distinct manufacturing steps, after which it is ready for mounting into a solar panel.

The first step in the cell manufacturing cycle is wet etching, which is described in depth in the second paper in this series [1]. Here, the imperfections created in the sawing process are removed, after which the wafer's surface is texturized to create the microscopic pyramid structures that will enable it to trap sunlight rather than reflecting it.

Described in the first paper in this series [2], the second step is a thermal diffusion process whereby an n-type layer is diffused through the wafer's top layer and down into its structure. Typically made of phosphorus-rich material, this n-type layer combines with the wafer's own p-type material to create the cell's p-n junction, a planar semiconductor device that will generate electrical current. During the diffusion process, a layer of glass is created on the surface of the cell and is removed in an additional etching and de-glassing process.

In the third step, the cell's antireflective (AR) layer is laid down in a plasma-enhanced chemical vapour deposition (PECVD) process that gives the cell its blue colour, after which the cell is ready for metallization. This was described in detail in the third paper in this series [3]. The PV industry uses screen printing as the method of choice for depositing silver and aluminium onto its solar cells.




Credit: NPD Solarbuzz

**Figure 1. Forecast PV-specific metrics for the top 10 PV equipment suppliers.**

## Market trends

Solar PV equipment spending was US$3.6 billion for 2012, down from US$12.9 billion in 2011, according to new research in the latest NPD Solarbuzz PV Equipment Quarterly report. Covering c-Si from ingot to module and thin film, the report says spending for 2013 could drop to levels not seen in the industry since 2006. "Spending for 2013 is forecast to decline even further to US$2.2 billion," said Finlay Colville, Vice-President of NPD Solarbuzz. The market analyst group expects only eight PV equipment suppliers to have PV-specific revenues during 2012 in excess of US$100 million, compared to twenty-three in 2011.

"Excessive investment in 2010 and 2011 was the catalyst of the over-capacity and over-supply situation that exists today. It was also a key factor in end-market price erosion that forced many of their customers to file for insolvency. The days of PV-specific backlogs and revenues at the billion-dollar level are unlikely to be repeated for at least three years," stated Colville.

With so much competitive c-Si capacity shipped during 2011 and 2012, NPD Solarbuzz states that the biggest fear for tool suppliers is the emergence of a secondary equipment market across China and Taiwan. Most importantly, this would delay any upturn in equipment spending.

> "The biggest fear for tool suppliers is the emergence of a secondary equipment market across China and Taiwan."

With regard to module shipments and revenues, IHS iSupply is expecting overall global installation markets to pick up again after the first six months of 2013 and then continue to improve over the rest of the year. Meanwhile, overcapacity that had built up because of massive investments in 2010 and 2011 will have less dramatic repercussions in 2013 than in 2012.

The IHS report said the decline in PV module prices afflicting the market will slow down in 2013 and then eventually stop by the second half of the year. By the fourth quarter of 2013, average crystalline module prices are forecast to reach US$0.55 per watt, down 14% from the same time in 2012, compared to a bigger contraction of 32% between the fourth quarter of 2011 and 2012. Overcapacity and a decline in pricing, as well as slowing growth in key worldwide markets, will serve to keep the global PV market for solar modules depressed, with recovery not expected until well into the second half of 2013. While this sounds better than the scenario for equipment suppliers, double-digit price erosion is not something that the market can sustain indefinitely.

This is not a rosy picture for the PV market, or its supply chain, and one of the conclusions is that, for many, it may never be so again. Why? The larger macroeconomic environment has changed. To a large degree, PV remains dependent on favourable government policies (subsidies, feed-in tariffs, carbon taxes, etc.). These policies are struggling to gain (or maintain) traction as governments (e.g. USA, Spain, Italy) struggle with massive budget deficits and accumulated debt. Separately, the widespread use of hydraulic fracturing has reduced the price of natural gas (a competing source of electricity generation) by a factor of three. Further, the natural gas supply chains are extremely well capitalized, involving some of the largest and most profitable corporations in the world.

In short, there is an oversupply of product, a substantial risk on the demand side due to financial constraints with governments, and a competitive technology (natural gas) that has undergone substantial and sustainable cost reductions.

What does this mean going forward? The bar has been raised. It is tempting to compare the solar industry with the semiconductor industry, where boom and bust cycles are common. However, the boom–bust cycles in the semiconductor industry have almost always been traced to basic supply and demand. It has been decades since that industry was highly dependent on government policy, and most of the competition has come from within the integrated circuit (IC) industry, not from competing technologies outside the industry.

One clear reality – there is no more room for current-generation 'me too' PV roadmaps. Current 'me too' products are unlikely to be profitable for a long time, if ever. With double-digit price erosion for c-Si modules, manufacturers must look for competitive advantages and those cannot be had with older, off-the-shelf processes. Upgrading processes is the only potentially viable business plan. In practice, companies should get accustomed to continuous upgrading; a static solar cell factory will not remain competitive for long, now or at any time in the foreseeable future. Just to be clear, the market will punish those who do nothing to improve their processes. As hard as it is to invest in a down cycle, it is the only way to survive.

> "Upgrading processes is the only potentially viable business plan."

Does that mean the end of 'turnkey factory sales'? The authors think that is a likely outcome. Additionally, module manufacturers are acquiring unique technologies at the cell level to ensure their survival through sustainable competitive advantages. As a result, it is expected there will be several announcements involving a deeper level of partnering (probably including acquisitions) of novel cell manufacturers and intellectual property (IP) developers before their technologies have been released to the broader market.

## Technology upgrades

The question then becomes, given the current challenges, where does one look for these technology developments that have the potential to create competitive advantages? This section looks at the best guesses for short-term opportunities – those that can begin to make an impact within 12 months, as well as other potential areas of interest. This section concludes by looking at one 'up-and-coming' approach to achieving improvements in cell efficiency and reductions in cell manufacturing costs.

### N-type wafers [4]

An early driver of PV was satellites. P-type (boron-doped) cells (i.e. cells based on p-type wafers) proved to be less sensitive to degradation caused by exposure to cosmic rays than n-type cells. This early application drove p-type cell development and that is where most production remains today. Recent research suggests a likely move to n-type (phosphorus-doped) cells. The results have shown a potential to outperform p-type cells in terms of efficiency. According to the International Technology Roadmap for Photovoltaics (ITRPV 03/2012), the market share of n-type cells could reach approximately 30% of the monocrystalline silicon solar module market by 2015 (currently around 5%).

An advantage of n-type cells is that they do not suffer from the light-induced degradation (LID) seen in p-type cells. In addition, n-type cells are less sensitive to impurities that are typically present in silicon feedstock. Consequently, n-type cells with higher efficiencies can theoretically be produced at a lower cost than p-type cells using the same wafer-manufacturing methods (Czochralski crystal pulling). N-type wafers, however, show a larger distribution of electrical resistance. This leads to a reduction in the number of wafers obtained from an ingot. One proposed solution is to use a continuous-feed Czochralski puller, which would provide equipment companies with new sales opportunities.

### $Al_2O_3$ passivation [5]

$Al_2O_3$ is of increasing interest because of the promise it holds for providing excellent passivation of p-type c-Si surfaces on industrially feasible scales. While $Al_2O_3$ exists in different crystalline forms, amorphous $Al_2O_3$ films are used for passivation layers. The films are transparent over the wavelength region of interest for solar cells. $Al_2O_3$ films for c-Si surface passivation can be deposited by atomic layer deposition (ALD) and PECVD, as well as by physical vapour deposition (PVD) sputtering. Sol-gel processes have also been investigated. Annealing of the films is typically required to achieve a high level of surface passivation. Results of $Al_2O_3$ with n-type cells have shown efficiencies greater than 23%.

PECVD and PVD are certainly scalable in c-Si PV manufacturing. The competitive edge of existing PECVD systems is that they can easily be modified to avoid large investments in new technologies. The results reported for PVD have not been as good as for PECVD and ALD. Conventional ALD is unsuitable for high-throughput solar cell production. However, throughput can be addressed by batch processing or through spatial-ALD (based on spatial separation of precursor gases instead of time-based separation), which would allow in-line atmospheric processing.

With regard to cost, it has been reported that the deposition of $Al_2O_3$ can be accomplished for just a few cents per cell. However, the implementation of rear-surface passivation schemes can have a major impact on cost of ownership (COO). One important cost-related finding is that passivation using $Al_2O_3$ does not require a semiconductor-grade precursor, and that solar-grade $Al(CH_3)_3$ produces excellent results, as does using less pyrophoric precursors.

## Cu metallization [6]

The metallization of c-Si cells is one of the main cost drivers in the manufacturing process [3]. Screen printing of silver pastes is still the dominant technique, but the need to replace silver with copper in order to lower costs is widely acknowledged. While elemental silver has better conductivity than elemental copper, electroplated copper has superior conductivity when compared with current silver pastes: data indicate up to a 0.5% cell efficiency improvement with electroplated copper.

Using copper as an electrode material for c-Si cells presents a number of issues that need to be addressed. First, copper diffuses into the silicon, where it forms a trap for the charge carriers in the semiconducting material: consequently, a diffusion barrier is required. Second, copper (unlike silver) oxidizes into a porous compound when exposed to air; addressing this issue requires extra protection of the electrode contact (e.g. capping). Third, the use of copper as an electrode material increases the complexity of the solar cell manufacturing process. For example, in order to make contact with the silicon wafer, the silicon nitride passivation layer must be opened by either etching or laser ablation. Subsequently, a diffusion barrier must be deposited followed by copper deposition. The latter can be done by electroplating, a technique that is well known in the IC industry, albeit at throughputs far below the requirements for solar manufacturing.

## Additional paths

There are many possible approaches to achieving improved cell efficiency and, hopefully, lower manufacturing costs (cost/watt), resulting in subsequent reductions in cost for the end user (levelized cost of electricity – LCOE) and in total cost of ownership for energy (TCOe). While the previously mentioned approaches, in the authors' opinions, have the best chances of impacting manufacturing during the next 12 months, there are other approaches that warrant mentioning.

### Selective emitter [7]

The advantages of a selective-emitter cell include a low contact resistance owing to heavy doping underneath the metal grid, improved front-surface passivation of the lightly doped region between the grids, and reduced recombination under the metal contact. Nevertheless, the very material that gives the p-n junction its functionality also forms a significant barrier to light in the blue part of the spectrum.

Selective emitters address this issue by varying the amount of phosphorus across the surface of the cell. The basic principle is to deposit more phosphorus directly under the metal grid to improve the contact between the metal and the silicon, allowing electrons to migrate more efficiently. Additionally, decreasing the amount of phosphorus between the grid fingers reduces recombination losses, which improves the cell's blue response.

There are a number of approaches to creating selective emitters, including doped silver paste, screen printing, selective diffusion, laser doping, etchback, doping paste etchback, buried contact and ion implant. However, the disadvantage of each of these processes is that any improvement in the blue spectrum response is attenuated by the absorption of the blue spectrum by other module components (glass and ethylene vinyl acetate – EVA). It is estimated that these materials reduce the benefit of selective emitters by 50%. Until improvements at the module level allow the full value of selective emitters to be extracted in the field, the benefit of the more costly and complex selective-emitter cell processes will be reduced.

### Heterojunction with intrinsic thin layer (HIT or HJT) [8]

In an HIT/HJT solar cell structure, an intrinsic a-Si layer followed by a p-type a-Si layer is deposited on a randomly textured n-type c-Si wafer to form a p-n heterojunction. On the other side of the c-Si, intrinsic and n-type a-Si layers are deposited to obtain a back-surface field (BSF) structure. On both sides of the doped a-Si layers, transparent conducting oxide (TCO) layers are formed, and finally metal grid electrodes are formed using a screen-printing method. By inserting the intrinsic a-Si layer, the defects on the c-Si surface can be passivated.

The HIT/HJT structure provides high performance, with the National Renewable Energy Laboratory (NREL) reporting approximately 23% efficiency. In addition, HIT/HJT cells exhibit a better temperature coefficient than conventional p-n c-Si solar cells. This technology may become more interesting now that some of the original patents have expired.

### Metal wrap-through (MWT) [9]

MWT is one of many types of back-contact technologies. In MWT cells, the front metal grids are wrapped through via holes to the rear side of the wafer, reducing shading and surface recombination losses. On MWT modules the strategy of full back interconnection of the cells results in lower cell-to-module losses by avoiding much of the resistive loss in existing double-side interconnected H-pattern solar cells. The reported efficiency improvement using MWT is 0.3%.

### Interdigitated back contact (IBC) [10]

IBC cells consist of a c-Si wafer and alternating lines (interdigitated stripes) of p-type and n-type doping. This cell architecture has the advantage that all of the electrical contacts to the p and n regions can be made on one side of the wafer. When the wafers are connected together into a module, the wiring is all done from one side. Efficiencies greater than 23% have been reported.

Another approach is to combine IBC with HIT/HJT (IBC-HJ). These cells have a very high efficiency potential of more than 24% and 25% on p-type and n-type wafers respectively. The IBC-HJ cell structure consists of a front side that is contactless and well passivated, and a back side that is formed of amorphous/crystalline silicon heterojunction contact structures.

### One to watch

One of the ways to improve overall cell performance is to retain more of the photons that hit the cell surface – easier said than done. A variety of techniques are used, often in combination, from forming random pyramids to AR coatings. A relatively new entrant is a process that involves the etching of nanopores into the silicon surface. This process results in a surface that captures a portion of the light that would normally be reflected off the usual AR

*Credit: Natcore Technology*

**Figure 2. Pyramidal texture etch (left) and the same type of wafer with a black silicon etch (right).**

coatings, including in low and diffuse light situations. Estimates are that close to 10% more photons can be harvested with fixed-angle installations. More photons reaching the device means more electrons are generated by it.

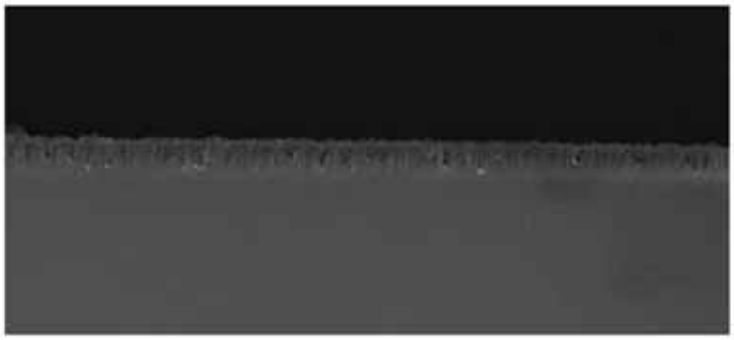
> "One of the ways to improve overall cell performance is to retain more of the photons that hit the cell surface."

Fig. 2 contrasts a commercial wafer having the standard pyramidal texture etch (left) and the same type of wafer with a black silicon etch (right). The wafer on the left still requires a silicon nitride AR layer to be added in order to reduce the reflectance from about 10% to about 5%. The wafer on the right does not need an additional AR layer to be added and has an average reflectance of about 1% or less.

Fig. 3 shows a high-magnification image of the cross section of a typical black silicon surface layer; a wet process step is used to create this layer. Fig. 4 shows a similar cross section of a black silicon layer, but one in which the pores have been filled and coated with silicon dioxide. The silicon dioxide is applied by a liquid-phase deposition (LPD) process at moderate temperatures (< 60°C).

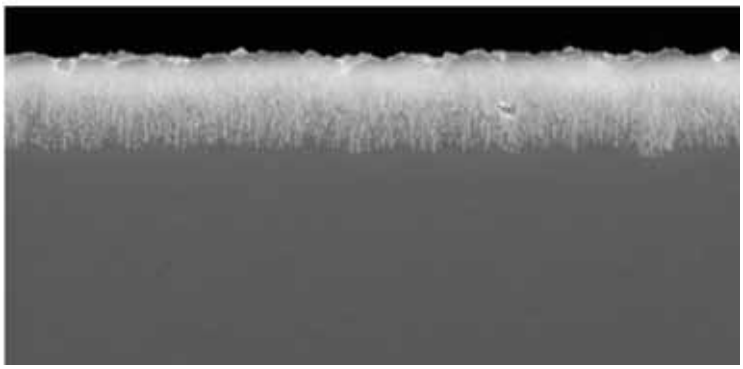
The silicon dioxide serves to passivate and protect the black silicon nanoporous structure. No further surface treatment is needed once the silicon dioxide has been deposited, and the wafer is ready for the usual screen-printed contact formation step of the cell line. The black silicon process is performed on a single wet station and eliminates the silicon nitride deposition step.

The step obviously incurs a cost, so the question is: how can this process be integrated in a manner that makes it cost effective? Fortunately, this is in part a replacement step; so, in order to be cost effective, it needs to be cost and value competitive relative to existing techniques. The combination of the nanopore creation and the deposition of a liquid phase oxide appears to be capable of being integrated into a single tool. The cost of the processes it may replace is thought to be approximately 10–12 cents per cell. Preliminary COO studies, including one discussed later in this paper, have been performed for a black silicon process: the new process is competitive at 12 cents, which translates (with rounding errors) to about $1 per conventional panel. If you can sell that panel for $1 more, then you have broken even. Even today, that is a relatively modest premium to pay given the added light captured by the process.



Credit: Natcore Technology

**Figure 3. High-magnification image of the cross section of a typical black silicon surface layer.**



Credit: Natcore Technology

**Figure 4. LPD-process coated black silicon surface.**

## Case study

Our 'one to watch' process is nanopore formation using Natcore Technology's black silicon process as an example. In order for nanopore formation to be something worth adopting in the near future, not only does it need to pass the technical requirements, but it must also offer a business objective of high payback. This objective will be explored through a preliminary COO analysis.

### COO review [11]

A more detailed discussion of COO can be found in the first paper in this series [2]. To review, the basic COO algorithm is described by:

$$C_U = \frac{C_F + C_V + C_Y}{L \times TPT \times Y_C \times U} \quad (1)$$

where

$C_U$ = cost per good unit (wafer, cell, module, etc.)
$C_F$ = fixed cost
$C_V$ = variable cost
$C_Y$ = cost due to yield loss
$L$ = process life
$TPT$ = throughput
$Y_C$ = composite yield
$U$ = utilization

### Overall equipment efficiency (OEE) review [12]

One of the most popular productivity metrics is OEE. It is based on reliability (mean time between failures – MTBF), maintainability (mean time to repair – MTTR), throughput, utilization and yield. All these factors are grouped into the following four sub-metrics of OEE:

1. Availability (joint measure of reliability and maintainability)
2. Operational efficiency
3. Throughput rate efficiency
4. Yield/quality rate

As seen in the above list, many parameters are required in order to

$$\text{OEE} = \frac{\text{Number of good units output in a specified period of time}}{\text{Theoretical throughput rate} \times \text{Time period}}$$

**Equation 2.**

| Parameter | Value |
|---|---|
| Throughput | 1300 wafers/hr |
| Wafer size | 156mm |
| Process lifetime | 7 years |
| MTBF | 200 hours |
| MTTR | 10 hours |
| Equipment cost | $2 million |
| Equipment yield | 99.90% |
| Utilities (lifetime) | ~$1.3 million |
| Consumables (lifetime) | ~$2.4 million |
| Maintenance (lifetime) | ~$1.6 million |

**Table 1. Major COO inputs.**

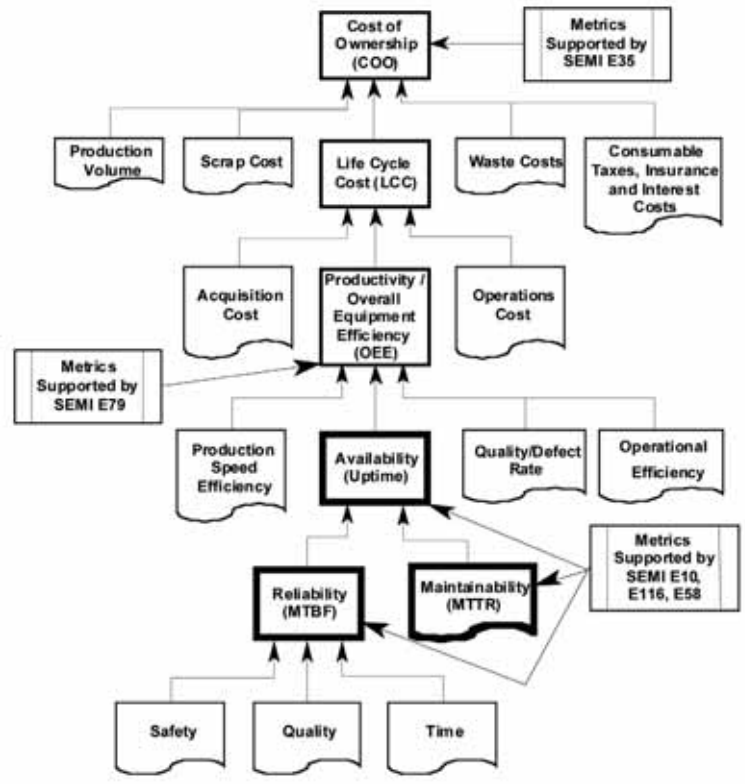



**Figure 5. Hierarchy of equipment performance metrics [13].**

calculate OEE. If the accuracy requirement is not a critical factor, the formula given in Equation 2 can be used to calculate an approximate OEE value.

### Relationship between metrics

There are many equipment performance metrics at different levels. Although they may appear disjointed, this is not the case – they all fit nicely into a hierarchical tree. Fig. 5 depicts the hierarchical tree of the equipment performance metrics. As shown in the figure, when a time dimension is added to quality and safety, it becomes 'reliability'. Reliability and maintainability jointly make up 'availability.' When production speed efficiency, operational efficiency and production defect rate are combined with availability, it becomes 'productivity' (OEE). Acquisition and operational costs, along with productivity, make up 'life cycle cost' (LCC). When scrap, waste, consumable taxes, insurance and interest costs are added to LCC, and the total is normalized by the production volume, it becomes 'cost of ownership' (COO).

| | |
|---|---|
| Cost per system | $2,000,000 |
| Number of systems required | 1 |
| Total depreciable costs | $2,225,000 |
| Equipment utilization capability | 90.99% |
| Production utilization capability | 90.99% |
| Composite yield | 99.90% |
| Good wafer equivalents out per week | 198,526.93 |
| Good wafer equivalent cost | |
| With scrap | $0.12 |
| Without scrap | $0.12 |
| Average monthly cost | |
| With scrap | $104,919 |
| Without scrap | $103,883 |
| Process scrap allocation | |
| Equipment yield | 100.00% |
| Defect limited yield | 0.00% |
| Parametric limited yield | 0.00% |
| Equipment costs (over life of equipment) | $2,385,041 |
| Per good wafer equivalent | $0.03 |
| Per good $cm^2$ out | $0.0002 |
| Recurring costs (over life of equipment) | $6,428,164 |
| Per good wafer equivalent | $0.09 |
| Per good $cm^2$ out | $0.0005 |
| Total costs (over life of equipment) | $8,813,205 |
| **Per good wafer equivalent (cost of ownership)** | **$0.12** |
| Per good wafer equivalent supported | $0.12 |
| Per good $cm^2$ out | $0.0007 |
| Per productive minute | $2.63 |

**Table 2. COO results.**

### Cost of ownership inputs

This section presents the results of the COO analysis run on the black silicon process. Table 1 highlights the major input parameters.

In addition to the Table 1 parameters, the authors used, where required, example values from SEMI E35 [11] for administrative rates and overhead. These values were provided by SEMI North American members and may not be applicable to other geographic regions. However, it is the authors' experience that these example values do not impact the COO results on a relative basis.

### Cost drivers

Examination of the detailed TWO COOL COO model [14] in Table 2 highlights the main cost and productivity factors. Recurring costs are approximately three times the initial capital costs over the life

| Cost drivers per good wafer equivalent | |
|---|---|
| Material/consumables | $0.050 |
| Depreciation | $0.031 |
| Maintenance | $0.022 |
| Labour | $0.014 |
| Floor space costs | $0.002 |
| Support personnel | $0.001 |
| Scrap | $0.001 |
| Training | $0.000 |
| System qualification costs | $0.000 |
| Other materials | $0.000 |
| ESH preparation and permits | $0.000 |
| Moves and rearrangements | $0.000 |
| Other support services | $0.000 |

**Table 3. Pareto of cost drivers.**

| Supply/ Consumable | Annual cost per system |
|---|---|
| Material 1 | $103,567 |
| Material 2 | $79,208 |
| Material 3 | $54,947 |
| Material 4 | $37,148 |

**Table 4. Annual supply/consumable costs.**

of the process and are driven primarily by the cost of consumables. Next, the top cost drivers and opportunities for improvement will be looked at more closely.

> "The top Pareto costs are materials/consumables, depreciation and maintenance."

Table 3 takes a closer look at the cost breakdown according to the 13 categories specified in SEMI E35. The top Pareto costs are: materials/consumables, which include utilities, supplies, consumables and waste disposal; depreciation, which is impacted by equipment costs, throughput rate and utilization; and maintenance, including repair parts and technician labour.

The top two cost drivers account for two-thirds of the total COO. For this reason, attention will be focused on those areas when the cost sensitivities to input parameters that drive material/consumable and depreciation costs are examined.

**Cost driver sensitivities**

The first factors to be examined are supplies and consumables. Table 4 shows the annual costs per system by supply item. One of the issues in defining a sensitivity analysis for these items is their potential interrelationship with other factors. Changing the price/quality of the consumables could impact throughput,

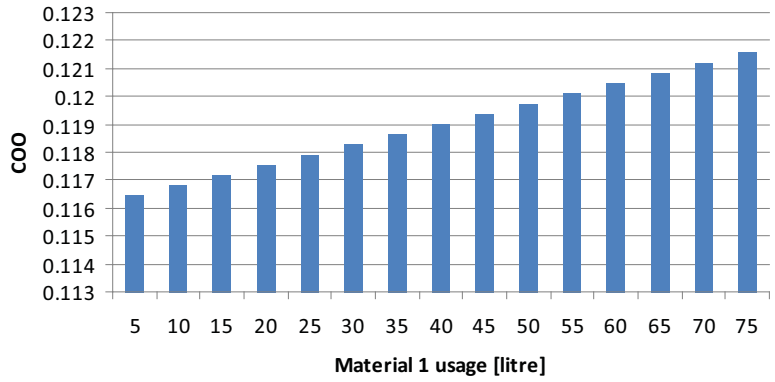



**Figure 6. Sensitivity analysis of Material 1 quantity vs. COO.**

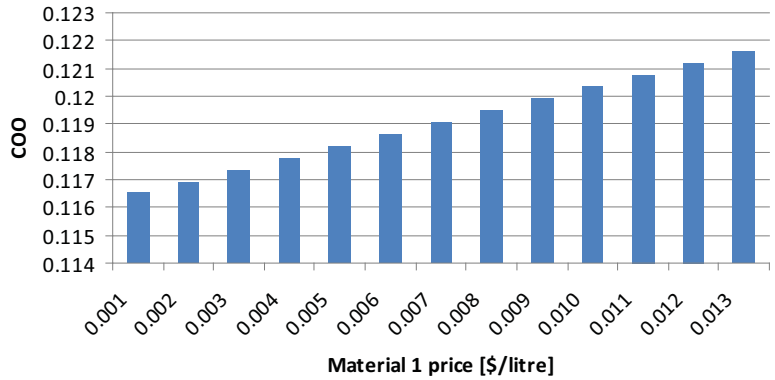



**Figure 7. Sensitivity analysis of Material 1 price vs. COO.**

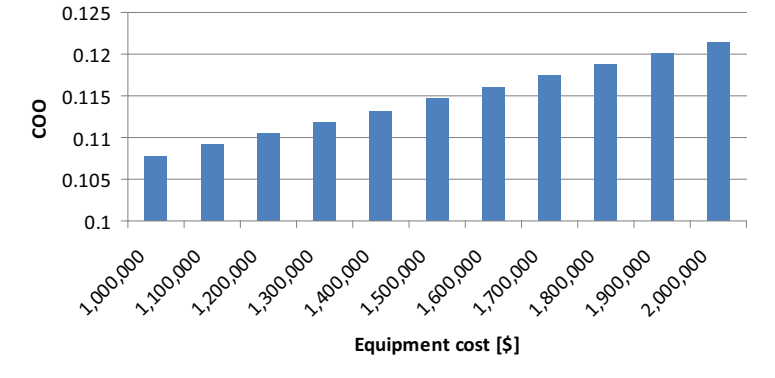



**Figure 8. Sensitivity analysis of purchase price vs. COO.**

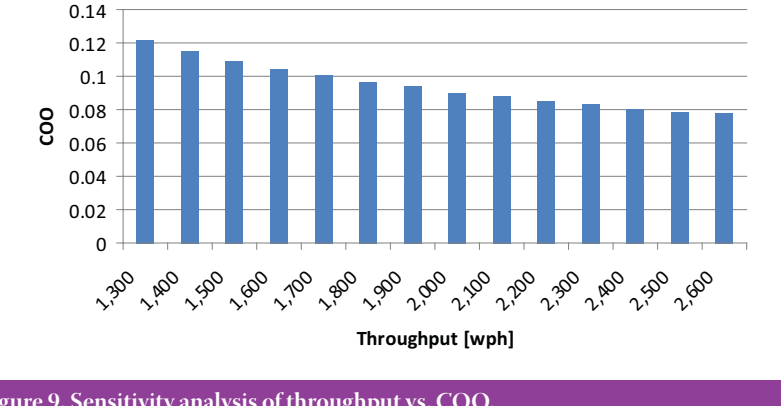



**Figure 9. Sensitivity analysis of throughput vs. COO.**

| | |
|---|---|
| Overall equipment efficiency | 90.90% |
| Availability efficiency | 90.99% |
| Engineering usage | 0.00 hr/week |
| Standby | 0.00 hr/week |
| Hours available/system (productive time) | 152.87 hr/week |
| Downtime | 15.13 hr/week |
| Scheduled maintenance | 7.00 hr/week |
| Unscheduled maintenance | 7.92 hr/week |
| Test | 0.00 hr/week |
| Assist | 0.21 hr/week |
| Non-scheduled time | 0.00 hr/week |
| Equipment uptime | 152.87 hr/week |
| Total time | 168.00 hr/week |
| Performance efficiency | 100.00% |
| Throughput at capacity/system | 1300.00 wafers/hr |
| Theoretical throughput | 1300.00 wafers/hr |
| Operational efficiency | 100.00% |
| Rate efficiency | 100.00% |
| Quality efficiency | 99.90% |
| Equipment yield | 99.90% |
| Defect-limited yield | 100.00% |
| Parametric-limited yield | 100.00% |
| Alpha error factor | 100.00% |
| Beta error factor | 100.00% |
| Redo rate | 0.00% |

**Table 5. OEE results.**

consumption or yield; consumption changes could impact throughput and the conversion efficiency of the device. The cost benefits that could be achieved by reducing the consumption or cost per litre of Material 1 will be examined.

As can be seen from Fig. 6, the usage of Material 1 has a low impact on the total COO. This sensitivity analysis is based on one tank using Material 1; however, there are two tanks that use the majority of this material. Thus, a 50% reduction in usage provides approximately a 6% reduction in the total COO for the process. While it may not be possible to achieve this level of reduction and maintain process control, it certainly presents an opportunity for cost reduction.

Likewise, the price of Material 1 has a similar impact on the total COO (Fig. 7): a 50% reduction in price provides an approximate 6% reduction in the total COO for the process. It should be noted that the reason Material 1 has a low impact on COO is that there are several consumables used in the process and Material 1 represents only about one-third of those costs.

The factors impacting depreciation, purchase price and throughput will be discussed next. Purchase price has a moderate impact on COO in high-throughput tools, especially those with higher variable costs (Fig. 8). The cost impact in this case is approximately 1.2% per $100,000 (5%) change in purchase price.

On the other hand, as can be seen in Fig. 9, improvements in throughput can have a significant impact on COO, depending on whereabouts on the curve the equipment is operating. In this case, the equipment is operating at an average throughput of 1300 wafers/hour (wph), and an improvement of 100wph near the average has a greater than 5% impact on COO.

### Overall equipment efficiency

Table 5 shows the OEE of the black silicon process step: as can be seen, on the basis of a maximum throughput rate of 1300wph, the OEE is in excess of 90%. One hundred per cent of the OEE losses in this model are attributed to availability efficiency primarily associated with equipment downtime (scheduled and unscheduled). Since this is a preliminary analysis of the process, the values of OEE and COO should be taken as potential opportunities only.

## Conclusions

The PV industry is in a challenging phase. The overcapacity issues are exacerbated by changing government policies and increased competition external to the PV industry. Solar cell providers who do not evolve will get eaten alive. As counterintuitive as it might seem in a period when money is tight, companies need to spend money. They must invest in newer, higher-value technologies and lower-cost processes. It is not a choice.

An attempt has been made to pick the investment options that the authors see as having the largest paybacks in the near term. In each case, these options differentiate themselves from baseline processes by improving costs or adding value to the product – in some cases, both.

Continuous improvement has been the norm for solar research and development; it has been more challenging in fixed production lines. But as factories get larger and the scale increases, it becomes apparent that this continuous improvement will require a near-constant evolution within manufacturing operations.

> "Ultimately, tools like COO and factory-level cost modelling will be essential in determining product roadmaps."

The uncertainty this brings in difficult business conditions is not appealing. It does, however, argue for a well thought out, disciplined process regarding the choices to be made. The roadmaps that companies pursue need to be carefully evaluated for the best business decision – which may well differ from the most 'talked-about' technology. Ultimately, tools like COO and factory-level cost modelling will be essential in determining product roadmaps – integrating these methods into both short- and long-term decision processes may prove to be the difference between the companies that do not survive and those that thrive.

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