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PV manufacturing materials: Technological and process-related options for cost reduction

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ABSTRACT

The PV industry is undergoing dramatic changes. Like a carnival ride gone dreadfully wrong, exhilaration has been supplanted by dread; joy has been replaced by fear. Just look around you – provided you are able to turn your head to defy the g-forces acting upon you as we bank and turn wildly along. You will see PV companies closing their doors for good. You will see extraordinarily talented people throughout the supply chain, shifting positions everywhere and looking for safe-haven jobs. And you will also see once-leading PV companies burning cash and losing their status as 'bankable'. Everywhere we turn, we see companies in the supply chain shuttering production as if to balance markets. Then it happens again. Another wheel comes off the roller coaster. While we all want this reckless ride to end safely, optimism that was once universal has been replaced by threats of bankruptcy, failing policy support and a looming trade war. Indeed, it is hard not to be concerned about what lies ahead. However, despite all the neck-snapping gyrations, there remain three keys to surviving and prospering in the long run. The first is cost reduction: now, more than ever, the industry must reduce the cost of everything, from upstream to downstream, in order to bridge the gap to grid parity. The second key is quality: there is nothing more harmful to the industry's potential than cutting corners and sacrificing quality. And, finally, there is the third key – profitable volume. A degree of cost reduction for the industry that delivers on these three key mandates of cost, quality and profitability will be discussed in this paper by taking a fresh look at which processes, as well as which technologies, show the most promise.

Global demand-supply dynamics

According to most estimates, demand surprisingly grew in 2011. This growth came in spite of subsidy cuts, less financing and Europe's sovereign debt crisis. As there are only a few countries reporting official installation numbers for 2011 thus far, AEI maintains that the global market for installations was 21.5GW and 23.8GW (Fig. 1), a maximum increase of approximately 20% from 2010. Yet another year-end rush, or 'pull-in', seems to have created even more disagreement than is usually the case among estimators with some full-year estimations in excess of 28GW, expressed after German officials registered a whopping 3GW of installations in December alone. With growth estimates for 2011 ranging from 'up to 20%' to 'over 40%', it would seem that the industry should be doing quite well, but that is not the case. Perhaps an estimator is off the mark, ourselves included – or is something else going on here?

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There is, however, one issue without much debate. Prices and profits for everything throughout the supply chain fell dramatically, and the fallout has resulted in an industry-wide requirement for everyone to reset their business models at this new lower level. While some of this need is taken up through supply-chain price discounting, the remainder must come from the adoption of processes that support production and result in restoring profits. Not an easy task given that pricing for everything moves so much and with very little warning, and often down as it has in the last three years.

The widening gap between supply and demand seems to have at last set

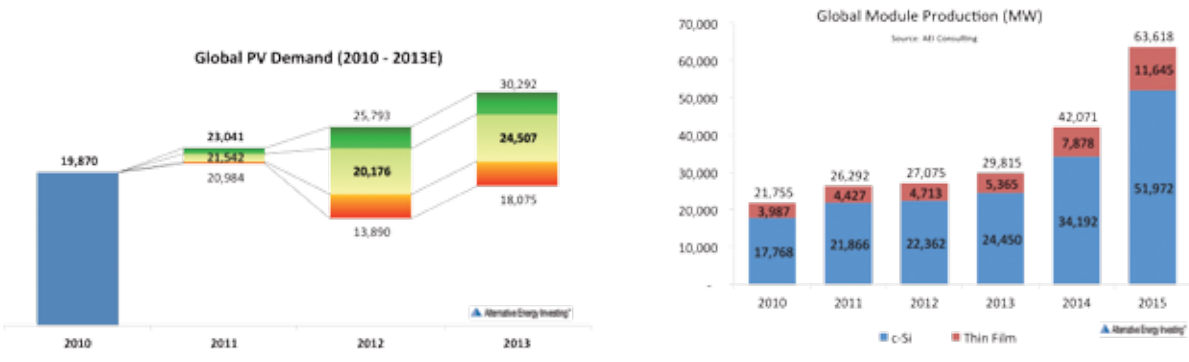


Figure 1. Global PV module supply and demand scenarios. The demand chart (left) illustrates the estimated outcomes corresponding to a 'worst-case', 'base-case' and 'best-case' scenario. This chart and the production chart (right) together characterize the supply/demand situation.

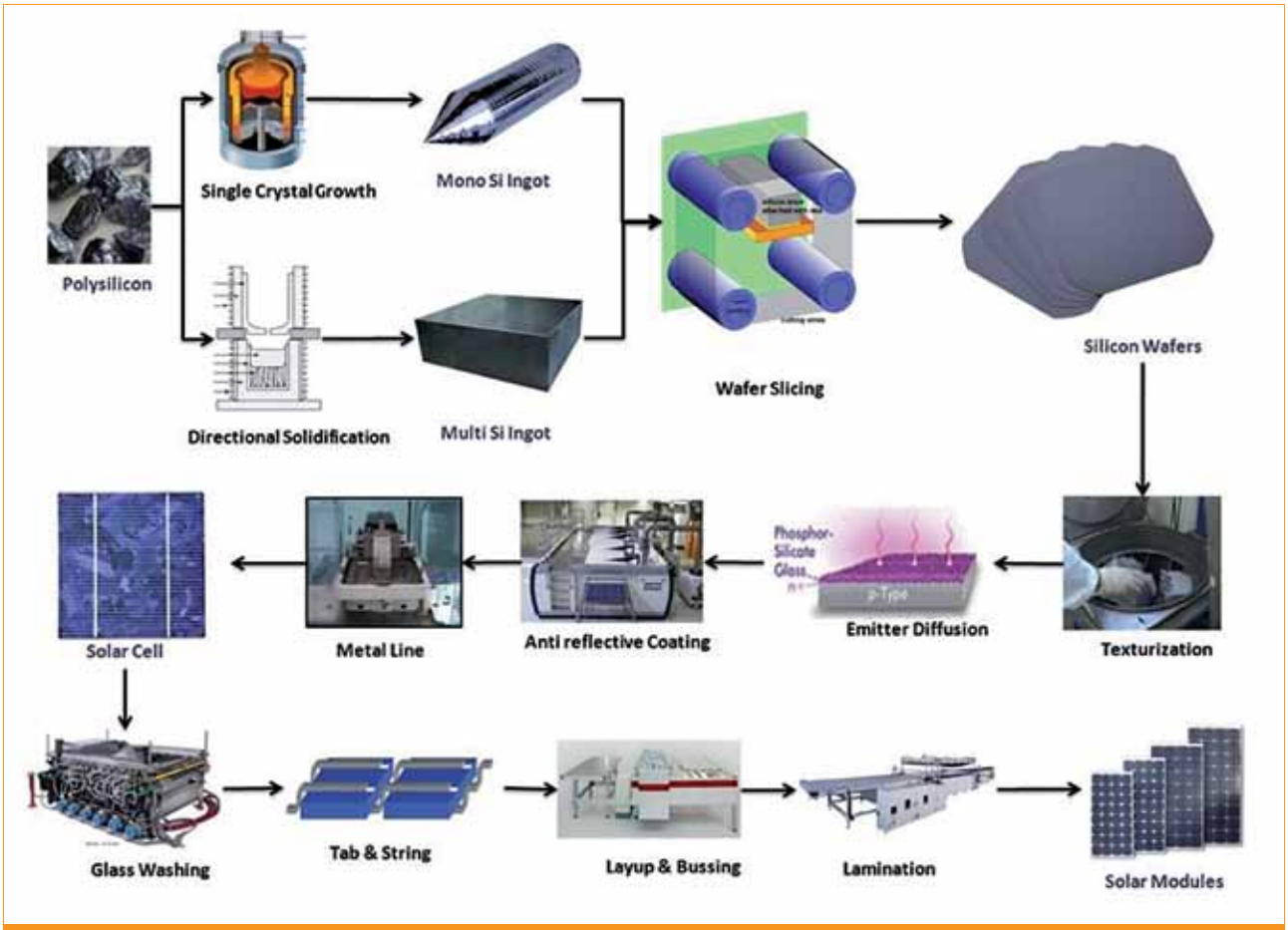


Figure 2. The standard crystalline silicon module manufacturing process sequence.

an expectation in the marketplace that average selling prices of modules will continue to fall. In 2011 alone we witnessed a 25% drop in the average selling prices (ASPs) of multicrystalline silicon (mc-Si) modules from Tier 1 Chinese companies. With prices hovering near $1/Wp, the ever-constant pressure to drive out costs reached the breaking point for practically every monocrystalline silicon (c-Si) module company except the Tier 1 cohort in China. Alas, to retain margins, and indeed hang on to their own survival, SolarWorld and others allege that Chinese module makers are dumping and a trade war looms. Given this as a backdrop, the key technological developments happening across the c-Si PV value chain will be reviewed, and areas for cost reduction with the potential for a 43% reduction in the medium term will be identified. Combined with falling polysilicon prices seen in the market today, total cost reductions for the industry may exceed 60% in the near term.

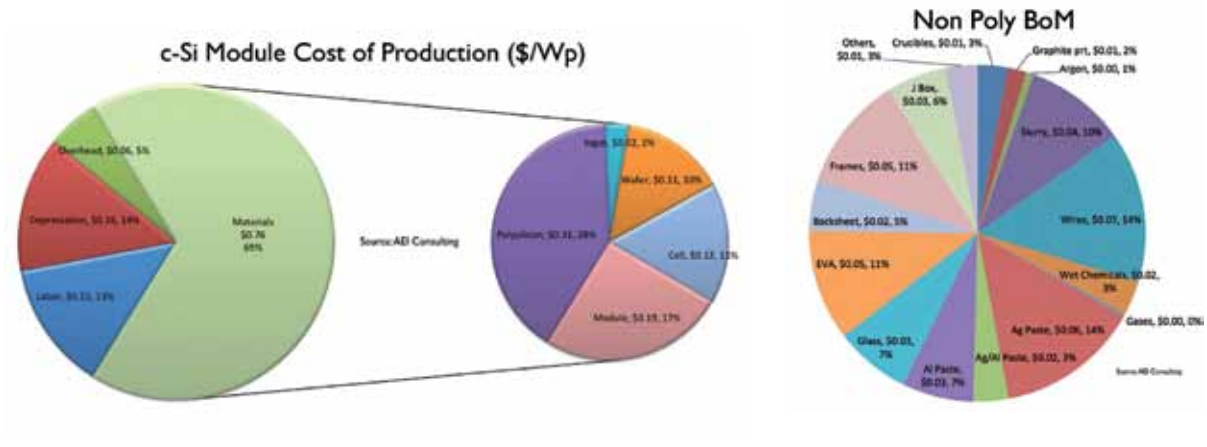
Whether installations grew at the high end or the low end of the range, the whopping growth of 200%+ during 2010 is over and we now face a slowdown in global demand growth, largely attributable to subsidy cuts in key regions – Germany, Italy and Spain – and persistent negative macroeconomic factors. Supply, on the other hand, for everything has continued to increase in the face of crippling news on the demand front. If announced capacities are adjusted to account for ramp-up delays and misinformation, etc., then it is still possible to arrive at a base level of module production of 26.3GW in 2011, 27.1GW in 2012 and 29.8GW in 2013, should companies proceed on their expansion plans. However, since supply continues to greatly exceed demand, more reductions in module prices are to be expected in the near future.

c-Si PV standard manufacturing process

The crystalline silicon module production process starts from polysilicon raw material. A PV module can be manufactured from the more costly and more efficient c-Si or from the less expensive but less efficient mc-Si. A c-Si ingot is manufactured using Czochralski (CZ) or float zone (FZ) processes, whereas an mc-Si ingot is manufactured using directional solidification (DSS). Processing a wafer from ingots and bricks requires slicing, which is done with wire saws using wires of up to 400km in length. The real cutting work is carried out by what is known as slurry – a mixture of oil and silicon carbide grains – while the wire is wound on guides that form a horizontal 'web' of up to 1000 wires in parallel. Motors rotate the wire guides, causing the entire web to move at a speed of 5 to 25 metres per second. The wire speed and the back-and-forth motion are adjusted throughout the cut as nozzles continuously spray the wires with slurry. The silicon blocks are mounted to cutting tables, which then travel vertically through the web, cutting blocks into wafers. The wafers are then processed into cells.

Through a series of chemical and physical stages, wafers are processed to make them sensitive to solar radiation and absorb photons of light, which then creates free electrons within a newly made solar cell. Since cutting silicon into wafers leaves the surface of the wafer covered with cutting slurry and damaged due to the action of the saw, the wafers are cleaned in a hot solution of sodium hydroxide that removes the surface contamination and the first 10µm of damaged silicon. The wafers are then textured in a more dilute solution of sodium hydroxide with isopropanol as a wetting agent.

The p-n (positive-negative) junction is finally created by exposing the wafer to heat in a thermal diffusion step in a high-temperature oven (about 1000°C) with a controlled and highly purified atmosphere. During this process, the first 0.5µm of the wafer is doped with phosphorous, turning its conductivity into n-type and thus creating a p-n junction. The rest of the wafer maintains



Source: AEI Consulting

Figure 3. c-Si module manufacturing cost.

a p-type conductivity, which acts as a separator for the electric charges created by the photons absorbed into the cell.

A very thin anti-reflecting coating (60–80nm) of silicon nitride (SiN_x) is applied through a plasma-enhanced chemical vapour deposition (PECVD) step to further reduce reflection and maximize the cell's light-absorption characteristics. Finally, electrodes are formed by printing silver paste grid lines on the front and aluminium paste on the back by means of a screen-printing process.

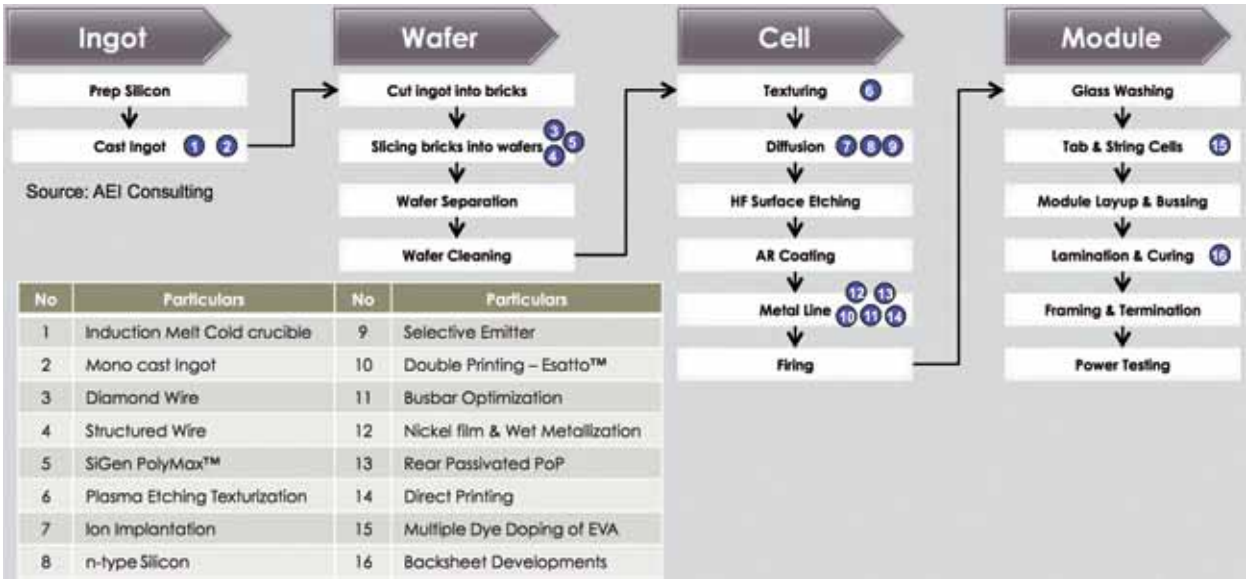
Once the solar cells are ready, individual cells are interconnected and laminated into a module. In this basic process, first using ribbon wire, individual cells are electrically connected into a solar cell string. The strings are then placed onto the glass panel and interconnected with bus ribbon, and encapsulated in EVA and a backsheet before aluminium frames are arranged around the laminated module stack. As a final step, junction boxes are put in place and final tests carried out.

> "Given the cost of materials to make a module, the industry is lowering the key cost contributors and has identified potential areas of cost-reduction across the value chain."

In 2011 around 75% of silicon PV modules were made from multicrystalline silicon and the balance of 25% from monocrystalline silicon. The average cell efficiency for multi was 14.85%, while for mono it was 15.15%; the market-weighted average cell efficiency was therefore approximately 14.93%. The average wafer thickness in 2011 is estimated to have remained in a variable range of 180–200µm. Polysilicon consumption was 6.16g/W and the average price of polysilicon was $50/kg for the year. With these assumptions, the average cost of manufacturing a module is estimated to be $1.12/W, with the total cost approximately split up into 66% materials, 13% labour, 14% depreciation and 5% overheads. The biggest factor in the cost of materials is of course polysilicon, which accounts for approximately 28%. Non-polysilicon costs were approximately $0.45/W. Of these, slurry (10%), sawing wires (14%), metallic pastes (24%), EVA/PVB (11%), frames (11%), and glass (7%) were the bulk contributors. Given the cost of materials to make a module, the industry is lowering the key cost contributors (polysilicon, sawing wires, metallic pastes, etc.) and has identified potential areas of cost-reduction across the value chain.

Cost reduction areas for PV materials and consumables

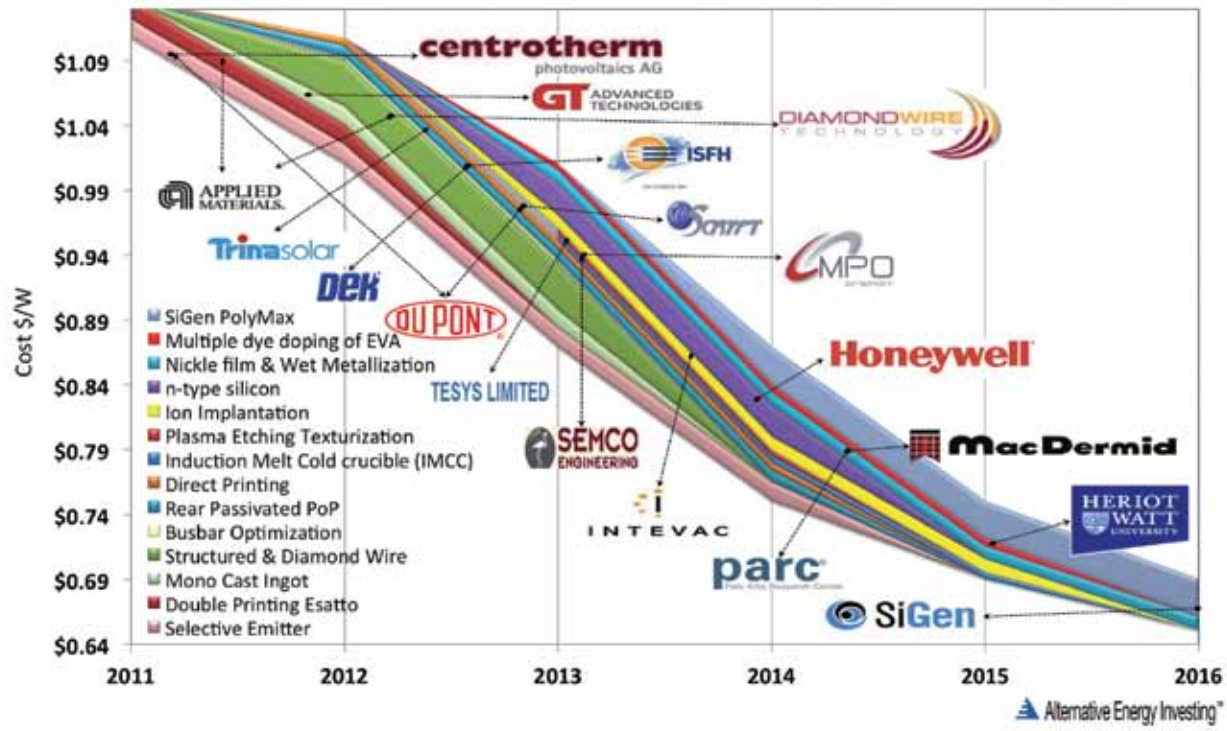
While there are numerous ways in which costs of materials and consumables throughout the c-Si supply chain can be reduced, there are several key focus areas



No	Particulars	No	Particulars
1	Induction Melt Cold crucible	9	Selective Emitter
2	Mono cast Ingot	10	Double Printing – Esatto™
3	Diamond Wire	11	Busbar Optimization
4	Structured Wire	12	Nickel film & Wet Metallization
5	SiGen PolyMax™	13	Rear Passivated PoP
6	Plasma Etching Texturization	14	Direct Printing
7	Ion Implantation	15	Multiple Dye Doping of EVA
8	n-type Silicon	16	Backsheet Developments

Source: AEI Consulting

Figure 4. Identified potential areas for cost reduction.



Source: AEI Consulting

Figure 5. Cost reduction potential.

for achieving this goal. Of these, the most critical are in the fields of improved wafer slicing, replacement of p-type silicon with n-type structures, and optimized metallization to reduce costly silver paste.

Given the current standard module manufacturing process, slurry and sawing wire together account for approximately a quarter of non-silicon material cost. Kerf loss associated with this process remains a big problem. Over the next two years, a sizable cost saving occurring in these areas alone through the replacement of conventional steel wires with structured and diamond wires should deliver a large part of the cost reduction. Beyond 2015, the sawing process itself may be replaced by novel and disruptive kerf-less wafering techniques that promise wafer thicknesses of 20µm, nearly a tenth of what can be achieved today on commercial production lines.

The replacement of p-type silicon with n-type silicon has been slowly gaining in importance because of the benefits of increased carrier lifetime and bulk resistivity, which lead to meaningful increases in cell efficiency. Process improvements and the introduction of innovative printable dopants are paving the way for potentially manufacturing n-type cells industrially on a large scale, a development which should contribute significantly to cost reduction in the coming years.

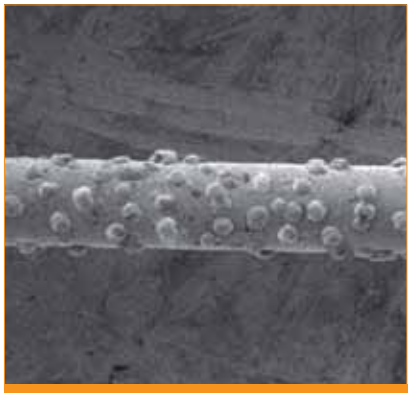
Metallic pastes account for approximately 24% of non-silicon material cost. Optimizing the screen-printing process is therefore critical to the overall cost-out equation. Techniques such as double printing, optimizing the busbar design, direct-printing technology, nickel film contact layers and so on are currently being used and tested or examined. These processes hold the potential for lowering costs by more than a third by 2016. Some of these process improvements are more popular and are being deployed much faster, which may result in accelerated cost reduction, depending on implementation and technology adoption. As noted, the standard manufacturing cost is currently $1.12/W, but it will be shown that this cost may drop to $0.64/W by 2016, given the adoption of improved technologies. Falling polysilicon prices may reduce costs for the industry beyond just those initiatives covered here. Assuming a $20/kg polysilicon price, with an average silicon usage of 5.01g/W by 2016 and a one percentage point increase in cell efficiency, the silicon cost could be $0.10/W, or 68% of the current level of $0.31/W. The combined effect of technological development and silicon price reduction may result in module manufacturing costs falling from $1.12/W to $0.43/W by 2016 – a 62% reduction from the current level.

Diamond wire (3)

Diamond wire is intended to replace the conventional multiple-wire slurry saw (MWSS) of today; however, the process remains very expensive. The wire is coated with diamond particles and these particles become the abrasive element instead of the SiC particles found in today's conventional sawing technology. Diamond wires have very high cutting speeds (2–5× the speed of MWSS): certain companies – such as Read Co., Ltd., Japan – claim that their diamond wire cuts 5× faster than slurry-based steel wire. This obviously results in higher productivity, lower wire usage and ultimately a lower cost of ownership (CoO) as stated by the value proposition. Since diamond wires use fixed diamond grit, no slurry (SiC and PEG) is required and therefore this cost is avoided. Diamond wires also have very high tension strength and can be reused for several cuts, which obviously means less wire usage.

Meyer Burger has demonstrated wire consumption of under 3m/wafer (for 156mm wafers) on their DS265 sawing machine. But, as previously noted, diamond wire remains too expensive and, with the cost in the range of $375/km to $450/km (e.g. Read is selling at $400/km FoB Japan) and MWSS prices of $1–2/km, it is likely that we must wait for the cost of this technology to fall before it can contribute to the cost-out mandate of the industry. In 2011, the average MWSS cost $1.28/km and required 185m per 156mm wafer. The cost of slurry was $0.16 per wafer, and depreciation approximately $0.12 per wafer. Therefore, MWSS total CoO works out to be approximately $0.512 per wafer.

Diamond wire's high speed and tension strength means a usage of between 1 and 3m per wafer. Higher productivity and lower depreciation cost are calculated to be approximately $0.03/W, and there is



Source: Applied Materials

Figure 6. Diamond wire.

no slurry cost. Presuming a price of $250/km for diamond wire, the CoO works out to be approximately $0.32 per wafer. This implies that replacing MWSS with diamond wire could result in a net benefit of $0.19/wafer. Assuming market weighted average cell efficiency of 14.93%, this implies a net benefit of $0.05/W. A nickel does not purchase very much anymore, but in PV a nickel becomes disproportionally large as the cost per watt for modules falls below $1.

Structured wire (4)

Today's state-of-the-art technology for c-Si wafering is based on the multi-wire saw method using abrasive grains as the cutting agent, suspended and transported in a liquid media ('slurry') as mentioned previously. The productivity and quality of the wafer slicing process essentially relies on the capability to transport slurry into the cutting channel. Applied Materials has developed a new process of using ultrathin, 120µm-diameter structured wire for slicing. This structured wire is a metal saw wire with a plurality of crimps or waves alternately oriented in two orthogonal planes. The idea here is to increase productivity by the more efficient transport of the slurry and by faster cutting speeds.

Applied Materials has demonstrated that structured wire can result in a 25–35% improvement in productivity over conventional MWSS. If structured wire results in 30% more productivity over MWSS, the wire use falls from approximately 0.185km/wafer to 0.142km/wafer, or a 23% reduction in wire consumption. Assuming structured wire costs 10% more than conventional MWSS, there is a net cost saving of $0.06/wafer. Again, assuming a market-weighted average cell efficiency of 14.93%, this implies a net benefit of $0.02/W.

SiGen PolyMax kerf-less wafering (ion-beam-induced cleaving) (5)

Kerf-less silicon wafer-making equipment has been suggested as the cost-effective alternative to the wire saw method. The potential benefits include greater efficiency of materials utilization and lower cost. However, it seems that commercial efforts have been abandoned because of the poor electrical quality of kerf-less wafers and the method's inability to compete with the steadily improving performance of wire-saw-based wafering. To become competitive and gain traction against modern wire-saw-based wafering, the kerf-less method must support sub-100µm thicknesses and produce wafers possessing good electrical quality and mechanical strength.

SiGen is developing an ion-beam-induced cleaving technique that seems to hold some promise. This company is developing a novel technology called PolyMax, a potentially disruptive new capability for wafer generation by cleaving the wafers, in contrast to the destructive wire sawing process. In PolyMax technology, electron beam injections of H ions are used to peel the wafer from the silicon ingot without generating silicon losses. Gluing, wafer cutting, wafer separation and wafer cleaning process steps are also eliminated. This technology offers wafer thicknesses of as little as 20µm as against today's standard of ~180–200µm. Currently, the standard process consumes silicon at the rate of approximately 6.16g/W. Assuming a silicon price of $50 per kg, the silicon cost is $0.31/W. In comparison, if PolyMax is successful, with the potential for initially reducing the wafer thickness to 120µm, the silicon usage rate will drop to 3.70g/W, resulting in silicon costs decreasing from $0.31/W to $0.18/W.

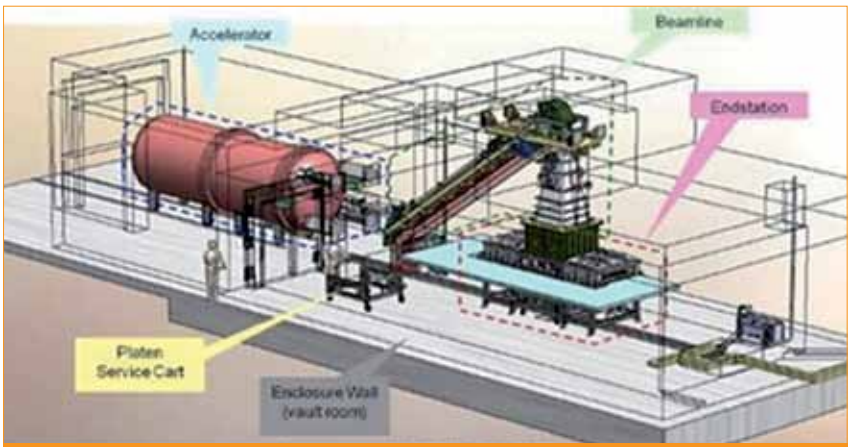
Again, the wire saw technique involves a cost of around $0.13/W in respect of crucibles, graphite parts, saw wires and slurry, which can be completely avoided by switching to PolyMax technology. However, PolyMax could involve higher upfront capital which, it is estimated, may entail $0.17/W higher depreciation charges. However, on the whole, switching to PolyMax brings to the table a net benefit of $0.09/W initially and potentially $0.23/W later on, once wafer thicknesses gradually slim down to 30µm as the technology matures further. As one can see, kerf-less process technology is a huge contributor to the industry's overall cost reduction programme.

n-type silicon (8)

Silicon is the most commonly used material in the production of solar cells. It is a non-conducting material, meaning that it does not conduct electrical current because it has wide energy bandgap. During material preparation, a dopant is introduced homogeneously into the silicon lattice to make it electrically semiconducting; in other words, it conducts electricity in only one direction, according to the type of dopant added. The most common dopants are phosphorous and boron. When a silicon lattice is doped with phosphorus, the electrical conduction is dominated by electrons and is called 'n-type'. Boron-doped silicon, on the other hand, is dominated by holes and is called 'p-type.' During cell fabrication, the electrical junction is formed by the thermal diffusion of oppositely charged impurities. For example, a junction is formed on the p-type substrate by phosphorous diffusion. The junction provides a built-in voltage that separates electron-hole pairs that flow through an external circuit.

Today most solar cells (whether mono or multi) are made from p-type (boron-doped) substrate on which phosphorous is diffused. There has been growing interest in developing a low-cost industrial cell manufacturing process based on n-type substrates. It has been successfully demonstrated that the use of n-type substrates could increase the minority carrier lifetime and bulk resistivity of devices, resulting in higher cell efficiency. Several studies have confirmed that efficiency improvements of 1–2% can be achieved by using n-type silicon instead of p-type standard silicon. Unfortunately, industrial manufacturing of n-type cells based on conventional architecture costs more than for conventional p-type silicon solar cells.

The process of manufacturing n-type cells usually involves two diffusion steps, including (for example) BBr_3 diffusion



Source: SiGen

Figure 7. SiGen PolyMax ion-beam implanter tool.

for top emitter formation, and $POCl_3$ diffusion for back-surface field (BSF) formation. In addition to the associated equipment depreciation, energy costs and safety concerns involved in handling BBr_3 in volume manufacturing, the added thermal budget seems to put limits on the use of this process for creating very high quality Si substrates. Honeywell presented an approach using a co-diffusion of boron emitter and phosphorus BSF using printable dopants. These dopants can be applied by various techniques, including inkjet printing and screen printing. Under diffusion conditions of 60 minutes at 925°C, the new technique has been able to achieve a sheet resistance (R_s) below 60Ω/sq for a boron emitter, with good doping uniformity over the entire wafer.

It is estimated that replacing p-type silicon with n-type silicon could result in a 1–2% absolute efficiency gain. However, with BBr_3 diffusion, this could involve higher material cost and could involve higher capex due to the extra process steps involved. On the whole, it is estimated that switching to n-type could result in a net benefit of between $0.05/W and $0.06/W.

Selective emitter (9)

Energy conversion in a silicon solar cell happens at its p-n junction, which is normally formed by firing the wafer in a phosphorus-rich atmosphere. The phosphorus diffuses into the upper zone of the wafer to form a layer that is uniform and planar, lies a few hundred nanometres under the surface, and extends across the wafer's entire area. This process is called 'emitter diffusion.' In this layer, photons of sunlight release electrons that migrate through the silicon to the cell's front face, where they are captured by the grid of silver conductor fingers printed on the cell's top side. The flow of electrons through this grid is the electrical current that constitutes the cell's power. These electrons then flow around the circuit back to the aluminium contact on the reverse side of the cell, where they once again join with atoms that are missing electrons (i.e. possess 'holes').

However, the top part of the cell where the phosphorus is most concentrated is essentially a 'dead layer' that reduces the cell's blue response. In other words, the electrons activated by blue light turn into charge carriers, but then, even before they leave the silver conductor grids, they recombine with the wafer's surface, generating heat rather than current. In order to resolve this problem it is desirable to deposit more phosphorus under the silver grid and less phosphorus between the grid fingers. This can be done through 'selective emitter' (SE) technology. Using SE approaches, it is possible to deposit more phosphorus directly under the silver grid to facilitate contact between the grid and the silicon, allowing the electrons to migrate efficiently. At the same time, by reducing the amount of phosphorus between the grid fingers, recombination losses are reduced and the cell's blue response is improved.

There are different ways in which selective emitters can be formed, such as doped silver paste, screen printing, selective diffusion, laser doping, etch back and buried contacts. Of these, laser doping may be the most promising. Centrotherm, together with its partners, has implemented a new SE process using laser doping in different industrial production lines in Asia. The company claims it has demonstrated a 0.50% absolute efficiency gain using its SE technique. The major task in laser-diffused selective emitters is to sufficiently increase the phosphorus concentration in the silicon close to the surface of the laser-treated areas, to enable a good contact resistance without causing too many crystal defects or contamination within the silicon.

Centrotherm's process flow for SE formation suggests that, in the current state-of-the-art process flow sequence, between the diffusion and the phosphorous silicate glass (PSG) etch, there is an additional process step. In this process step the contact resistance of the previously diffused emitter with high sheet resistance and inferior contacting properties is improved to a level of contact quality comparable to standard emitters. The two main cost drivers in SE technologies are the number of additional pieces of equipment added to the production line and the amount (and price) of additional consumables needed. In both respects Centrotherm's laser-diffused selective emitter seems to be very cost effective. There is only one additional piece of equipment – a laser – which needs almost no consumables. Apart from this, the cost structure of the standard process remains unchanged. Thus, the method used is probably one of the most economical SE processes available.

When calculating the cost-saving potential of SE technology, the overall cost structure remains more or less unchanged and so the efficiency gains determine the net benefit. In an alternative approach, DuPont Innovalight offers innovative silicon inks for screen printing selective emitters on the solar cells. The proprietary material comprises silicon nanoparticles dispersed in an environmentally friendly blend of chemicals. For the silicon ink SE cells, as-cut wafers are first cleaned and textured in an alkaline bath to create a random pyramid-textured surface. Silicon ink is deposited in a screen-printing step and heavily doped regions are required for good contact formation. This screen-printing step includes a simple drying process to drive off the remaining organic solvents and densify the printed silicon ink film. An n-type phosphorus diffusion is subsequently performed in a quartz diffusion tube: in this step, selectively doped regions are formed on the front surface of the wafer. Typically, heavily doped printed regions achieve sheet resistance values of 30–50Ω/sq, whereas unprinted areas remain at 80–100Ω/sq.

SE technology offers very good cost-saving potential by substantially increasing the cell efficiency: DuPont claims that, using Innovalight, efficiency can be improved by 2–3%. The Innovalight technology requires the additional cost of silicon ink dopant, and it is assumed that this could add 5% to material costs. The process also requires the silicon ink to be screen printed, for which new screen-printing equipment is needed. It is estimated that this could entail 30% additional capex. Our analysis suggests that there is a cost saving potential of $0.06/W.

Double printing – Esatto (10)

In current state-of-the-art c-Si cell making, a screen-printing method is used to produce electrodes on the cells. In this method, a printing mask that has been formed with a predetermined pattern is placed at a fixed distance from the wafer, and paste (including an electrode material) is applied to the mask. The paste is spread on the printing mask by a squeegee, and only the paste on a meshed area is applied. The coated wafer is then baked at a predetermined temperature, depending on the electrode material, and the electrode is formed. The objective is then to print thin lines that reduce efficiency losses due to the 'shadowing' effect. On the other hand, if the lines are very narrow, increased sheet resistivity reduces cell efficiency. So, in order to optimize the printed line structure, and to increase efficiency and reduce cost, Applied Materials have introduced Esatto – a double-line printing technology.

Esatto was designed to allow the use of advanced contact-formation techniques, such as double-printed front-side metal lines, and the multiple process flows required to create selective emitters. Esatto enables manufacturers to print taller and narrower grid lines that reduce shadowing and improve conductivity. In a production environment, Esatto replaces single 120µm-wide lines with two-layer, double-height lines of width less than 80µm on the finished cell. Customers have demonstrated a 0.46% absolute cell efficiency gain using Esatto and up to a 14% reduction in silver printing paste consumption.

Currently, the front-side silver paste consumption is estimated to be 0.18g/cell (156mm), and the price for paste is approximately $1220/kg. Assuming an average cell efficiency of 14.93%, front-side

paste costs $0.06/W and the total module cost would be $1.12/W. Given a 0.40% increase in efficiency and a 10% reduction in paste usage per cell, the incremental benefit of using Esatto is approximately $0.03/W. Therefore, if the Esatto upgrade costs $650,000, assuming 2000 wafers/hour throughput and 3520 days working per year, the added capita cost is approximately $0.02/W. Given a 5-year system life the additional depreciation expense is 0.50¢/W, resulting in a net benefit of ~$0.03/W when using Esatto.

Direct-printing technology (14)

The challenge in front-contact grid-line printing is to reduce the grid width to limit shading losses without reducing line conductivity in the process. This is to increase the aspect ratio (height/width) while increasing cell efficiency. DuPont, nScrypt and others have presented a direct-printing technology that offers tools for patterning fine grid lines with high aspect ratios. This technology is based on micro dispensing and uses a special pump assembly and a printing head, which is able to handle screen-printable paste and thixotropic materials with very high viscosities. Printing as fast as half a metre per second is possible in some cases. Multiple nozzles enable this process to print each wafer in about 2 seconds.

To achieve fine lines with high aspect ratios, a silver paste for front-side metallization should be modified based on available screen-printing paste. In a typical case, the line is as small as 50µm wide by 30µm tall after firing. This is generally more precise than stencilling, which can usually only achieve a width of around 110–130µm. Direct printing effectively reduces the shading area while maintaining high grid-line conductivity and low contact resistance. The company claims that solar cells made with direct-printed grid lines show up to a 0.5% absolute efficiency increase over those with screen-printed grid lines, resulting in $2–3 million annual savings for solar cell manufacturers.

If it is assumed that direct printing reduces the print width to 50µm from a current width of 120µm, the paste usage could be reduced from 0.184g/cell to 0.112g/cell. Again, this could increase overall cell efficiency by 0.50%. It is calculated that the incremental cost saving achieved by introducing direct printing could be $0.06/W. An nScrypt direct-printing tool could cost 20% more than a normal screen-printing tool. In this case, assuming 2000 wafer/hour throughput, the capex could work out to be $0.11/W. The assumption of a 10-year system life implies a depreciation cost of an additional $0.01/W. Therefore, the net benefit of introducing direct printing could be $0.05/W.

Nickel film contact layer (12)

Reducing the contact resistance is one of the major challenges for the front-side metallization of crystalline silicon solar cells. Screen printing silver paste and firing through the silicon nitride antireflection coating layer is the most common technique for front-side metallization of today's industrial silicon solar cells, but it also produces a poor, very resistive metal-silicon contact.

Palo Alto Research Center has developed new approaches for the front-side metallization of crystalline silicon solar cells using a blanket sputtered nickel film as the contact layer, which is aimed at dramatically reducing the specific contact resistance between the metal grid line and the n+ emitter layer. One technique involves drilling the contact holes in the silicon substrate through the nitride layer using a laser ablation method, and then sputtering a thin nickel film on the whole surface. This is followed by screen printing silver grid lines which are aligned with the contact holes. Finally the uncovered nickel film is etched away using the silver grid lines as a protective mask. This approach could significantly reduce the specific contact resistance and it has been demonstrated that this equates to an absolute efficiency gain of as much as 0.9%. This improvement in efficiency implies that an additional 9W can be generated per 1m^2 area, which translates to a cost saving of $0.064/W. It is estimated that this could involve additional capex: for direct printing, the capex could be as high as 120% of that for current screen-printing tools. Nevertheless, this leaves a net benefit of $0.05/W.

Rear-passivated cells with print-on-print front contacts (13)

In current state-of-the-art cell manufacturing, the silver (Ag) front-side metallization with finger widths of around 90–100µm reflects about 7% of the incident solar radiation. Similarly, the screen-printed full area Al BSF exhibits only a moderate passivation quality. In addition, only about 70% of the infrared light reaching the Al rear contact is reflected back into the silicon wafer. With improvements in these areas, there is a great potential for significantly increasing the cell efficiency.

The Institute for Solar Energy Research Hamelin (ISFH) and DEK Printing Machines have suggested a new approach for overcoming these problems. Before texturing and phosphorus diffusion, a dielectric protection layer is deposited on the rear side of the solar cell. The dielectric layer acts as a barrier against the alkaline texturing process as well as the phosphorus diffusion. Accordingly, only the front side of the solar cell is textured and phosphorus doped, with a sheet resistance of about 70Ω/sq, whereas the rear side remains planar and boron doped. The PSG etch after the diffusion step is slightly adjusted in order to remove the dielectric layer at the rear in addition to the PSG at the front. In the case of Al_2O_3-passivated PERC cells, the wafers are coated with a 10nm plasma-assisted ALD-Al_2O_3 layer. To improve the front printing quality, a print-on-print (PoP) technique has been suggested. The number of fingers has to be increased for PoP in order to minimize resistive losses due to the significantly smaller finger width. The process flow of the PoP cells is identical to standard single-printed solar cells. However, the Ag front contact is deposited in two consecutive screen-printing steps.

Rear passivation and PoP together can result in an efficiency gain of 1% and a reduced silver paste usage by decreasing the print width. It is calculated that these could translate to a cost saving of $0.08/W. However, extra steps are required because of additional chemical deposition and consequent printing; this entails additional capex, which is estimated to be $0.20/W. Therefore, the proposed technological development could yield $0.06/W net benefit.

Busbar optimization (11)

With the price of silver material rising, the cost of screen-printed silver paste has become one of the major components of the total cost in $/W for PV modules. In traditional H-grid front metallization pattern design, over a third of the total metallization area comes from busbars, which are required to be wide enough for terminal contacts in *I-V* measurements and for reducing the series resistance.

The State Key Lab of PV Science and Technology (Trina Solar) has presented a segmental busbar design which cuts down silver paste usage significantly (by over 30%), while the fill factor (*FF*) and maximum output power of the final module remain at the same levels. Experiments on 125mm × 125mm Cz-Si mono cells show that, because of the increase in resistive losses along the busbars, the segmental busbar design will lead to a 0.45% drop in the cell's *FF* and a 0.12% drop in cell efficiency. However, this loss can be compensated for by soldering ribbons in modules, which results in almost the same performance. This implies that over 30% of the cost of silver paste can be saved without any influence on the final module's output power.

Normally two busbars, each 2mm wide, are used in standard cells. Per cell, the busbars usually occupy 612.5mm^2 of area and consume 60mg of silver paste. In the proposed optimization, the busbar regions between contact terminals have been hollowed out, while the regions corresponding to the positions of the *I-V*

tester contact pins remain untouched. In this case, the current from the fingers flows through the edge of the busbar and reaches the contact terminals. Typically around 30% of the busbar area is hollowed out and hence 30% less silver paste is used. Therefore, the amount of paste used per cell busbar area can be reduced to 42mg. Assuming silver paste is priced at $1200 per kg, this implies a net cost saving of $0.01/W.

Ion implantation (7)

In standard solar cell manufacture, the starting material consists of p-type boron-doped silicon wafers. The first process is an acid etch, to remove saw damage and texture the surface, which improves the absorption of incident light. The wafer is then heated in a furnace (800 to 1000°C) with a phosphorous atmosphere, causing a small amount of phosphorous to be incorporated in the outer layer of silicon. This is called 'thermal diffusion', in which phosphorous doping is performed in a furnace with $POCl_3$ gas that creates a light n+ emitter region on the silicon surface. The diffusion causes the creation of PSG, and a hydrofluoric acid etch is done to remove PSG. Diffusion is performed in a furnace with a flow of gas running over the wafers. This step, as with the acid etch, is not selective, so the photoresist and patterning processes need to be done prior to this step.

Ion implantation is being evaluated as a replacement for the diffusion process. While diffusion uses the natural state of gas spreading to locations where there is no gas, ion implantation shoots the desired dopant ions into the wafer. Even though ion implantation has several advantages over diffusion – such as saving energy, time and chemicals – historical semiconductor-based ion implantation tools did not meet the performance and cost requirements of the solar industry.

Intevac recently developed a high-throughput ion implantation tool for solar application, in which wafers are transported horizontally in three columns on a conveyor belt. Despite having a smaller footprint than commercial ion implanters, the ENERGi tool is capable of processing 2400 wafers per hour, with low or high sheet resistivity. The implantation of either n-type or p-type dopants is possible, allowing for greater flexibility in emitter design. It has been demonstrated that the total CoO of this ion implantation tool could be $0.025/W, compared with $0.04/W for the conventional diffusion process. This implies a cost saving of ~$0.04W.

Plasma-etching texturization (6)

Surface texturing is the first process to be carried out on incoming wafers in silicon cell manufacturing. Texturing also allows removal of the saw damage layer that develops during the slicing of the Si ingots into wafers. The defects induced by slicing with a wire saw (in the form of μ-cracks), well known for degrading cell performance, are removed during the texturing process. The isotropic etch in an acidic bath, based on a HF/HNO_3 mixture, is now a standard procedure in the photovoltaic industry for mc-Si with randomly oriented grains.

As an alternative to the well-established isotexture process, MPO Energy, Semco Engineering and others have developed a combination of a wet etch and a plasma process, for which a specific plasma chamber has been designed. The resulting texturing procedure was then successfully implemented in a solar cell process. Surface characterizations underlined the fact that no plasma damages occur during this texturing process. Solar cell results exhibit an increase in short-circuit current density and no drop in open-circuit voltage. This leads to a gain in efficiency for the plasma-texturing process, compared to the standard texture process (alkaline or acidic).

The new approach could result in an improvement of 0.15% in efficiency. This implies that an additional 1.5W can be generated per $1m^2$ area. This translates to $0.011/W in cost savings. Normally, a texturization tool could cost $2 million and it is assumed that the additional capex could be 50% of that amount. This implies that $0.002/W additional annual depreciation charges would be incurred in implementing this approach, therefore leaving a net benefit of ~$0.01/W.

Mono-cast ingot (2)

Silicon ingots can be either mono or multi. Mono ingots are much more efficient than multi ingots, but are more expensive to manufacture. GT Advanced Technology has developed a new technique called 'MonoCast' to produce quasi-mono ingots at a very low cost. The DSS450 MonoCast furnace produces the industry's highest mono volume yield in production ingots comprised of up to 25 bricks. The new mono-cast technology uses a lower-cost multicrystalline ingot process to manufacture higher-quality, mono-like ingots, without the associated higher production costs. Cells produced from DSS450 MonoCast wafers are claimed to have lower light-induced degradation (LID). Moreover, the full-square surface dimension area across the MonoCast wafer provides greater surface area (~1.8% more) for electricity generating than the pseudo-square shape of traditional monocrystalline wafers. MonoCast ingots produce three grades of wafers: Grade 1 (mostly mono), Grade 2 (hybrid) and Grade 3 (mostly multi). Over 95% of the wafers produced are either Grade 1 or Grade 2.

Mono-cast technology offers sizable cost savings by increasing the ingot quality, which in turn results in greater cell efficiency. The current weighted-average cell efficiency is assumed to be 14.93%. It is believed that mono-cast quasi cells could increase the cell efficiency by 0.35%, which could result in a 10% reduction in ingot material usage. Our analysis suggests that there is potential for reducing the total cost by $0.03/W.

Induction melting in cold crucibles (1)

The standard technology used for producing multicrystalline silicon ingots is the directional solidification method in quartz crucibles. This method has several drawbacks: inhomogeneity of ingots;

Source: Intevac

Figure 8. Intevac's ion implantation tool for manufacturing solar cells.

part of the material is contaminated with oxygen/metal impurities; the productivity of growing is rather low, etc.

To overcome these drawbacks, Tesys Ltd. and Piller Ltd. introduced the process known as induction melting in cold crucible (IMCC) as an alternative to directional solidification. The technology of producing multicrystalline silicon ingots by the IMCC method consists of induction heating and melting of silicon held in a water-cooled (cold) segmented copper crucible. Melting is accompanied by ingot formation via crystallization of the melt in the cross-sectional shape of the cold crucible, thus forming the ingot; the IMCC technology is consequently considered to be continuous casting. Application of induction heating provides a high concentration of energy in the melting zone, thus achieving a high rate of fusion and high-speed crystallization and formation of the ingot. At the same time, the resulting ingot has both a uniform structure and a homogeneous distribution of impurities along its entire length.

IMCC offers significant cost savings by increasing the productivity and reducing the consumption of disposable quartz crucibles and graphite components. A 20% productivity gain and 40% reduction in crucible usage are assumed and no graphite component consumption is required, resulting in a potential net benefit of $0.01/W.

Multiple dye doping of EVA (15)

In a study the School of Engineering and Physical Sciences at Heriot-Watt University, Edinburgh, UK, have optimized the light-absorption properties of luminescent encapsulation layers made from (poly)ethylene vinyl acetate (EVA), by using multiple dye doping and varying the concentration of the most promising dye. These layers were used to encapsulate mc-Si solar cells. This led to a 25% enhancement of the external quantum efficiency (EQE) for the region 300nm < λ < 400nm, leading to an efficiency increase of $\Delta\eta$ = 0.3% absolute for a 59cm^2 single-cell mini-module.

By optimizing the light-absorption properties of EVA by dye doping, module efficiency could be increased by 0.3%; this implies that an additional 3Wp power can be produced per 1m^2 area. It is assumed that this multiple dye doping could cost 20% of the EVA cost, which would result in a potential saving of $0.02/W if this new approach were adopted.

Backsheet developments (16)

Most backsheets are multilayer composites which enhance the performance of PV modules in many ways. They offer protection from the environment, provide electrical insulation and contribute to aesthetics. The backsheet has a dominant role in providing long-term protection for the solar module. It has been established that the main reasons for PV system failure include degradation of packaging materials, adhesional loss, degradation of interconnects, degradation due to moisture intrusion, and semiconductor device degradation. Improvements in backsheet quality are therefore reflected in improved system life, decreased degradation and, to some extent, improved yield, which could reduce the cost of production. Consequently, the best parameter to look at for expressing improvement in backsheet technology and quality is the levelized cost of energy (LCOE), because, as the backsheet improves, the LCOE can fall. Indeed, paradoxically, an increase in the per watt manufacturing cost may be offset by a decrease in degradation, resulting in increased system lifetimes.

Peel strength, water vapour transmission rate (WVTR), dimensional stability and dielectric strength are considered to be some of the critical factors in determining the quality of the backsheet; these factors have an impact on the LCOE of the module. An exhaustive database of backsheets, including 39 products offered by 13 companies, has been created. However, different companies may apply different chemistries, so, to assess them, the following assumptions have been made in order to calculate the LCOE for different backsheets.

To avoid delaminating effects in the long run, it can be assumed that peel strength should be higher for the backsheet. It has been noted that the average peel strength for the backsheets in the database is 4.84N/mm, with a minimum of 2.5 and a maximum of 12.0. A backsheet is considered to be 'excellent' if peel strength is greater than or equal to 6.0 and 'bad' if peel strength is less than 3.0. If peel strength is 'excellent', the annual power degradation can be reduced by 0.1% and the system life increased by 2 years; if it is 'bad', the annual power degradation can be increased by 0.1% and the system life reduced by 2 years.

It can also be assumed that WVTRs for the backsheet must be more effective in blocking water vapour in the air from entering the panels over time. The WVTRs averaged 2.75g/m^2 per day, with a minimum of 0.8 and a maximum of 9.0, in our database of backsheets. A backsheet is considered to be 'excellent' if the WVTR is less than or equal to 1.5 and 'bad' if the WVTR is greater than 3.5. When the WVTR is considered 'excellent', annual power degradation could be reduced by 0.2%; if the performance is 'bad', annual degradation may increase by 0.2%.

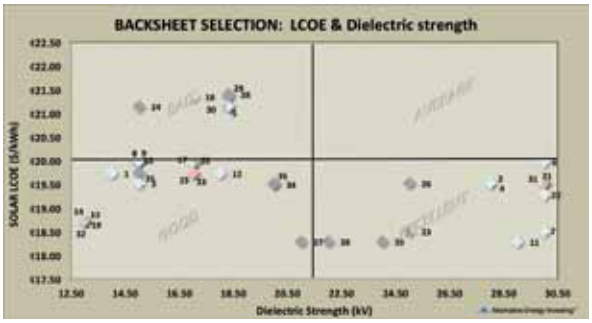
Dimensional stability is assumed to be a factor because, as a backsheet changes its shape, the manufacturing yield could be lower. An average dimensional stability of 1.21% was noted, with a minimum of 0.05% and a maximum of 5%. A backsheet is considered to be 'excellent' if its dimensional stability is less than or equal to 0.8% and 'bad' if its dimensional stability is greater than 1.5%. If the dimensional stability is 'excellent', the manufacturing cost could be decreased by 3%; if it is 'bad', the cost could be increased by 3%.

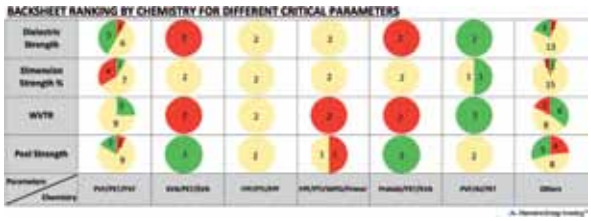
On the basis of these assumptions and frameworks for ranking this group of backsheets, the LCOE was calculated for a typical module incorporating these backsheets in Frankfurt, Germany. The analysis showed that the lowest LCOE is achieved for Solar Gard's backsheet (11 in Fig. 9), which uses PVF/PET/PVF chemistry; the highest dielectric strength is noticed for Krempel's backsheet (31 in Fig. 9), which uses PVDF/PET/PVDF chemistry. On the whole, Solar Gard (11 in Fig. 9) and DuPont (7 in Fig. 9) backsheets, with higher dielectric strength, have demonstrated relatively lower LCOEs. However, technology changes may rewrite the rankings observed here.

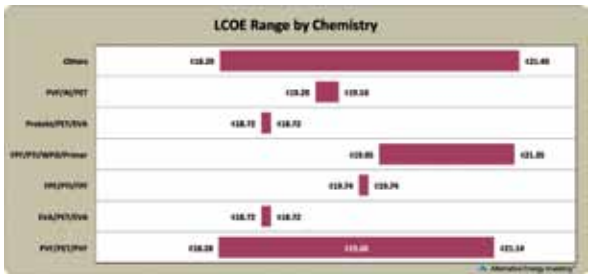
Most multilayer backsheets are constructed from laminated layers glued together, with distinct adhesive layers. An alternative to laminating different layers with adhesive is a coating process: coating one or more layers is a well-known way of producing highly functional multilayer structures. DuPont, Asahi and Daikin are some of the major companies developing this promising field of fluorinated coatings for photovoltaic backsheets. Coating-based backsheets can simplify their manufacturing process by dispensing with the need for an adhesive layer to bond the fluoropolymer to the PET. This allows a thinner construction.

In 2009 DuPont introduced PV2400, which is a system for making TPT by coating PVF formulations directly on PET. After coating, the formulations are heated and processed in a similar way to PV2100. However, in the case of PV2400, the dried PVF coating adheres to the coated substrate. At the end of 2011, DuPont developed TPNext – a solar backsheet technology based on a single protective layer – which improves adhesion for c-Si solar module encapsulants, resistance to UV light, and backsheet production throughput. The new laminate consists of Tedlar film, polyester and an extrusion-coated tie layer that reduces the use of organic solvent-based adhesives. An extrusion-coated process is used to put down the tie layer. Since no solvents are used, it can be done at much greater line speed than traditional means for putting down solvent-based adhesives. This results in enhanced productivity for the backsheet makers. DuPont expects to release TPNext in 2012.

# No	Company	Chemistry	Peel Strength Ranking	WVTR Ranking	Dim Strength Ranking	Dielectric Strength	LCOE €/kWh
1	Krempel	PVF/PET/PVF					19.74
2	Krempel	PVF/PET/PVF					19.53
3	Krempel	PVF/PET/PVF					19.53
4	Krempel	PVF/PET/PVF					19.53
5	Dunsolar	PVF/PET/PVF					21.14
6	Dupont	PVF/PET/PVF					19.86
7	Dupont	PVF/PET/PVF					18.51
8	Hefon New energy	PVF/PET/PVF					19.86
9	Hefon New energy	PVF/PET/PVF					19.86
10	Hefon New energy	PVF/PET/PVF					19.86
11	Solar Gard	PVF/PET/PVF					18.26
12	Isovolta	PVF/PET/PVF					19.74
13	Madico	EVA/PET/EVA					18.72
14	Madico	EVA/PET/EVA					18.72
15	SFC	FPF/PET/FPF					19.74
16	SFC	FPF/PET/FPF					19.74
17	SFC	FPF/PET/WPO/Primer					19.86
18	SFC	FPF/PET/WPO/Primer					21.36
19	Madico	Protekt/PET/EVA					18.72
20	Madico	Protekt/PET/EVA					18.72
21	Krempel	PVF/Al/PET					19.53
22	Krempel	PVF/Al/PET					19.29
23	DNP Solar	ETFE / PET / Olefin					18.51
24	Dunsolar	Fluorinated Layer / PET / Primer					21.14
25	SFC	FPF/Al/PET/Primer					19.86
26	Avery Dennison	FPF/PET/FPF					19.53
27	SFC	FPF/PET/FPE					19.74
28	Dunsolar	PET / PET / Primer					21.40
29	Dunsolar	Primer / PET / Primer					21.36
30	Dunsolar	PVDF Film / PET / Primer					21.14
31	Krempel	PVDF/PET/PVDF					19.53
32	Madico	PVF/PET/EVA					18.72
33	Backfilm	PVF/PET/FPE					19.74
34	Covemo	PVF/PET/Primer					19.49
35	Filmcutter	SN/PET/SN					19.74
36	Isovolta	PA/PA/PA					19.53
37	Isovolta	PA/PET/PA					18.29
38	Isovolta	FPF/PET/PA					18.29
39	Isovolta	PVF/PET/PA					18.29







PVF: poly vinyl fluoride
WPO: low - oligomer white polyester film
PTI: polyester film
ETFE: ethylene tetrafluoroethylene
PA: polyamide
Protekt: multi-layered laminate

FPF: fluoropolymer
PET: polyethylene terephthalate
SN: saturated nonwoven
PVDF: polyvinylidene fluoride
FPE: fluoropolyethylene resin

Figure 9. Backsheet selection.

"The innovations discussed in this paper offer a way to bring the cost of modules down from the current $1.12/W level to $0.43/W by 2016."

Conclusions

Now, more than ever, the industry must reduce the cost of everything, from upstream to downstream, to bridge the gap to achieving grid parity. Quality must also remain a critical component: there is nothing more harmful to the industry's potential than cutting corners and sacrificing quality. But these two requirements mean very little without profitable volume.

By taking a fresh look at which processes, as well as which technologies, show the most promise, a degree of cost reduction has been estimated for the industry in the near term that delivers on the three key mandates of cost, quality and profitability. PV demand is expected to soften before once again accelerating in the future. A widening gap between demand and supply is creating tremendous dislocations in the marketplace. On the basis of announced capacity expansion by major module makers, it is assumed that the gap could widen in the near future, resulting in additional price reductions. This increases the pressure on module makers to reduce the cost of production.

A number of innovative technological advancements that focus on cost reduction have been identified. The innovations discussed in this paper offer a way to bring the cost of modules down from the current $1.12/W level to $0.43/W by 2016. While many of these innovations may fail to transition into commercial production, those mentioned seem to be the most likely of the hundreds of others to be tested by the industry. Therefore, despite the risk of failure, they set the stage for c-Si module costs to reach a level that by any account opens natural markets for solar around the globe.

About the Author

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