Crystallization on dipped substrate wafer technology for crystalline silicon solar cells reduces wafer costs

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ABSTRACT

A new wafer technology, named CDS (Crystallization on Dipped Substrate), is under development and has been found to be effective in the reduction of wafer cost and silicon feedstock. CDS technology was applied to 156mm × 156mm-sized wafers, obtained via the throughput of 1825cm²/min, and the resulting cell efficiency of 14.8% was confirmed. This paper outlines the principle behind the technology and outlines the procedure

Introduction

The silicon wafer-based solar cell plays a main role in the present photovoltaic market. As a result, the development of wafer technology is very important in realizing the mass supply of inexpensive solar cells. Conventional multi-crystalline silicon wafers are produced by ingot casting technology; however, the reduction of wafer cost and silicon feedstock is difficult because of the unavoidable sawing process. On the other hand, ribbon technologies hold hope, due to the lack of kerf losses. However, these technologies have the problem of low throughput, or small wafer size. Therefore, a new ribbon technology has been developed that has demonstrated high throughput and large wafer size.

CDS technology

CDS enables the formation of multicrystalline silicon sheets directly from molten silicon, with no kerf loss.

Basic principle

Figure 1 illustrates the basic principle behind CDS technology. Firstly, a substrate is dipped into molten silicon. The silicon crystallizes uniformly at the surface due to the extraction of the latent heat. Secondly, the substrate is pulled out from the molten silicon. Next, a multicrystalline silicon sheet is detached from the substrate. Finally, it is cut to an appropriate size by a laser cutter [1].

Development of CDS technology

The development of CDS technology began in 1997 and in the intervening 11 years, the technology development achieved practical-sized wafers (156mm × 156mm) – a figure that is compatible with high throughput (1825cm²/min). The progression to this point is shown in Figure 2.

Comparison with other ribbon methods

There are many other kinds of silicon ribbon technologies, such as Edge-defined

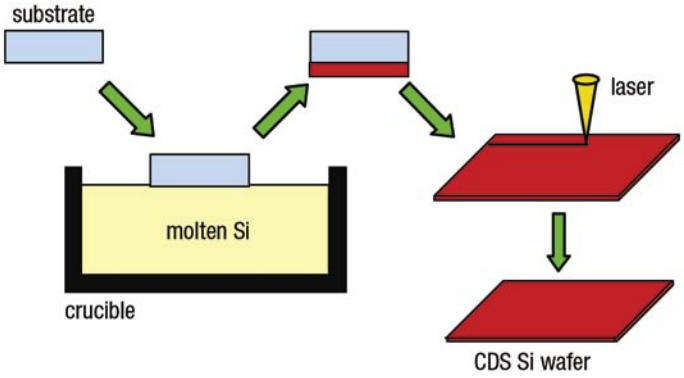

Figure 1. Principle of the CDS Si wafer production technique.

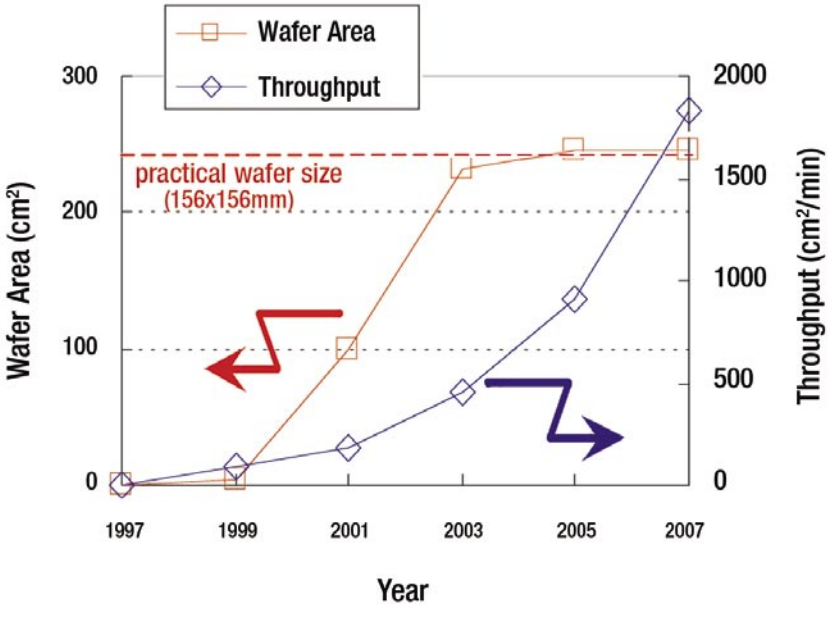

Figure 2. Development of CDS technology.

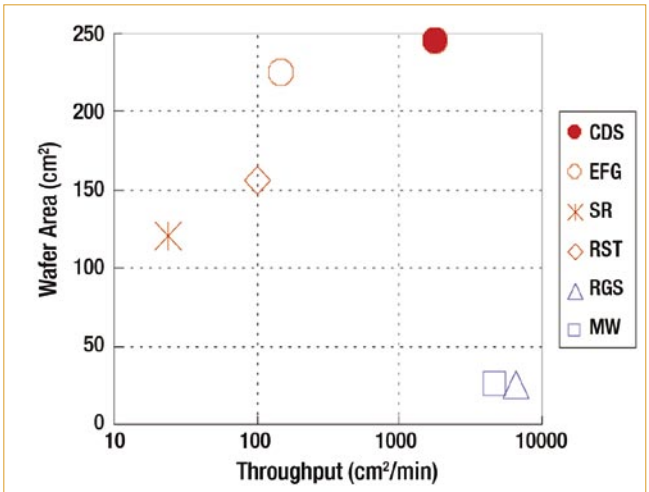

Figure 3. Wafer size and throughput of ribbon methods [2-7].

Figure 4. CDS Si wafer (156mm × 156mm).

Film-fed Growth (EFG), String Ribbon (SR) Ribbon Growth on Substrate (RGS), among others. From a practical point of view, both wafer size and throughput are hugely important. Figure 3 shows wafer size and throughput of these technologies. EFG technology boasts excellent wafer sizes, while both RGS and Molded Wafer (MW) technologies present excellent throughput. CDS technology has achieved both practical-sized wafer and high throughput, and is a ribbon method much suited to mass-production.

CDS wafer and facilities

Figure 4 shows a 156mm × 156mm-sized wafer obtained via CDS technology. Figure 5 shows a general view of the CDS process, an inline wafer process that enables the production of 10,000 wafers in one day (one wafer every 8 seconds). Therefore, a wafer cost of approximately 50% of cast-process wafer was achieved in our estimation.

> "CDS technology has achieved both practical-sized wafer and high throughput, and is a ribbon method much suited to mass-production."

Characteristics of CDS silicon wafers

CDS technology is significantly different from other ribbon technologies. Therefore, we have evaluated the properties of the new wafer by surface photovoltage analysis (SPV), and electron backscatter patterns analysis (EBSP) [8]. Surface photovoltage (SPV) measurements are used to determine the minority carrier diffusion length of a silicon wafer. The minority carrier diffusion length of CDS Si wafer turned out to be longer than 100μm.

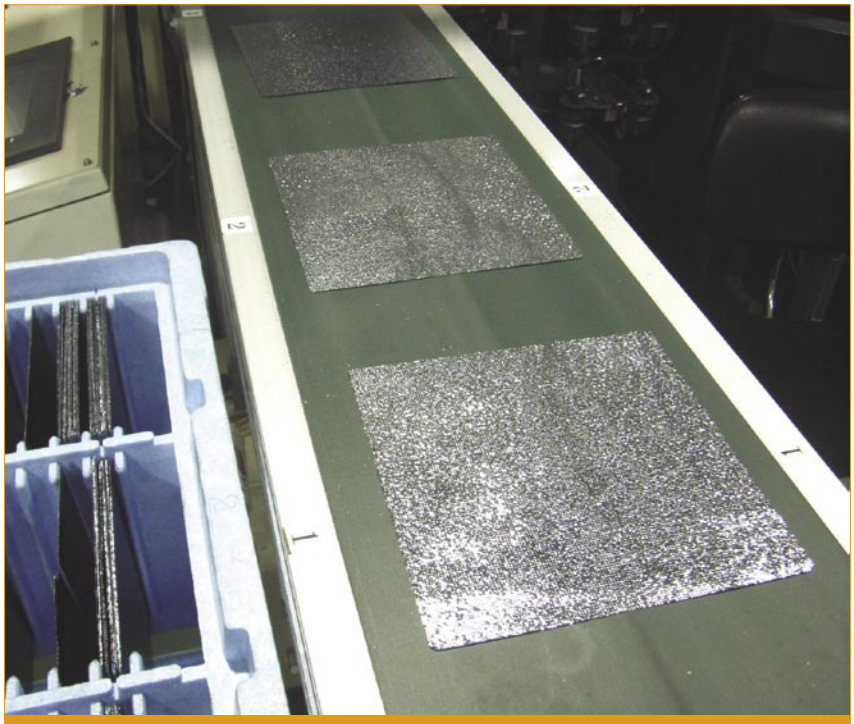

Figure 5. General view of the CDS process.

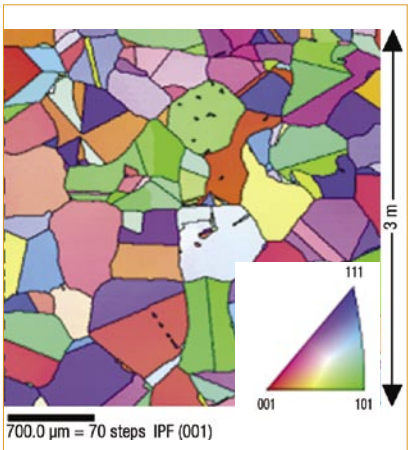

Figure 6. Planar IPF map of a CDS Si wafer.

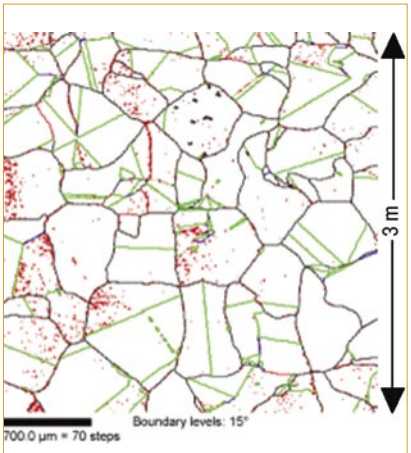

Figure 7. Coincident site lattice map of a CDS Si wafer (black: random; green: Σ3; red: other CSL GB and errors).

The evaluation of the multicrystalline silicon grain boundary that uses the Electron Backscatter Patterns (EBSP) method was reported in recent years. Figure 6 shows the planar Inverse Pole Figure (IPF) map of the CDS Si wafer. Judging from the result of the IPF map within our observed range, there can be no specific silicon growth directions in any CDS Si wafers, with grain sizes of 1mm or less, similar to externals.

Elements such as grain size and crystal direction, as well as silicon grain boundaries, have a huge impact on the cell's efficiency. The straight grain boundary, known as twin, or the Σ3 coincident site lattice (CSL) grain boundary, signifies good quality and electric inactivity. Figure 7 shows the CSL map of the CDS Si wafer, clearly showing remarkable Σ3 CSL grain boundaries.

A cross-sectional map of the crystalline orientations showing confirmed columnar grain structures is presented in Figure 8. While there are relatively few grain boundaries in the up-and-down direction, through which current flows in the solar cells, it is expected that these columnar structures will induce an excellent result in the cells.

Cell processing and cell development results

Solar cell process

A quite simple screen-printing-based cell process was applied to CDS as shown in Figure 9. However, since the crystalline property of CDS is quite different from cast Si, each process has been optimized to CDS taking its character into consideration.

An example of process optimization is the firing of the aluminum back electrode by rapid thermal processing (RTP). The firing time of RTP is much shorter than conventional firing and we have succeeded in an increase of about 1.0 in absolute efficiency by RTP compared to conventional firing [9]. It is presumed that such an eminent improvement by use of RTP is caused by hydrogen passivation or aluminum gettering. Since CDS Si wafers have many grain boundaries, there must be a significant amount of space for such an improvement by such an effect.

Development of CDS cell efficiencies

Figure 10 shows the development of CDS cell efficiencies. 14.8% cell efficiency of CDS cell was obtained in 2006 by a quite simple process of in-house measurement. This is the result of step-by-step refinement of each process, such as the RTP technique application.

CDS modules

A practical-sized module (1165mm × 990mm) made up of 42 solar cells (156mm × 156mm) was also fabricated in this process, and a maximum output power of

Figure 8. Cross-sectional map of crystalline orientations (black: blank). CDS Si wafers had a quite small grain size, but contained columnar grain structures and good grain boundaries, elements that are suitable for solar cells.

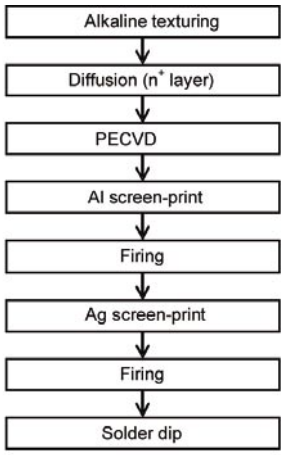

Figure 9. Flowchart showing stages of the cell process.

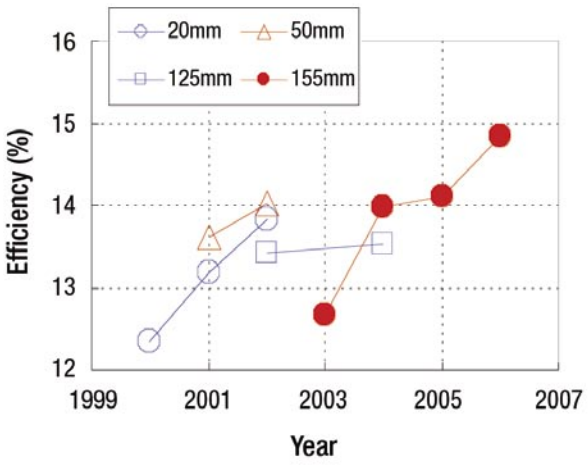

Figure 10. Development of the CDS cell efficiencies.

Figure 11. The appearance of the practical-sized module (1165mm × 990mm) made up of 42 screen-printed CDS solar cells.

144W($\eta_{AV.}$=14.2%) was confirmed through in-house measurement. The resulting module is shown in Figure 11.

"Characterizations of wafers showed that CDS Si wafers have columnar grain structures, containing a significant amount of high-quality grain boundaries."

Conclusions

A new technology, CDS, which is effective in the reduction of wafer cost and silicon feedstock, has been developed. Through use of this technology, practical-sized wafers (156mm × 156mm) featuring high throughput (1825cm^2/min; 10,000 wafers production in one day) were demonstrated, and a low wafer cost (approximately 50% of cast wafer) was estimated. Characterizations of wafers showed that CDS Si wafers have columnar grain structures, containing a significant amount of high-quality grain boundaries. Using these wafers, solar cells and solar cell modules were fabricated using a conventional low-cost process. Cell efficiency of 14.8% and module maximum output power of 144W were confirmed.

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