Methods of emitter formation for crystalline silicon solar cells

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ABSTRACT

The emitter or p-n junction is the core of crystalline silicon solar cells. The vast majority of silicon cells are produced using a simple process of high temperature diffusion of dopants into the crystal lattice. This paper takes a closer look at the characteristics of this diffusion and possible variations in the process, and asks whether this step can lead to optimal emitters or whether emitters should be made with different processes in order to obtain the highest possible efficiency.

Basic properties of emitters and requirements for optimal performance

The ideal scenario

The operation of solar cells relies on light absorption generating electron-hole pairs. Electrons and holes then diffuse and/or drift to a charge-selective interface and are spatially separated as positive and negative charges at that interface (a process known as 'collection' – see Fig. 1). Collection leads to build-up of a potential difference between both sides of the interface, more commonly known as the cell voltage. The cell will generate a current when collected charges are allowed to flow through an external circuit.

The most important parameter for practical use is obviously the power output of the cell, which is equal to the product of voltage and current. Electron-hole pairs may be bound (excitons) or unbound, leading to distinctly different device design requirements. In the case of crystalline silicon, electron-hole pairs are normally unbound, which means that generated electrons and holes are able to move independently. The standard interface used for charge separation is the p-n homojunction. Here, 'p' and 'n' refer to p- and n-type doping, respectively, while 'homo' indicates that the doping is present in the same kind of semiconductor material which, in this case, is crystalline silicon. The resulting structure is a silicon bipolar diode. A well-known alternative for the selective interface is a heterojunction, where two different semiconductor materials are combined, e.g. crystalline and amorphous silicon.

The reverse process of generation of electron-hole pairs is recombination. When silicon is driven out of thermal equilibrium by light absorption and generation of extra electron-hole pairs, it will naturally respond by (net) recombination. This may prevent electrons and holes from being separated, since they may recombine before reaching the junction. Recombination may therefore lead to a reduced output current. Another effect of recombination is reduction of output voltage, as will be discussed later. Part of the art of solar cell processing and design is thus to minimize recombination and to maximize the probability for electrons and holes to be separated and collected.

The most commonly used solar cell device structure in crystalline silicon is a planar diode structure (see Fig. 2), where a thin layer of heavily doped silicon (n^+ or p^+) is present at the front surface of a moderately doped wafer of the opposite type (p or n). The heavily doped region is often called the emitter, while the moderately doped (wafer) material is referred to as the base. The term 'emitter' can be appreciated after a more detailed treatment of the p-n junction behaviour. The emitter area is the region that 'emits' (injects) most of the charge carriers under (dark) operation. It is also found in transistor terminology, where 'emitter', 'base' and 'collector' are the device regions.

For the majority of commercial solar cells the wafer is p-type, but there is an increasing interest in n-type silicon. Reasons for the interest in n-type silicon are the absence of light-induced degradation due to boron-oxygen complex formation and the lower sensitivity to impurities of n-type silicon compared to p-type silicon. There is no fundamental reason why the p-n junction should be present at the front of the cell and neither is it essential to employ a planar structure. The most extreme and relevant illustration is the back-junction back-contact solar cell, where the collecting junction is present in the form of highly doped regions at the rear of the device. This cell is also referred to as the Interdigitated Back Contact (IBC) solar cell and has been developed and commercialized by SunPower Corp.

In the current standard process, the emitter is formed by in-diffusion at high temperatures of an n-type dopant (phosphorous, P) into the surface region of a p-type wafer doped with boron (B). By adding phosphorous at much higher concentrations than the background boron doping level, the surface region is inverted from p- into n-type silicon and a p-n junction is formed. This region thus consists of 'compensated' material. The point at which p- and n-type active doping concentrations are equal is called the metallurgical junction. On both sides of the metallurgical junction a depletion (also called space charge) region is found. This region is depleted of mobile charge carriers and thus only contains fixed charges at the ionized doping atoms, the

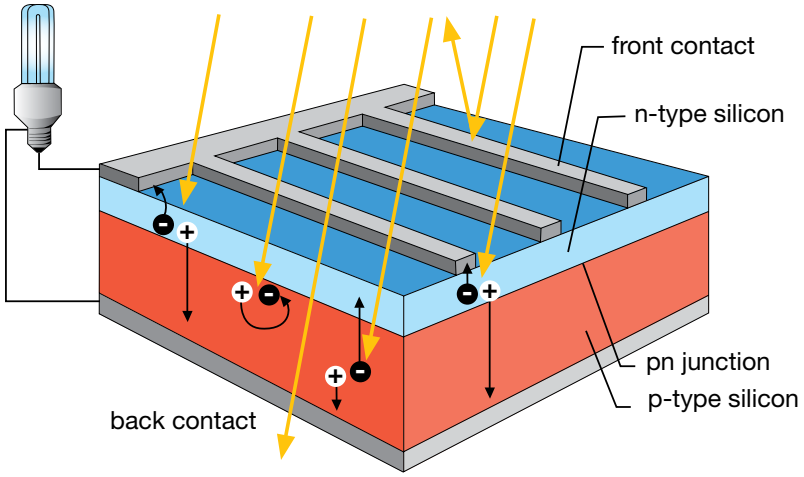

Figure 1. Schematic cross-section of a crystalline silicon solar cell under illumination.

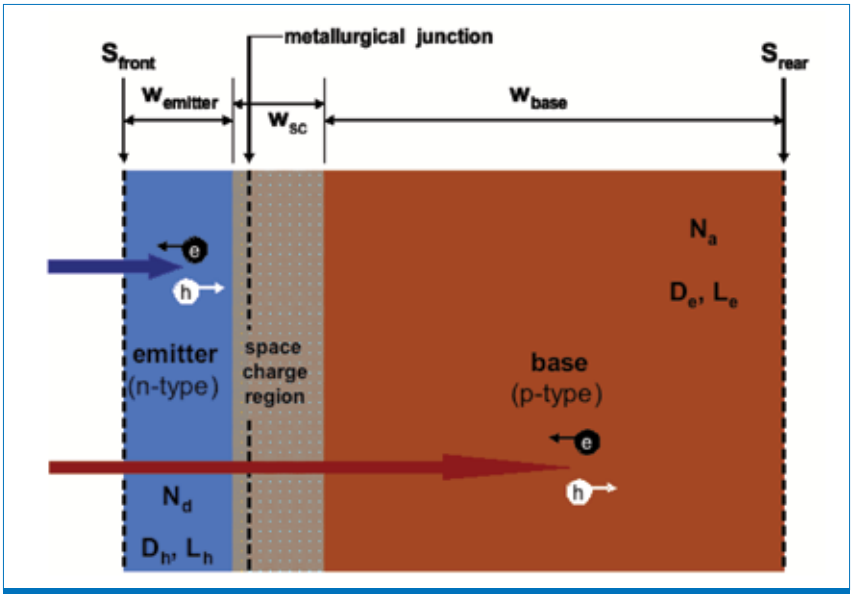

Figure 2. Schematic cross-section of a p-n junction solar cell, indicating the neutral emitter and base regions and the space-charge region around the metallurgical junction. It is shown schematically that red (long wavelength) light generates electron hole pairs deeper in the wafer than blue (short wavelength) light.

so-called space charge. At the n-type side of the junction the space charge is positive; at the p-type side it is negative. Note that the total space charge is zero: charge neutrality still holds on the device level. The widths of the space charge regions on both sides of the metallurgical junction therefore depend on the respective doping concentrations. For a heavily doped emitter (typically 10^{19}cm^{-3}) on a moderately doped base (typically 10^{16}cm^{-3}), almost the entire depletion region thickness of roughly 1µm is found on the base-side of the junction. An electric field is present within the space-charge region. This field counteracts the diffusive force on mobile charge carriers that results from the huge asymmetry in concentrations at both sides of the junction and allows establishment of an equilibrium situation. Note that the material outside the depletion region is field-free.

In order to understand the design and processing requirements for solar cell emitters, it is essential to consider the equation of an ideal solar cell under illumination [1]:

$$J(V) = J_o(\exp\frac{qV}{kT} - 1) - J_l \qquad (1)$$

where J(V) is the solar cell output current density as a function of voltage, J_0 is the diode saturation current density (also called dark current density), q is the elementary charge, k is Boltzmann's constant, T is the absolute temperature and J_l the light-generated current density (normally equal to the short circuit current density J_{sc}).

The saturation current density J_0 of the p-n diode is given by:

$$J_0 = \frac{qD_e n_i^2}{L_e N_a} + \frac{qD_h n_i^2}{L_h N_d} = J_{o,base} + J_{o,emitter} \qquad (2)$$

where D and L are the diffusion coefficient and diffusion length of minority electrons (e) in p-type silicon (usually the base) and holes (h) in n-type silicon (usually the emitter), respectively. The intrinsic carrier concentration, n_i, is constant at a given temperature, N_a is the acceptor doping concentration in p-type silicon, and N_d is the donor doping concentration in n-type silicon. Note that in thermal equilibrium $n_i^2 = [e]\cdot N_a = [h]\cdot N_d$. This relates the minority carrier concentrations to the majority carrier concentrations and thus to the doping concentrations for the case that all doping atoms are active and have donated an electron or a hole.

The diffusion length L (i.e. the average distance a generated minority carrier travels before it recombines) is determined by the diffusion coefficient D and the minority carrier lifetime τ, where $L = \sqrt{D\tau}$. L and τ are dependent on the strength of recombination. Materials and layers of high (electronic) quality are characterized by a long lifetime and a long diffusion length, although it should be noted that 'long' is a relative concept and must be defined in relation to device dimensions.

In general, three recombination mechanisms play a role: radiative recombination (the true inverse of generation by light absorption), defect-level-assisted recombination (also called Shockley-Read-Hall, SRH recombination) and Auger recombination. Defect levels may result from crystal imperfections in the bulk of the material and at the surfaces. Crystalline silicon has an indirect band gap [2], and both light absorption and radiative recombination are relatively weak processes because of the indirect nature of the band structure. Therefore defect-assisted and Auger recombination are the dominant mechanisms. As a rule of thumb, defect-assisted recombination limits the quality of industrially used moderately-doped silicon, while Auger recombination is dominant in heavily-doped silicon layers (and in very-high quality, high-purity, low-defect silicon). Surface recombination is determined by defects.

The quantitative values of $J_{o,base}$ and $J_{o,emitter}$ and thus also their relative importance may vary greatly with actual device and material parameters. For solar cell device optimization, both base and emitter components need to be taken into account.

From Equation 1 it follows that the open-circuit voltage V_{oc} of the cell (V @ J = 0) is given by:

$$V_{oc} \cong \frac{kT}{q}\ln(\frac{J_{sc}}{J_0}) \qquad (3)$$

Maximizing V_{oc} thus implies minimizing J_0 and, as far as possible, maximizing the short-circuit current density J_{sc} (assumed equal to J_l).

In a very simple model, where material properties and the generation rate G are assumed to be constant, the short-circuit current density is given by:

$$J_{sc} = qG(L_e + W_{sc} + L_h) \qquad (4)$$

in which W_{sc} represents the total thickness of the space-charge region. The current-contributing regions of the cell lie within one diffusion length from the junction.

The third parameter determining solar cell efficiency is the fill factor (FF):

$$FF \equiv \frac{J_{mp}V_{mp}}{J_{sc}V_{oc}} \qquad (5)$$

where J_{mp} and V_{mp} represent the current and voltage at maximum power output, respectively. For ideal diodes the value of FF is an only function of V_{oc} [3], but in practical cases FF is limited by other effects, as outlined in the following section.

Non-ideal diode behaviour: surface and resistance effects

Equations 1, 2 and 6 hold for an ideal diode without surface effects, i.e. with infinite dimensions $W_{emitter}$ and W_{base}, as depicted in Fig. 2. In view of the importance of finite dimensions and surface recombination, a more general description that takes into account surface effects can be used [3]:

$$J_0 = \frac{qD_e n_i^2}{L_e N_a} * F_p + \frac{qD_h n_i^2}{L_h N_d} * F_n \qquad (6)$$

where F_p and F_n are functions of the following parameters:

S – the surface recombination velocity (the product of S and the minority carrier concentration [e] or [h] yields the flux of carriers recombining at the surface).

$\frac{W}{L}$ – ratio of the layer thickness W to the diffusion length (L, the 'span of control' of the junction, represents the typical thickness of the region that is influenced by surface properties). If $\frac{W}{L} >> 1$, surface quality is of minor importance; if $\frac{W}{L} << 1$, device quality is dominated by surface properties.

$\frac{D}{L}$ – the 'diffusion velocity', is the volume equivalent of surface recombination velocity. If an 'infinitely thick' base or emitter region of a solar cell, in which recombination is fully determined by volume recombination, is made thinner, recombination in the new structure is equal to that in the old structure if the surface recombination velocity is set at $\frac{D}{L}$.

Thus, if one is able to make high-quality surfaces with $S << \frac{D}{L}$, device behaviour may be improved by using thinner or electronically more transparent (smaller $\frac{D}{L}$) wafers or (emitter or back surface field) layers, provided that light absorption can be sufficiently maintained.

Note that Equation 1 does not yet account for the effects of series (R_{se}) and shunt resistance (R_{sh}), nor does it include the effects of recombination in space-charge regions, which leads to non-ideal diode behaviour, expressed through the occurrence of a current term J_{on} with an ideality factor $n \approx 2$. Note that lateral inhomogeneities in diode characteristics such as local variations in series resistance and minority carrier lifetime may also result in an (apparent) ideality factor $n > 1$ [2]. Taking these effects into account yields the current-voltage characteristic as shown in Equation 7 below).

$$J(V_a) = J_{o1}\left(\exp\frac{q(V_a - JR_{se})}{kT} - 1\right) + J_{0n}\left(\exp\frac{q(V_a - J_{se})}{nkT} - 1\right) + \frac{V_a - JR_{se}}{R_{sh}} - J_l$$

Equation 7.

R_{se} and R_{sh} are so-called lumped parameters, in which contributions from all parts of the device are taken together. This is obviously just an approximation of more accurate 2D and 3D device models. The expression shows that the voltage over the actual junction in the device, which governs the diode current, may be lower than the voltage over the device terminals (i.e. the applied voltage V_a). This leads to a loss in fill factor, and hence, in efficiency.

While the effects of shunt resistance may be negligible in well-processed practical devices, series resistance can usually only be optimized for maximum device performance. Series resistance is associated with current conduction in various parts of the device. The components related to the emitter are (see Fig. 1):

- lateral transport of collected carriers through the emitter to the contact (emitter 'sheet' resistance, which is the integral of emitter resistivity over depth);
- transport through the silicon-metal interface (contact resistance);
- transport through the front metal pattern.

Real emitters

As mentioned, emitters are usually formed by diffusion of dopant atoms into the silicon wafer surface. This does not yield a constant doping concentration throughout the layer as assumed so far. In the case of an infinite dopant source, diffusion ideally leads to a complementary error function doping profile; in the case of a finite source a Gaussian profile is obtained. As a result, the second term in Equation 2 has to be evaluated as a function of depth and Equation 6 takes a more complex form. Clearly, this can only be done using numerical simulation tools like PC-1D [3]. In addition to these rather trivial modifications, another effect needs to be considered. In the case of relatively high doping density gradients $\frac{dN_d}{dx}$ such as in the emitter, an electric field ε is formed even outside the depletion region [3]:

$$\varepsilon(x) = -\frac{kT}{q}\frac{1}{N_d}\frac{dN_d}{dx} \qquad (8)$$

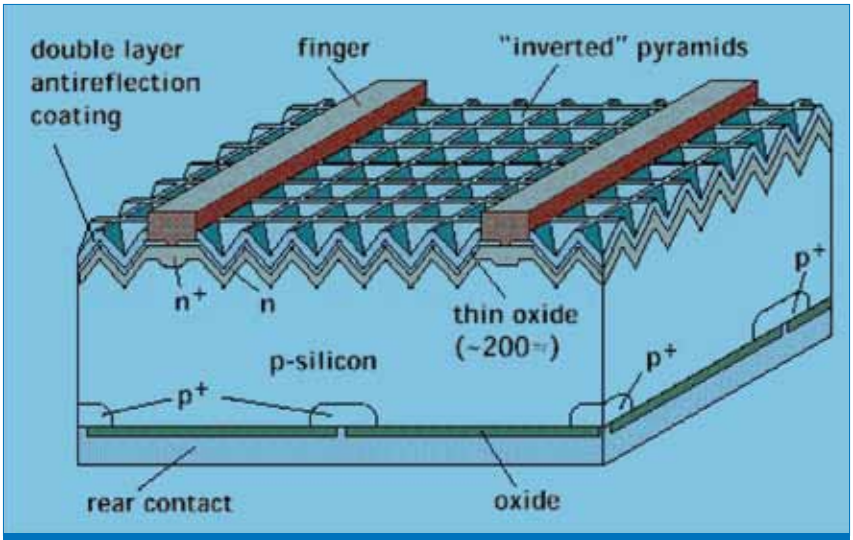

Figure 3. Passivated Emitter Rear Locally diffused (PERL) cell [8].

Although the strength of this field is much lower that that of the depletion region, it may assist diffusion of generated minority carriers to the junction (and thus prevent them from diffusing to the surface where they might recombine) by adding a small drift component.

The optimum doping profile (peak concentration, shape and depth) in the emitter can only be evaluated using a multi-parameter analysis. Moreover, the optimum is different for (shadowed) emitter regions under the front metallization and regions in between the metal fingers. This has led to the development of so-called selective emitters, where the doping profiles in both regions are different. Regions under the metallization do not have to absorb light and contribute to current generation, but they do need to provide a low-resistivity contact to the metallization (i.e., majority carriers can cross the interface without significant losses).

Furthermore, they need to prevent excessive recombination of minority carriers at the ohmic contact, which is characterized by a very high recombination velocity. This typically leads to a relatively deep doping profile with a very high surface concentration and a significant doping gradient. The high doping concentration at the surface guarantees the formation of low-resistivity tunnel contact [7], while the combination of concentration, depth and gradient reduces surface recombination. In terms of Equation 6, $\frac{W}{L_{eff}} > 1$, in which L_{eff} is the 'effective' diffusion length in the emitter. It is noted that L decreases with doping concentration due to increasing Auger recombination.

Emitter regions in between the metal fingers need to be designed taking the following aspects into combined account:

- *efficient collection of the carriers* generated by light absorption in the emitter (determining the internal quantum efficiency for short-wavelength light);
- *low-loss lateral transport of (majority) carriers* from the location where they are collected to a nearby metallized area (this translates to an emitter sheet resistance in relation to the distance between metal fingers, which is in turn determined by the (minimum) width of fingers that can be made to avoid excessive shadow losses);
- *maximum output voltage* (see Equation 3). At first glance this seems to point towards maximizing the doping concentration, but when the decrease of diffusion length with doping concentration is considered, one finds an optimum rather than a maximum. This is strongly influenced by the possibility of providing a surface passivating coating on the emitter.

In practice, optimization of the parameters involved (taking into account the boundary conditions set by processing) leads to a doping profile that is distinctly different from that under the metallization. Under the condition that surface recombination can be effectively reduced by a well-passivating coating, it pays to reduce the overall doping concentration in the emitter to a minimum that is set by the requirement of low resistance losses for lateral current transport. In contrast to the region under the metallization, the active emitter regions are thus characterized by $\frac{W}{L_{eff}} < 1$, allowing efficient collection of generated carriers, but also minimizing the right-hand term in Equation 6, and thus maximizing the output voltage (see Equation 3). The argument can even be enforced: for carrier collection, the best emitter is a very thin emitter. The collection efficiency achieved in the regions under the emitter (depletion region and moderately doped base) is normally better than that achieved in the highly doped emitter.

It is emphasised, however, that detailed design optimization for practical (industrial) cells should take into account the actual lowest value of the surface recombination velocity that can be achieved as a function of surface doping concentration (see the considerations about S vs. $\frac{D}{L}$ with Equation 6).

The concept of selective emitters has been applied very successfully in the 25% world-record cell made by Professor Martin Green and his team at the University of New South Wales [5] (see Fig. 3). This Passivated Emitter Rear Locally diffused (PERL) cell even employs a further refinement of the selective emitter design, by using emitter-contact areas that are narrower than the metal fingers on top. This sophistication allows a better trade-off between surface recombination at the silicon-metal interface and contact resistance losses.

Heavy doping, dead layers and impurity gettering

Standard diffusion processes can present an infinite source of impurities. These processes result in an impurity concentration in the emitter surface region equal to the solid solubility at the temperature involved. For phosphorous at a temperature range of 850-950°C, the solid solubility is $\approx 3 \cdot 10^{20} cm^{-3}$ (≈ ½ % of Si atoms is replaced by a P atom). Ideally, the active carrier (electron) concentration should be equal to the phosphorous concentration. At such extremely high carrier concentrations, Auger recombination is very effective and lifetime and diffusion lengths are very short. Moreover, P atoms may not be distributed homogeneously and (thus) phosphorous may be present at even higher concentrations, distorting the silicon lattice and leading to enhanced defect-assisted recombination. Under such conditions, not all dopant atoms are active and the chemical P-concentration may be higher than the electrically active concentration. Such surface layers are characterized by extremely short lifetimes and are called 'dead layers' accordingly. They may seriously deteriorate cell performance, particularly in active (unshaded) emitter areas. If dead layer formation cannot be avoided, it may be useful to remove it, either by chemical etching or by a drive-in diffusion during which the phosphorus impurities are redistributed over a thicker layer. Alternatively, dead layer formation may be prevented by reducing the dopant source strength or by diffusion through a barrier layer.

In specific cases the extremely high emitter dopant concentrations may be used to enhance cell performance. Highly doped (distorted) layers may act as sinks for impurities during gettering. At high temperatures (such as used in diffusion), lifetime-degrading impurities in the base of the cell become mobile. If the effective solubility in the highly doped emitter regions is higher than in the base of the solar cell, impurities may end up primarily in the emitter (they are 'gettered'). Provided that the negative effect they have in the emitter is smaller than the effect they had in the base, this will lead to enhanced cell performance. Given the fact that emitter recombination is normally determined by

Auger processes (as opposed to impurity- and defect-assisted processes) and taking into account that the emitter contribution to the saturation current density J_o may be small compared to that of the base, this is not an unlikely situation.

Practical emitters formed by diffusion

Diffusion is the most common way of forming an emitter for c-Si solar cells. It does not require vacuum equipment and a large number of wafers (500) can be processed at once. The electricity consumption is small in spite of the high process temperature. Therefore, cost of ownership (CoO) of a diffused emitter is small compared to the overall CoO of a solar cell's manufacture. This technology was transferred from the semiconductor industry at the introduction of c-Si solar cells. In the meantime, the diffusion process is unpopular in the semiconductor (especially VLSI) industry because of its limited controllability of the doping profile.

For most solar cells, phosphorus is applied as an n-type dopant. Before phosphorus is diffused into the silicon, phosphorus has to be fixated on the silicon surface because the phosphorus diffusion temperature in silicon is above 800°C. At that temperature, most simple phosphorus compounds (e.g. P_4, P_8, P_2O_5, etc.) are at vapour phase.

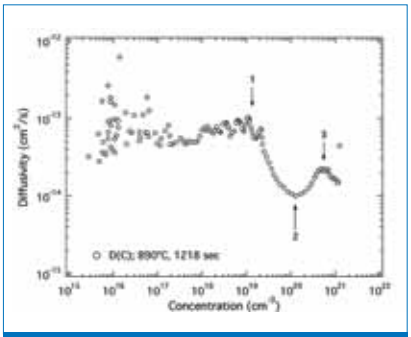

Figure 4. Phosphorus diffusivity as a function of phosphorus concentration [6].

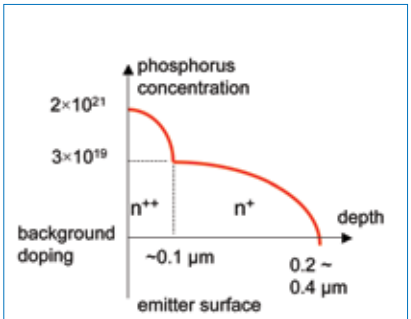

Figure 5. Schematic phosphorus dopant profile of a diffused emitter.

This is why a film of phosphosilicate glass (PSG), or $SiO_2:(P_2O_5)_x$ is required as a dopant source.

The amount of P_2O_5 in PSG is preferred to be 4%, which is the upper limit of incorporation. A stable and uniform formation of PSG is key to reproducible formation of the emitter layer. If the PSG concentration is not uniform, the doping profile will not be uniform either, reducing solar cell efficiency. Oversupplying phosphorus is an easy method to achieve uniform formation of PSG with saturated concentration of P_2O_5.

At the interface of PSG and silicon, P_2O_5 is reduced and phosphorus is

	J_{sc} (mA/cm²)	V_{oc}	FF (%)	Eff. (%)
Single plateau (conventional)	33.4	610	77.8	15.9
Multi plateau	33.7	613	77.8	16.1

Table 1. Results for 243cm² mc-Si cells as average values of 25 cells. Efficiency, J_{sc} and V_{oc} are improved, including a 0.2% absolute gain for the efficiency, while the fill factor is kept at the same level.

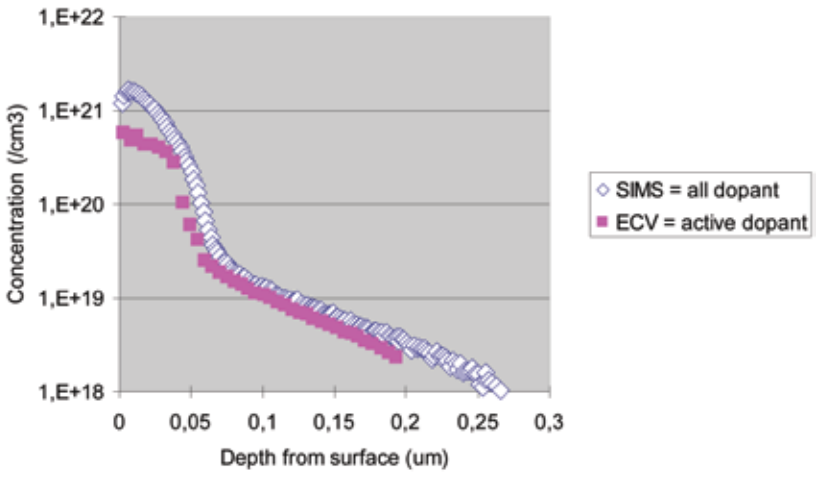

Figure 6. SIMS and ECV of a typical phosphorus dopant profile.

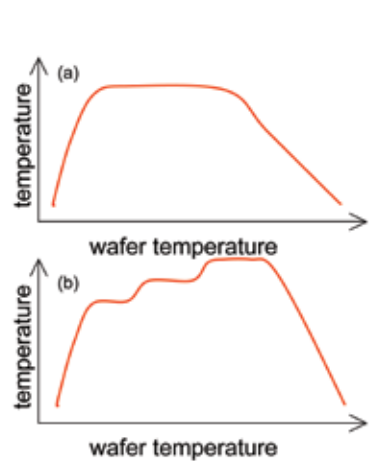

Figure 7. (a) Typical temperature time (T-t) curve with single temperature plateau carried out at the industrial production lines; (b) T-t curve example with multiple plateau.

supplied to silicon:

$$2\,P_2O_5 + 5\,Si \rightarrow 4\,P + 5\,SiO_2.$$

Although the solid solubility of phosphorus in silicon is known from literature to be less than 5~8 × 10^{20}cm^{-3}, SIMS measurements indicate that phosphorus concentration near the PSG/Si interface (Si side) is about 2 × 10^{21}cm^{-3} which corresponds to about 4% the saturation value of P_2O_5 in SiO_2.

There are several methods of forming PSG. Most PSG is formed by decomposition of gaseous, phosphorus oxychloride ($POCl_3$). $POCl_3$ is a colourless liquid material with a boiling point of 106°C. It is normally introduced into a process chamber using bubbling by inert gas. After wafers in the process chamber are heated to 800~850°C, $POCl_3$ is introduced with a small amount of oxygen, resulting in $POCl_3$ being decomposed to P_2O_5 which is captured into the SiO_2 film growing on the surface by oxidation. This process requires a closed or semi-closed reaction chamber to isolate harmful and corrosive by-products (mainly Cl_2). Normally, a quartz tube furnace is used which can stand both high temperature and corrosive atmosphere. PSG formation and subsequent drive-in processes are carried out in one continuous (single) step.

A second method is deposition of a liquid phosphorus containing source, like a sol-gel or diluted phosphoric acid. A sol-gel consists of phosphorous doped silicate, i.e. a network of interchained SiO_2 and P_2O_5, dissolved in some solvent. Coating with sol-gel is normally performed using spinning of a few drops on a c-Si wafer. With a properly chosen solvent, it is possible to spray a sol-gel or phosphoric acid on a wafer. Baking after coating enables the formation of PSG. A subsequent drive-in step is performed separately or can be performed in the same furnace.

A subsequent phosphorus drive-in can be performed, which in essence is a simple annealing process. When $POCl_3$ or phosphoric acid is used for PSG formation, PSG formation and drive-in are performed in a single heating step. Since the temperature for PSG formation is normally high enough to drive phosphorus atoms into the silicon crystal, drive-in already starts at the beginning of the PSG formation.

Bentzen et al. investigated the dependence of phosphorus diffusivity on the phosphorus doping concentration [P] and observed three phase transitions in the diffusivity as shown in Fig. 4 [6].

Transition points are indicated with arrows 1, 2, and 3 in Fig. 4 at [P] = ~2×10^{19}, ~2×10^{20}, and ~6×10^{20}cm^{-3}, respectively. These transition points cause different diffusion speeds at different doping concentrations, resulting in a doping profile which cannot be described with a simple Gaussian distribution model. Fig. 5 shows a schematic phosphorus emitter profile formed with the diffusion process.

Two Gaussian-like curves appear: one starts at the surface and the other starts at [P] ≈ 3×10^{19}/cm^3 due to the transition point 1 (arrow 1 in Fig. 4) where diffusion speed is several times higher at [P] < 2×10^{19} than at [P] = ~1×10^{20}. This causes the formation of two different layers with different [P], henceforth referred to as n^{++} and n^+ layers.

The existence of the n^{++} layer has both positive and negative effects. The major positive effect is that it enables a good metal contact. One of the negative effects is that the heavily-doped phosphorus in the n^{++} layer results in an increased carrier recombination, yielding a lower operating voltage of the solar cell. Highly doped phosphorus causes both higher surface recombination and higher emitter bulk recombination. A higher voltage and a better contact are therefore

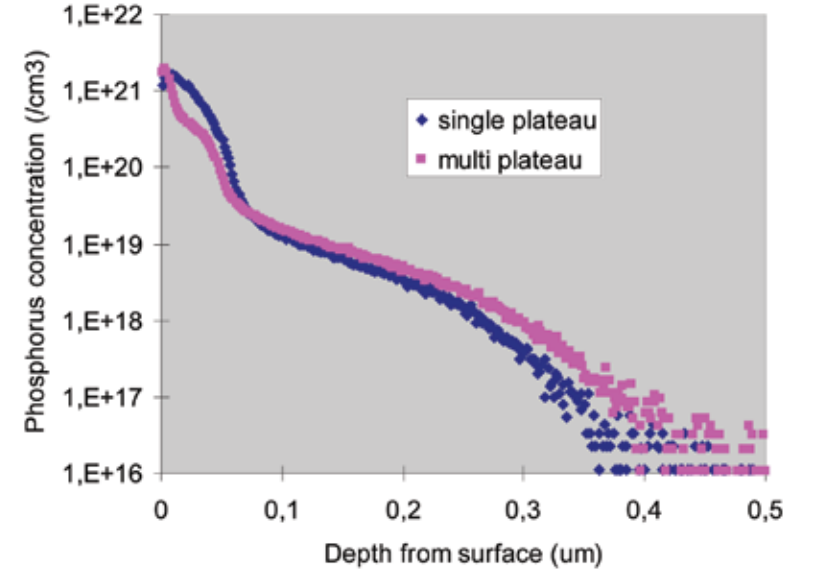

Figure 8. SIMS phosphorus dopant profiles for single- and multi-plateau temperature profiles.

contradictory requirements, and a compromise must be reached by optimizing the n^{++} layer.

Fig. 6 shows a typical phosphorus doping profile characterized by SIMS (secondary ion mass spectroscopy), and compares it with an active dopant profile by ECV (electrochemical capacitance voltage). The active dopant concentration levels off close to 3×10^{20} as is expected from the solubility limit described earlier. The difference between these two curves suggests the existence of a large number of inactive phosphorus atoms, which are likely to contribute strongly to the surface and the bulk emitter recombination, related to the 'dead layer' effect that was described earlier.

In order to minimize the effect of the inactive high dopant region, we manipulated the doping profile [7] to optimize the phosphorus concentration to a 'moderate' level without increasing the total diffusion process time. This is achieved by introducing so-called 'multi-plateau' time temperature curves as shown in Fig. 7, resulting in the reduction of phosphorus atoms toward the active dopant levels in the n^{++} layer (see Fig. 8).

Recently, boron diffusion has been attracting much interest. The principle of boron diffusion is the same as phosphorus diffusion – like phosphorus, the diffusion source of boron should be fixated in a borosilicate glass (BSG) formed on a silicon surface; the boron oxide is reduced at the interface of the BSG and Si; the boron atoms are driven in into Si; and the emitter surface is exposed after BSG is removed by HF solution.

However, there are several differences:

1) A highly-boron-doped layer may have some gettering effect, but it does not have such a strong effect of preventing contamination from inside or outside the wafer [8] as phosphorus. A significant lifetime drop was observed using a BSG formation process with a metal conveyor furnace and sol-gel diffusion source [9]. Therefore, a quartz tube with BBr_3 (boron tribromide) as the source material should be used.
2) Boron oxide, the diffusion precursor of boron, is in the liquid phase at the temperature of BSG formation and drive-in, while phosphorus oxide, the phosphorus precursor, is in vapour phase. This is why it is more difficult to distribute the BSG precursor uniformly to the silicon wafers in the process chamber than the PSG precursor.
3) The temperature suitable for drive-in is 900~950°C, which is almost 100°C higher than that of phosphorus.
4) At the interface of the BSG and the boron emitter, boron atoms are precipitated as B-Si alloy. This makes it difficult to remove BSG with HF solution as it is therefore an oxidation of the B-Si alloy that is needed.
5) Peak boron doping concentrations as measured by ECV and the SIMS are almost identical at $1\sim2\times10^{20}cm^2$. This suggests that a diffused boron emitter does not include inactive boron atoms even in its heavily-doped region, unlike a phosphorus emitter.

ECN has recently overcome these aspects and published high efficiencies on n-type cells with a boron emitter [10].

Emitters formed by ion implantation and anneal

An alternative method to create a dopant profile for an emitter is to use ion implantation. In the 1980s, good laboratory solar cells were made with implanted emitters on single-crystalline substrates, either shallow and passivated [11] (V_{oc} exceeding 640mV) or deep and passivated [12].

Ion implantation is used in microelectronics because of its good process control and repeatability of amount and position of the doping [13]. Implantation is based on creation of a beam of dopant ions, which are accelerated by typically keVs and bombarded onto the silicon wafer. Conventional tools are of the beamline type (with a magnetic mass analyser to improve the purity of the ion beam). The ion source uses source gases such as PH_3 or BF_3. More recent developments are plasma-assisted doping, and plasma immersion ion implantation (acronym PIII or P3i) which were developed for high dosing requirements. However, these methods (PLAD, PIII) do not offer the mass filter capability of a beam line.

As for conventional emitters, an implanted emitter will have to make a trade-off between the requirements for emitter recombination (low surface concentration) and contact (high surface concentration). Profiles have been published [14] with a concentration far exceeding the solid solubility at drive-in temperature in the first nanometres from the surface. This likely produces similar properties as the dead layer in classical diffusion: good contacting but high recombination.

Advantages of implantation are:

- excellent control over surface dose;
- potentially better control over the doping profile. Implantation allows the complete separation of the steps of deposition (for example, creating a delta-doped layer) and drive-in;
- the possibility of patterned implantation to create, e.g., selective emitter structures and interdigitated back contact cells. This could lead to very high efficiencies;
- the possible absence of a need for a separate edge isolation process step.

Implantation allows an elegant cell fabrication sequence by implanting front and rear of the wafer with opposite dopants, followed by a combined drive-in (what would nowadays be called 'co-diffusion'), where the drive-in is used to simultaneously form a passivating oxide layer [11].

Potential disadvantages are:

- the need to anneal to remove implant damage at the relatively high temperature of 900°C and higher (which can, however, be combined with the drive-in);
- possible absence of effective gettering by phosphosilicate glass;
- possible co-implantation of unwanted impurities; and
- possibly cost and throughput. To produce a 100Ω/square emitter sheet resistance, at least 7-8E14cm^{-2} phosphorous atoms will be required. It is within reach of the highest currents that can be produced in some tools (20-40mA) to realize this in 1 second. However, this dose excludes the formation of a highly doped surface area for metal contacting and the increase of doping required for a textured surface. Clearly, very high dose implant methods (10mA or more) will be required for PV.

Both high temperature anneal and potential absence of gettering may be a reason why implantation is unsuitable for multicrystalline silicon. In any case, there are no literature reports on high performance implantation doped mc-Si solar cells.

Emitters grown by epitaxy

Epitaxial growth can be a potential alternative for emitter formation. Its main advantage is the speed of emitter formation. When high temperature CVD is employed, it takes less than 1 minute to form a 1µm-thick emitter [15] while diffusion requires at least 20 minutes [16]. In addition, the epitaxial emitter can be varied in profile and a lowly doped high efficiency emitter can be easily realised [17]. No dopant deposition is necessary, as the emitter is grown in-situ by adding the dopant gas to the silicon precursor. Furthermore, no glass is formed, which is the case when using an oxygen-containing dopant. Therefore, less chemical etching is needed before and after the emitter formation.

Schmich carried out a wide range of studies on epitaxy of emitters grown by high temperature (1000°C-1170°C) CVD, including boron-doped p$^+$-emitter and phosphorus-doped n$^+$-emitter, in which the investigated cell size was as large as

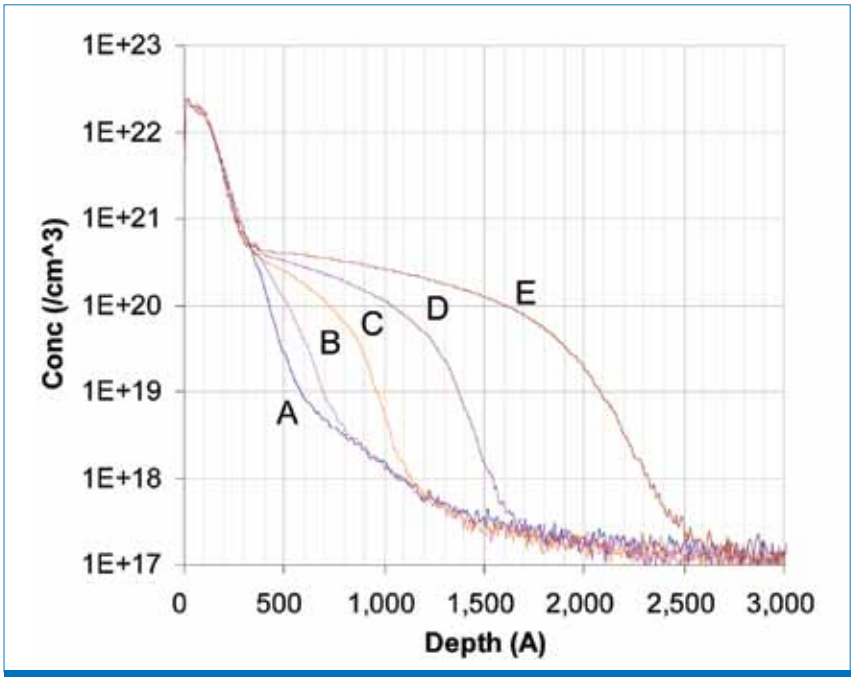

Figure 9. SIMS profiles of P3i B_2H_6 implants (8 sec., 8kV wafer bias, 3×1016/cm^2 dose) followed with 25 second anneals at (A) 900°C, (B) 950°C, (C) 1000°C, (D) 1050°C and (E) 1100°C (from [14], courtesy of Applied Materials).

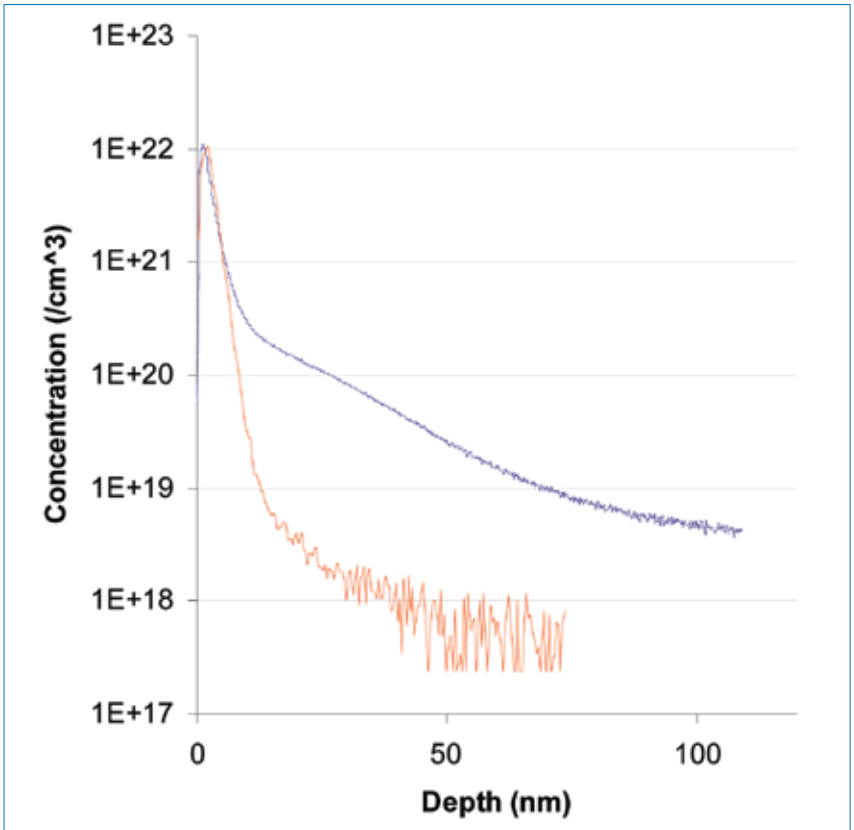

Figure 10. SIMS profiles for PH_3 implants at different energies (from [14], courtesy of Applied Materials).

10 × 10cm² and both evaporated contact (Al/Ti/Pd/Ag for p^+ and Ti/Pd/Ag for n^+-emitter) and screen-printed paste of Ag [18]. The monocrystalline silicon solar cell with an epitaxiyally-grown n^+-type emitter in the best case showed the efficiency of 14.9% and a V_{oc} of 655mV, which was 7mV higher than that of the reference cell with a $POCl_3$-diffused emitter. The same V_{oc} difference of 7mV was shown for multicrystalline silicon, wherein the V_{oc} was 634mV and the efficiency was 13.4%. While evaporated contact was employed in this case, the best monocrystalline cell with screen-printed contact showed a V_{oc} of 618mV. The study implies that this value can still be improved upon. Since the principal motivation of this work is to develop the emitter for an epitaxially-grown base region of thin-film crystalline silicon, the emitters mentioned here were grown on some 20µm-thick epitaxially-grown base. Nevertheless, the epitaxial emitter also functions sufficiently for the case grown directly on a wafer as well as that grown on an epitaxial base.

Fig. 11 illustrates the doping concentration profiles of the epitaxial emitter with ca. 1µm deposition. To prevent the out-diffusion of phosphorus from the surface after the emitter growth – which causes a large contact resistance with the metal contact, PH_3 flow must be kept while cooling. Since the emitter depth of the best cell is 0.9µm with the sheet resistance of 85Ω/square, the optimal profile should look like a horizontally shrunk version of the curve with closed squares in the figure.

The doping profile is much deeper than that of a diffused emitter. Therefore, the recombination is much lower and the open circuit voltage is higher. It is questionable whether the surface concentration of an epi emitter is high enough to allow for a good screen-printed contact. One of the drawbacks of the epitaxial emitter is the inhomogeneous thickness of the emitter due to its high growing speed. However, the surface doping concentration can be almost uniform, enabling uniform contact resistance.

Another drawback of the epitaxial emitter is the implementation of texture surface. Schmich attempted the emitter growth on a pyramidary textured wafer [18]. The reproducible fabrication condition was not yet established, though one of the cells reached an efficiency of 16.5% with a V_{oc} of 607mV, J_{sc} of 34.4mA/cm², and FF of 79.0%.

Van Nieuwenhuysen et al. took a different approach [19]. They used the method of plasma texturing of already epitaxially-grown emitter followed by additional epitaxial growth of thin and highly doped top layer. The solar cells using this epitaxial stack showed (on average) an efficiency of 16.0% with a J_{sc} of 33.0mA/cm², a V_{oc} of 621mV, and FF of 78%.

Even though these applications of the epitaxial emitter to c-Si solar cell processes are still limited to laboratory scale, the intrinsic drawback against the diffusion emitter looks to have been solved already. This suggests that the epitaxial emitter can be a real alternative to the diffusion process in the future, because of the benefit of its much shorter process time and easier controllability of the doping profile. Since the epitaxial emitter process is compatible with the thin-film epitaxial base growth process, it will highly probably be employed when the concept of epitaxial thin-film Si solar cells is realized [20].

Inversion layer junctions as emitter

An alternative to the diffused p-n junction is the metal insulator semiconductor inversion layer. This junction is formed at the interface of SiN_x coating on a p-type wafer with moderate resistivity (1 – 1.5Ω/cm). Fixed positive charges in the dielectric layer increase the electron density close to the SiN_x/Si interface such that they become the majority carrier.

These junctions are characterized by a very small width depending on the surface charge's density and wafer resistivity. This is well illustrated in Fig. 12, where an n^+ region of the diffused emitter profile (R_{sheet} 60Ω/sqr) is compared to the profile of a surface charge induced emitter (Q_f =5e12cm^{-2} both on a 1.5Ω/cm p-type wafer). As a consequence of this shallow junction with peak electron densities in the order of 1e19 and 1e20cm^{-3}, the sheet resistance of surface charge induced emitters are typically in the range of 10,000 to 4,000Ω/sqr respectively [21], which is much

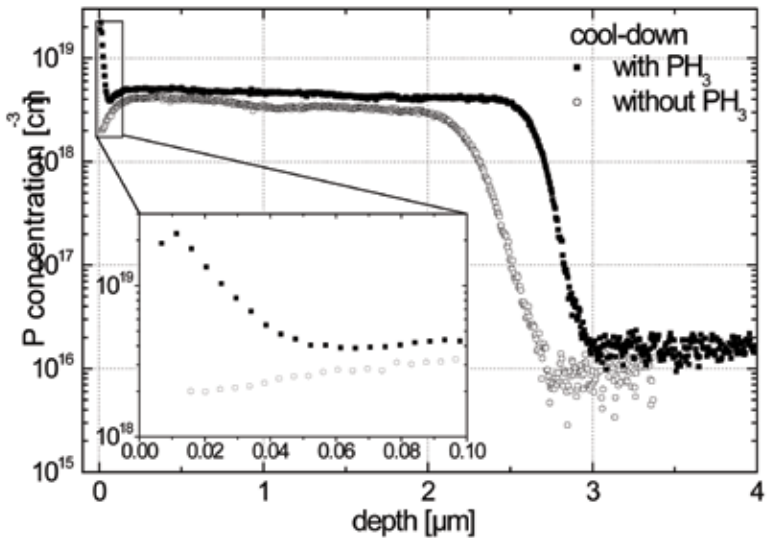

Figure 11. SIMS measurement of epitaxial emitters cooled with and without PH_3 [18].

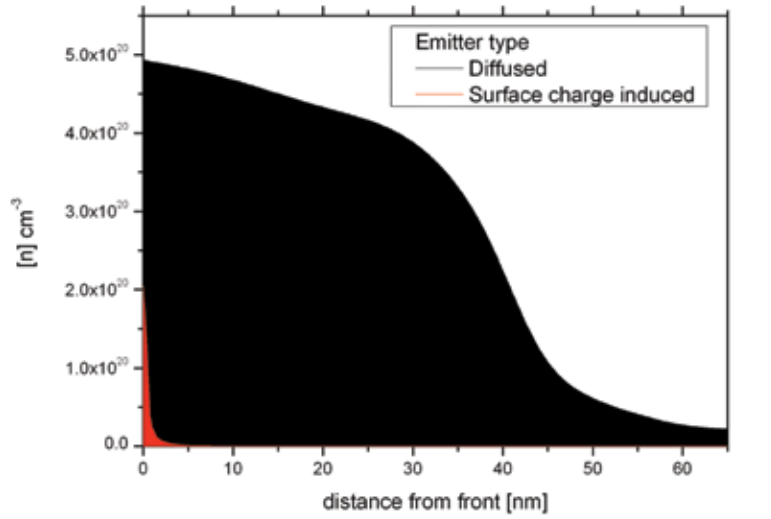

Figure 12. Electron density distribution of two emitter types: diffused phosphor emitter and surface charge-induced emitter.

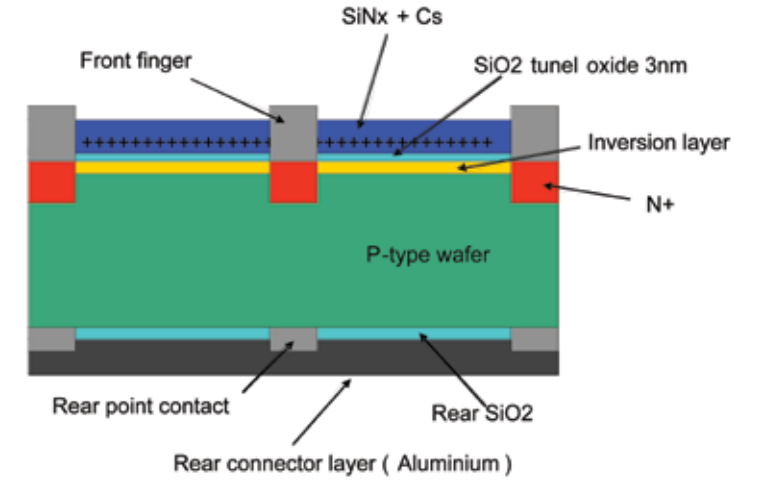

Figure 13. Structure of MIS-IL solar cells with oxide rear surface passivation and additional evaporated CsCl-layer. Front surface received random pyramid texture and a 4% metallization coverage, comprising of 300 micron pitched fingers.

higher than for diffused emitters (50 to 100Ω/sqr).

Another difference is the contacting scheme. As the emitter formation depends on the presence of the dielectric layer on the surface, it is necessary to find a way of extending the emitter below the front metal contacts. This has been achieved by local diffusion below the contact in analogy of selective emitters [22] but also by formation of a Schottky barrier. Careful selection of the metal work function of the leads allows formation of an inversion layer below the contacts (ϕ<4.5eV). One attractive candidate is aluminium for its low cost, its abundance and suitable work function (4.1 - 4.3eV). Thin films of CsCl (5nm) have been found to have even lower work function in the order of 2.1 eV, which increases the band banding even further and reduces contact recombination and J_o [23]. To further reduce contact recombination, a tunnelling oxide (d~1.5mn) is often used as it offers a selective tunnel path for majority carriers.

The MIS-IL solar cell has demonstrated cell efficiencies that reach 20% with very high V_{oc} values up to 693mV and J_0 values as low as 60fA/cm²) [22]. This demonstrates the potential for high efficiency concepts comparable to diffused junctions. The high efficiency cell concept is illustrated in Fig. 13.

This leads to the following advantages:

- no high temperature diffusion step is required;
- the inversion layer can be achieved with an SiN_x anti-reflection coating;
- no recombination effect due to diffused impurities and very low dark saturation currents.

and disadvantages:

- a new contacting scheme is required with related uncertainty in reliability;
- no impurity gettering effect exists, making it unsuitable for lower quality silicon wafers; and
- high sheet resistances lead to resistance losses.

Heterojunctions

A heterojunction emitter combines two different materials to create the charge-separating field. Both, but particularly the silicon heterojunction emitter, based on thin amorphous silicon films on a crystalline silicon wafer, are under intense R&D, as both have been proven by Sanyo to be very successful for creating high-efficiency solar cells [24].

The special properties of the silicon heterojunction emitter are that 1) they allow for excellent surface passivation, and 2) they provide reasonably effective selective contacts for majority carriers, reflecting minority carriers back into the wafer. This results in an emitter recombination current of about 25fA/cm², according to [25].

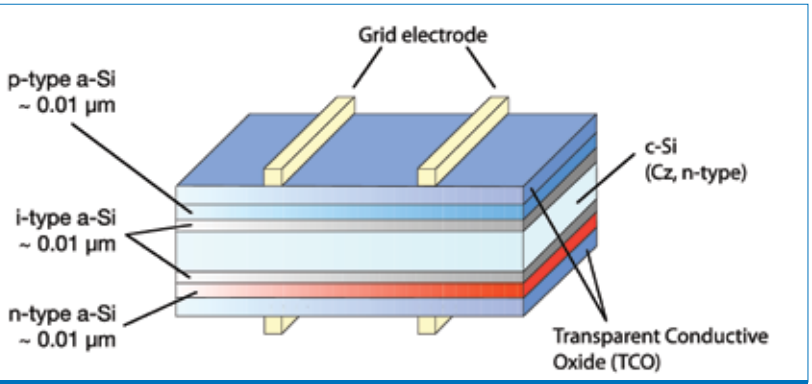

Figure 14. Structure of HIT cell.

The silicon heterojunction solar cell in principle requires only a doped amorphous silicon layer on the silicon wafer. Typically an n-type monocrystalline wafer will be used for its high lifetime to get the most from the high-efficiency capability of the cell structure. This means that the emitter will be based on a p-type amorphous silicon layer. Other layers, such as microcrystalline silicon and silicon carbide, have also been investigated for emitter layer. Sanyo has demonstrated that incorporation of an intrinsic (undoped) amorphous silicon buffer layer between the wafer and the p-type doped film is very beneficial in increasing the passivation, and thus the V_{oc} and cell efficiency. This approach named the heterojunction with intrinsic thin layer (HIT) technology.

As Sanyo's patent on the use of an intrinsic buffer layer will expire in a few years, several companies, such as Roth & Rau, are gearing up to provide silicon heterojunction solutions to the PV industry. Kaneka (in collaboration with IMEC), and Jusung (in collaboration with INES) are also active in the development of silicon heterojunction technology.

The structure of the HIT cell as developed by Sanyo is shown in Fig. 14. It consists of a textured n-type wafer, coated on the front with ultra-thin i/p amorphous silicon layers, and on the back with ultra-thin i/n amorphous silicon layers. The lateral conductance of the inversion layer (emitter) and accumulation layer (BSF) in the wafer is low (sheet resistance of order kOhm), therefore the device is coated with transparent conductive oxide films (TCOs) on front and rear to enable carrier conduction to the metal grid. The TCO also functions as anti-reflection coating. An H-pattern metal grid is printed on the front and rear of the cell, while the a-Si layers are normally deposited by PECVD.

Sanyo has demonstrated efficiency of 22.8% on 100µm-thin wafers and Swanson [26] has estimated that without optical shadowing and absorption losses, the efficiency generic to the device concept is about 25%. Due to the very good surface passivation, the V_{oc} is also very high (well over 700mV). Other advantages include:

- low temperature coefficient of voltage, meaning good module performance at high ambient temperature;
- bifacial cell design, minimizing stress on wafer and allowing bifacial modules;
- low temperature processing.

Some potential disadvantages are:

- proprietary technology – only Sanyo has been able to exceed 20% efficiency;
- the need to use excellent surface preparation;
- the need to use low-temperature metallization, resulting in the need for special printing techniques and a larger amount of Ag used per cell.

Process technology for silicon heterojunction cells differs drastically from normal cell process technology. For good performance, suitable wet chemical preparation of the wafer surface is very important. Amorphous silicon thin films do not survive temperatures higher than 200 or 300°C, which means that the cell process has to be a low-temperature one. Specifically, this means that gettering or hydrogenation is not possible (making mc-Si unattractive as a substrate), and that a printed metal grid cannot be sintered. The conductivity of the metallization is therefore low, and very high aspect ratio lines are required on the front.

The critical aspects for device performance have only recently become somewhat better understood, and are still subject to much fundamental and applied research. The extraction of majority carriers through the p-type amorphous silicon has to deal with a large semiconductor band offset, and therefore tunnelling plays an important role. As a result, the thickness of the amorphous silicon has to be kept very thin [27]. Additionally, the p-type amorphous silicon is usually contacted by n-type indium tin oxide, which means the p-type a-Si must be highly doped to create sufficient V_{oc} [28]. Limiting optical absorption losses is another reason for keeping the a-Si layers as thin as possible, but regardless of this, their passivating properties have to be very good.

Recently, results have been reported of back junction, back contact devices based on heterojunctions [29, 30]. This very interesting development potentially offers the advantages of silicon heterojunction cells (high V_{oc}, very good surface passivation), without the disadvantages (optical losses in a-Si and TCO, need for high aspect ratio metallization). An example of such a device is given in Fig. 15.

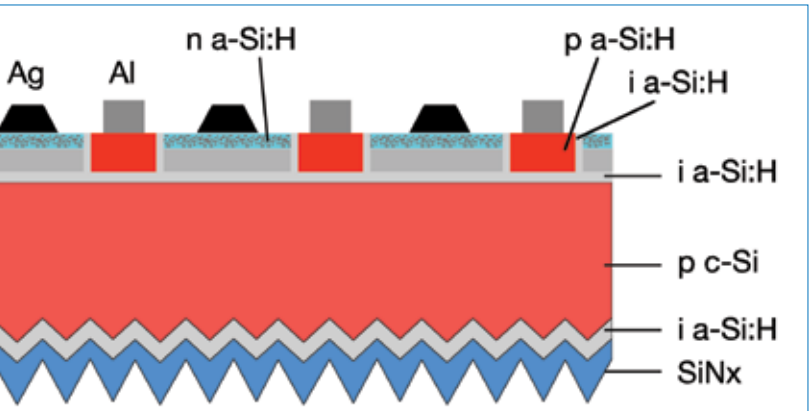

Figure 15. BEHIND cell, back junction, back contact heterojunction design [29].

Conclusions

Emitter quality to a large extent determines the efficiency potential of silicon solar cells. From a practical point of view, a high quality emitter is obtained when low recombination in the bulk of the emitter, a low-recombination interface with a coating, and a low contact resistance to the metal grid are combined.

Suitable and nearly ideal emitters can be made using the current industrial equipment – quartz tube diffusion furnaces, for example – but processes will have to be optimized more than is common in current industrial practice. However, for homojunction emitters, the requirement for low grid contact resistance will likely always mean a compromise with increased emitter recombination, whatever the method used to create the emitter.

For homojunction emitters, the metal contact requires a high surface dopant concentration. This is automatically provided during a standard emitter diffusion; alternative methods need special procedures to obtain this. This, of course, makes alternatives more complicated when applied to 'standard' cell concepts.

Because current emitter technology is already capable of near-ideal emitters, the benefit of alternative emitter processes, such as epitaxy, CVD, implantation, etc., will therefore have to be found to especially improve CoO or in practical advantages such as feasibility to make structured emitters.

For high efficiency concepts, there will be a need for interdigitated local emitters and local back surface field. This may favour new ways of providing dopants and alternative methods might also be introduced for these concepts.

The ultimate, ideal emitter will, apart from displaying very low bulk recombination, have a very well passivated interface to the contact, which contact should reflect minority carriers and extract majority carriers only. One of the closest known approximations to such an ideal emitter is the c-Si/a-Si/TCO heterojunction with intrinsic buffer layer.

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