In-line quality control in high-efficiency silicon solar cell production

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ABSTRACT

There are numerous tools and methods available on the market for the optical and electrical quality control of high-efficiency silicon solar cells during their industrial production, and even more are discussed in the literature. This paper presents a critical review of the possibilities and limitations of these tools along the value chain, from wafer to cell, in the case of passivated emitter and rear cells, as well as a discussion of some showcases. Economic and technological challenges and future trends are addressed.

Introduction

Within the PV industry, every player on the market faces fierce competition. Solar cell and module manufacturers aim at reducing their costs and the use of consumables, while at the same time improving throughput and uptime, yield, process stability, cell reliability and cell output power. In order to achieve higher solar cell output power, more and more cell and module manufacturers seek salvation in switching from conventional silicon solar cells with full-area aluminium back-surface field to passivated emitter and rear cells (PERCs), as the latter concept allows higher output power with minimum change to the production line. However, the higher potential of this type of device comes with a higher sensitivity to material and process variations. In order to better control these variations, as well as to find further potential for process improvements, an intelligent use of in-line characterization techniques should ideally combine the required investigation of material and device properties with real-time process and production control.

In-line quality control along the PERC value chain, from wafer to cell

From the point of view of a solar cell manufacturer, in-line quality control can be prioritized as follows. Solar cell manufacturers buy wafers, fabricate solar cells and finally sell them. The output power of the cells under standard test conditions is very important for establishing the price at which they are sold. Thus, in the first place, cell manufacturers need to measure the output power or energy conversion efficiency; consequently, a current–voltage measurement tool with a sun simulator at the end of the cell production line is indispensable. Next, the manufacturers want to get hold of inexpensive and high-quality wafer material, which can be tested either at the end of the wafer production line or at the beginning of the cell production line. A specific

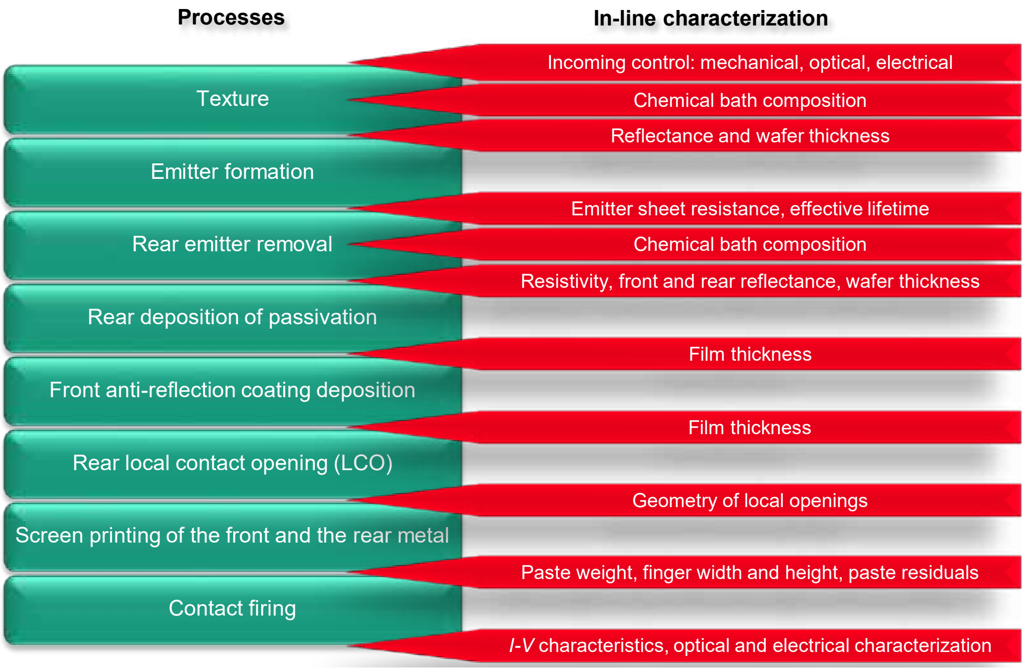

Figure 1. Simplified process flow typically used for the fabrication of PERC solar cells, along with important corresponding in-line characterization tasks.

type of incoming test is therefore also a high priority for cell manufacturers. During the production of solar cells, a high quality and stability of the individual process steps is required. For this purpose, many scientists and metrology suppliers have developed various methods and products that are available on the market, though little used in industry because of their obvious costs and arguable benefits.

> "A specific type of incoming test is a high priority for cell manufacturers."

A typical PERC manufacturing process will now be described and will cover the value chain from wafer to cell. Currently available tools for in-line quality control will be mentioned, and some examples of applications will be elucidated. Aspects of in-line quality control from crystallization and wafer manufacturing, however, are not discussed here but are covered elsewhere in the literature. The enumeration is not claimed to be comprehensive, but it certainly covers many important and interesting tools.

Process sequence

A simplified process flow for PERC cell production is shown in Fig. 1. First, the p-type mono- or multicrystalline wafers are wet-chemically textured. The n-type emitter is formed on the front and rear surfaces of the wafers in a diffusion oven. Prior to surface passivation, the rear emitter is typically wet-chemically removed, followed by a cleaning step. The passivation of the rear surface is realized, for example by an aluminium oxide (Al_2O_3) layer deposited by fast atomic layer deposition (ALD). A silicon nitride (SiN_y) layer serves as the capping layer on the rear. As regards the front surface passivation, typically a plasma-enhanced chemical vapour deposition (PECVD) SiN_x layer is used. The rear passivation layer stack is locally opened, for example by ablation using a laser process in order to obtain line-shaped local contact openings (LCOs). The front- and rear-side metallization is applied by screen printing. Finally, the contact firing is performed, for example in a conveyor belt furnace.

Incoming control

The high electrical and mechanical quality of wafers can be checked during the incoming inspection in solar cell production or during the final inspection in wafer production. Poor-quality wafers should be identified and discarded at an early stage in the process in order to avoid unnecessary costs. The wafer properties that are accessible in line are: the wafer thickness and its variation, the wafer size and geometry, and the extent of saw marks and roughness, chipping, holes and cracks. The electrical properties are: base resistivity, effective lifetime and crystal defects. In addition, surface contamination and reflectivity are optical properties that are worthy of investigation. Recent SEMI standards cover the measurement of most of these properties.

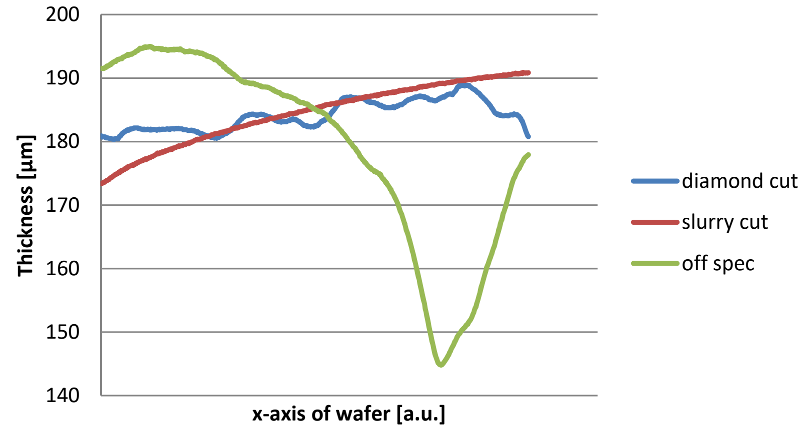

Figure 2. Three examples of thickness profiles. The diamond-cut wafer shows a typical large-scale saw-mark structure, the slurry-cut wafer shows a strong gradient, while the off-spec wafer shows a very distinct saw mark.

The measurement of wafer thickness is typically capacitance based. Tools measuring, for example, three traces with several hundreds of measurement points each allow the detection of not only the mean thickness (typically ~180µm), but also the total thickness variation (~20µm) and more details about the wafer shape. Slurry-cut wafers have a thinned edge, and whether this plays a role during production is worth investigating. Diamond-cut wafers, on the other hand, can have a specific large-scale saw-mark structure which might cause problems during screen printing (Fig. 2). Wafer size and geometry are identified using line or matrix cameras and are important parameters for machine alignment and handling tolerances. Special care needs to be taken as wafer sizes go up from 156.0 to 156.75mm or even further.

The presence of smaller saw marks and roughness with a spatial resolution of few micrometres can be determined using laser triangulation. We have seen no correlation of these parameters with the final solar cell results or with the manufacturing process, and therefore question the importance of such data. Chipping and edge-defects can be identified with high-resolution imaging, but automatic image processing can be problematic for wafers with strong grain contrasts or differences in reflectivity. Large and even small cracks, with lengths of a few millimetres and widths below a micrometre, can be detected using, for example, infrared transmission, infrared reflectance and photoluminescence images. In the case of monocrystalline material, the automated identification is relatively simple; in contrast, for multicrystalline material, advanced algorithms are required because of the muddled contrast between the grain boundaries and the dislocations [1]. The assessment of the criticality of a crack in the as-cut state and later process steps in terms of wafer breakage [1], solar cell efficiency losses and module hot-spot danger [2] is crucial for wafer, cell and module manufacturers.

Optical inspection using line or matrix cameras can reveal staining, residuals from cleaning, or other surface contaminations; although this method works well for slurry-cut wafers, the use of the same set-up for diamond-wire-cut wafers is not straightforward. The reflectivity of the wafers can be measured by means of a spectrometer. Since the reflectivity strongly depends on the cutting of the wafers, it can be used as a quality

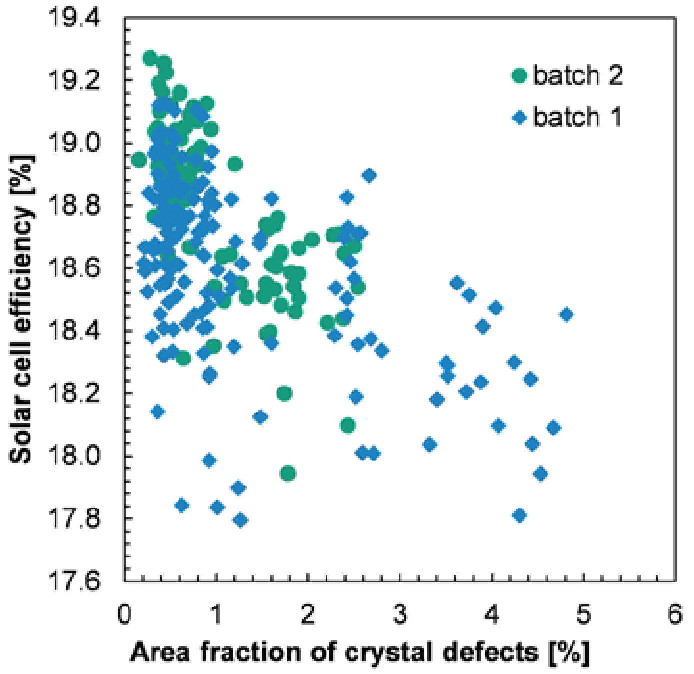

Figure 3. The solar cell efficiency of two mc-Si PERC batches is limited by the area fraction of crystal defects, here measured via photoluminescence on the as-cut wafers. Further variations in wafer properties and processes induce more efficiency variations.

parameter. In addition, reflectivity is an input parameter for the calibration of all optical detection methods that use cameras for detection or lasers for excitation.

The resistivity of the wafer is typically measured via inductive coupling: several traces with hundreds of measurement points each can be implemented. There are two obstacles when dealing with the resistivity measurements – one concerning monocrystalline silicon and the second concerning multicrystalline silicon. In Czochralski-grown monocrystalline silicon wafers, thermal donors can be formed during crystallization, depending on the oxygen concentration and thermal treatment. During heat treatments above 500°C, such as during emitter formation, these thermal donors are dissolved; hence, the resistivity measured in the as-cut state is higher for p-type and lower for n-type wafers than the actual value after thermal donor dissolution. Thermal donors therefore hinder the precise calculation of the emitter sheet resistance by combining the resistivity measurement in the as-cut state with a later measurement after

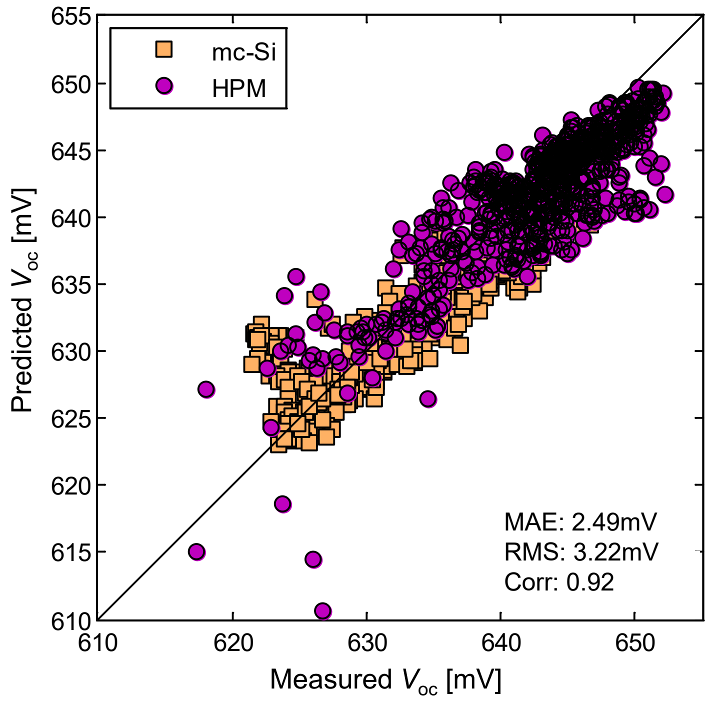

Figure 4. Predictions of the open-circuit voltage V_{oc} for more than 1,300 PERCs (adapted from [9]). The results are obtained using a regularized regression model based on empirical data, and are shown for conventional multicrystalline silicon (mc-Si) and high-performance mc-Si (HPM) wafers. The graph presents the evaluation, with the most challenging prediction of 'unknown' material shown for two unknown manufacturers whose material was not included in the training set. The approach performs well in predicting PERC data (mean absolute error MAE of 2.49mV, root-mean-square-error RMS of 3.22mV, Pearson correlation coefficient of 0.92).

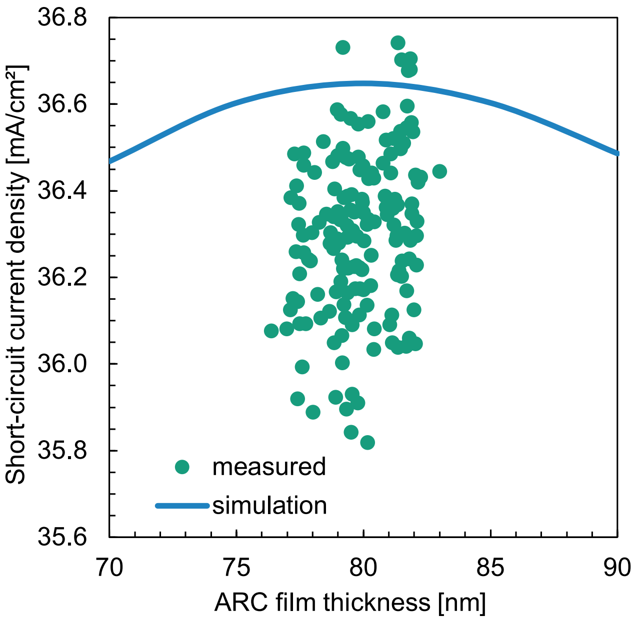

Figure 5. For these multicrystalline PERC cells, the ARC was deposited with a thickness ranging from 75 to 85nm. This variation does not degrade the short-circuit current density because of the surface texture and the very small thickness variation. From a simulation, a J_{sc} variation induced by the ARC thickness of less than 0.05mA/cm^2 is expected; the actual variation observed is mainly caused by other effects.

emitter formation; however, this can be overcome using photoluminescence imaging [3]. For multicrystalline silicon, potential barriers are formed at grain boundaries after wet-chemical treatments of the wafer and are annihilated by thermal processes, such as during emitter formation. These potential barriers increase the apparent resistivity [4]. The emitter sheet resistance should therefore be calculated by combining the resistivity measurements in the as-cut state and after emitter formation.

The bulk lifetime of minority-charge carriers is one of the most important parameters for characterizing the electrical quality of wafers. Unfortunately, in the as-cut state only an effective lifetime can be measured, which is severely limited by surface recombination and thus does not allow a correlation with the final solar cell parameters. Only wafers with very low lifetimes (e.g. as a result of crucible contaminations) can be identified and sorted out. Nevertheless, lifetime measuring systems based on microwave-detected photoconductivity (MPD) [5], microwave-detected photoconductance decay (MW-PCD) [6] and quasi-steady-state photoconductance (QSSPC) [7] measurements are available. To overcome the surface recombination limitation, the lifetime can be inspected at later process stages (e.g. after passivation).

For multicrystalline wafers in particular, crystal defects in the form of dislocation clusters can be detected with photoluminescence (PL) imaging [8], despite the high surface recombination; the technique shows the distribution of defects that severely degrade the lifetime. Such defects are detrimental to solar cell performance, as the example in Fig. 3 shows: maximum efficiencies decrease with increasing area fraction of crystal defects. (It will be seen later, in Fig. 6, that these crystal defects partly stay present during solar cell processing and reduce the efficiency of the finished cells.)

This correlation between defects and efficiency, along with the other data from the incoming inspection, can be utilized to set up a powerful prediction of solar cell efficiency, as shown in Fig. 4 [9]. Metrology suppliers are working on such prediction models for production lines, which is very difficult because prediction results are highly dependent on the solar cell process and are distorted by processing fluctuations. With Cz wafers, ring-like

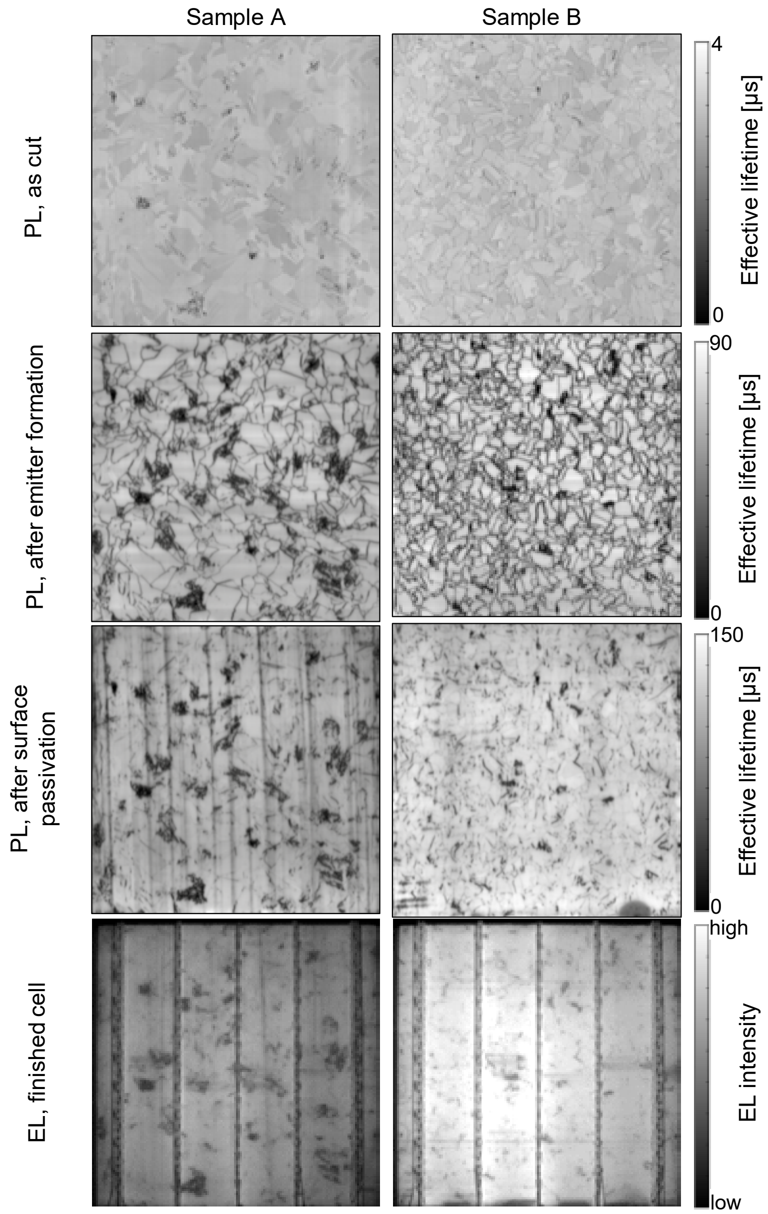

Figure 6. Photoluminescence (PL) and electroluminescence (EL) images of two multicrystalline samples at different stages of the PERC production sequence. In the as-cut state, dislocations and grain boundaries are visible and become even more pronounced after emitter formation. Following surface passivation, the grain boundaries are not clearly visible in both samples, but line-shaped defects (possibly induced by saw marks) become apparent in sample A only. In the finished cells, several material- and process-induced defects (possible saw marks, crystal dislocations, finger interruptions, edge shunts) are superimposed.

features may be detected: these are caused by thermal donors and might hint at efficiency-limiting oxygen-induced stacking faults [10].

Production processes

In-line quality control at an intermediate point between the incoming test of the as-cut wafers and the outgoing test of the finished solar cells is not believed to be very widespread. It is nevertheless a prerequisite undertaking in order to quickly detect problems that arise during production and to constantly achieve high solar cell conversion efficiencies, and one which increases in importance as the efficiency increases.

During the texturing, the concentration of chemicals in the bath can be continuously controlled using near-infrared spectroscopy. Acidic (HF, HNO_3) and alkaline (KOH, organic additives) baths that are typically used in silicon photovoltaics have been analysed [11–15]. After the texturization process, the reflectance of the wafer and its thickness can be measured and used to control the quality of the light-trapping properties and of the silicon removal respectively.

Many of the following methods require a combination of several measurements (e.g. resistivity and wafer thickness, or resistivity as-cut and after diffusion); thus, the data need to be attributable to specific individual wafers. For this purpose, methods for tracking a single wafer (e.g. using data-matrix codes) have been developed [16–18].

After the emitter formation, the resistivity can be measured and used to calculate the emitter sheet resistance. Care has to be taken in case of potential barriers at the grain boundaries in multicrystalline silicon [4], and because of thermal donors [3], as discussed above. Similarly to the as-cut state, inductive methods can be applied, but infrared techniques too are beneficial. The effective lifetime can be measured after the emitter formation, again using the same techniques as for the as-cut wafer; this is recommended in order to detect severe degradation of the bulk lifetime due to the high temperatures and large thermal budget required for emitter formation. Especially for Czochralski-grown silicon, the formation of oxygen-induced stacking faults can significantly reduce solar cell efficiency [10]. Relating the effective lifetime after emitter formation to the I–V parameters of the final cell (i.e. open-circuit voltage V_{oc} and efficiency η) is more meaningful than in the as-cut stage because of an active field-effect passivation from the emitter; however, the procedure is not straightforward.

After emitter removal on the rear side, the reflectance on the front of the wafers can be measured in order to track any wrap-around and the related degradation in texture quality. Likewise, the rear-surface reflectance can be used to track the rear-surface roughness, which is important in terms of the achievable rear-side passivation quality. Measuring the wafer thickness enables the silicon removal to be controlled. In the case of asymmetric emitter formation, for example caused by different surface structures or back-to-back boat loading, it is of interest to determine the emitter sheet resistance.

After the deposition of the thin

dielectric films on the front and rear sides of the PERC cells, the film thicknesses can be determined from reflectance measurements [19] or by colour inspection. In the case of the front-side anti-reflection coating (ARC) shown in Fig. 5, the film thickness was deposited within a sufficiently small range to not degrade the final cell *I–V* parameters.

The samples can be weighed before and after screen printing of the front and rear metal, to determine the amount of silver and aluminium paste deposition. By optical inspection after screen printing, the finger width and paste residuals, as well as other grid defects, can be determined. The large contrast between the highly reflective front metal and the highly absorptive active cell area makes it challenging for in- and off-line 2D vision, and in particular for 3D vision, to determine the finger height [20].

Finished solar cells

After contact formation (i.e. when the cell is finished), extensive in-line characterization is available. Line or matrix cameras are used in visual inspection of the front side of the cells for detecting paste residuals and chipping defects, for measuring the finger width and cell dimensions, and for determining the colour of the ARC [21]. By inspecting the rear of the PERC cells with full-area Al print, the darkening of the aluminium at the LCOs caused by silicon alloying during the contact formation can be detected; this can in turn be used to detect inhomogeneous formation of the local back-surface field. In the case of bifacial solar cells, the visual inspection of the cell rear is in principle the same as that of the cell front: paste residuals, chipping, finger width and colour can be detected.

> “The most important in-line characterization for finished solar cells is without doubt the measurement of the *I–V* characteristics under standard test conditions.”

The most important in-line characterization for finished solar cells is without doubt the measurement of the current–voltage (*I–V*) characteristics under standard test conditions (STC: 25°C, 1000W/m^2 illumination with AM1.5g spectrum); from this the energy conversion efficiency can be deduced and the cells can be sorted into the corresponding bins. The choice of calibration can have a significant impact on the measured values of short-circuit current and conversion efficiency [22]. Besides these measurements under constant illumination, the suns-V_{oc} characteristic can also be measured, as well as the forward and reverse *I–V* characteristics in the dark, which together allow a basic analysis of series resistance, ohmic and non-linear shunting, and hot-spot danger.

Besides the measurement of the *I–V* characteristics of the solar cells, there are upgrades available for the *I–V* testers. By measuring the resistance from one busbar to another, the resistance of the metallization can be determined in order to track the stability and quality of the front and rear printing steps. In-line measurements of the quantum efficiency or spectral response of the solar cells are offered, which allow losses occurring in the emitter to be distinguished from those occurring in the bulk and at the rear of the devices. Electroluminescence (see Fig. 6) and photoluminescence imaging allows the detection of cracks, finger interruptions and dark areas [23]. It will be interesting to see if advanced luminescence methods (e.g. [24–27]) with additional benefits can be implemented in-line in the future. Thermography is used to determine hot spots of the cells and to predict possible module hot spots locally [28–31]. Such a local analysis is preferable to an analysis of the global dark reverse current, because inhomogeneous reverse current and power dissipation within the cell is the norm, not an exception. This is highlighted in Fig. 7, where the thermography image of an mc-Si PERC cell shows a significant increase in temperature after only 40ms, which is likely to damage the module. Since the cell’s reverse current at −12V is below 2A, this hot-spot danger cannot be predicted from the *I–V* characteristics.

The addition of more and more measurement tools to the cell tester means that the automat’s footprint becomes larger, and that potentially more than one contacting unit with a corresponding power supply

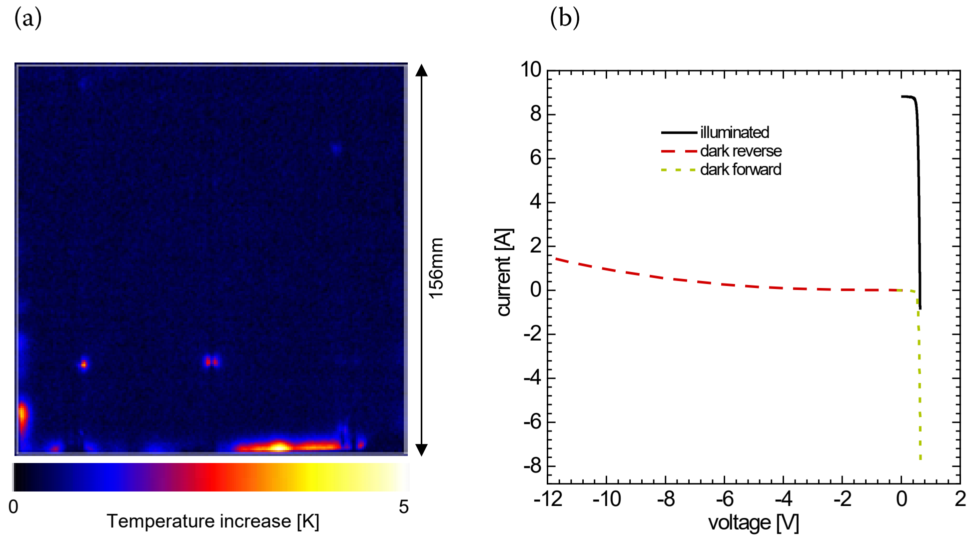

Figure 7. (a) Thermography image of an mc-Si PERC cell with a severe temperature increase of up to 5K after applying a reverse voltage of −12V for only 40ms, indicating hot-spot danger for the module. (b) *I–V* characteristics of the same cell, showing a moderate reverse current of less than 2A at a reverse voltage of −12V.

is required. Since this implies additional cost, the metrology suppliers are seeking to reuse the same hardware several times. However, when several measurements are combined within a single tool, the fraction of cycle time available for each measurement clearly decreases, implying that capacitive effects [32] and methods to deal with them [33] become increasingly important. For example, it is recommended to correct for capacitive effects when decreasing the measurement time for the *I–V* characteristics significantly below 40ms, and when increasing the open-circuit voltage of the cells above approximately 650mV.

Typical sorting criteria used to define the bins are: 1) the energy conversion efficiency or cell output power; and 2) the current at the maximum power point. The former is preferred by cell manufacturers (since a higher cell efficiency attracts a higher price), whereas the latter is favoured by vertically integrated cell and module manufacturers (since mismatch effects in the module can be minimized). Cells may also be sorted out on the basis of hot-spot danger or the presence of cracks.

Assessing the economic profitability of in-line characterization in production

When cell and module manufacturers are faced with decisions on whether to invest in advanced in-line characterization techniques, the first thing they want to know is the expected return on investment. In real production environments, parameters such as the uptime or the yield of a production tool are randomly influenced by failures, consumables and wafer quality, as well as other factors. It therefore often seems unclear how to distinguish between the positive effects of in-line quality control and the other factors affecting the performance of a production tool. This lack of clarity makes it difficult to appropriately prepare an investment decision for an in-line characterization technique.

To better understand the economic impacts of an integration of in-line characterization techniques into a production environment, a 500MWp/year monocrystalline PERC cell production process was simulated and examined using Fraunhofer ISE's cost of ownership (COO) calculation tool 'SCost' [34,35]. A calculation was made of the essential productivity improvement (in terms of cell efficiency gain) for the cell manufacturer with respect to the projected capital expenditures (capex) on in-line characterization in the production line – in other words, how much capex can be spent to break even with regard to the expected production performance enhancement.

For this analysis, the assumptions are a depreciation period of five years for the production equipment, and in-line characterization technique and wafer and module production costs of €ct78.8/wafer and €58.37/module, respectively. Moreover, it is assumed that uptime, production yield and line throughput are not influenced by the application of the in-line characterization technique.

Fig. 8 shows the resulting break-even analysis based on the Wp-cost equivalence before and after the application of the in-line characterization techniques. Since the advantage of a higher cell efficiency rises along the PV value chain, the analysis was done for the value chain stages by considering: 1) only the net costs of the cell production – excluding (for example) wafer costs – referred to as *net cell production costs*; 2) the costs of the cell production – including wafer costs, selling, general and administrative expenses (SG&A), and capital costs of the company – referred to as *all-in cell costs*; and 3) the all-in cell costs plus the corresponding costs for module manufacturing, referred to as *all-in module costs*.

The analysis shows that a capex spending of €250,000 for in-line characterization equipment is justified for a cell manufacturer if, immediately after its application for the time of usage (here five years), a mean cell efficiency increase from 20.614% to 20.657%, or $0.043\%_{\text{abs}}$, can be exceeded.

In the case of a vertically integrated cell manufacturer, or a cell manufacturer that has appropriate bargaining power with its customers (the module manufacturers), the module Wp costs instead of the cell Wp costs are preferably used for assessing investment decisions. For the break-even analysis in Fig. 8, it is seen that the capex spending of €250,000 is already justified for a cell efficiency increase of $0.026\%_{\text{abs}}$ from the reference efficiency of 20.614% to 20.640%.

If, by using the in-line characterization technique, the cell manufacturer realizes a higher cell efficiency increase than that stated above, the all-in cell (all-in module) costs decrease compared with the reference values. This influence of cell efficiency enhancement on the all-in cell costs is analysed in Fig. 9: the cell costs of a reference Cz PERC cell line (red line) are compared with four different Cz PERC cell lines (blue dashed lines) equipped with additional in-line characterization techniques at additional costs of €50k, €100k, €250k and €500k, respectively. It can be seen in this figure that the intersections of the reference cell cost line (black horizontal line) with the blue dashed lines mark the break-even points, which are also shown in Fig. 8. For each of the equipped cell lines, the cell efficiencies exceeding the values marked by the vertical lines lead to lower cell costs compared with those for the reference cell, as a result of the application of in-line characterization techniques.

This finding shows just how small the efficiency increase needs to be to justify in-line metrology; however, it also suggests, in general, the importance of the demonstration of such a cell efficiency increase induced by in-line control in order to prepare a clear and transparent investment decision regarding in-line control techniques. As noted previously, however, production parameters are strongly interlinked, and therefore economic investigations of the effects of in-line control on uptime, production yield, and so on should be carried out specifically for a dedicated application.

Challenges and future trends

In general, the most challenging question for cell manufacturers and metrology suppliers concerning in-line metrology relates to which tools and methods are required and economically advisable. A core question is how to control and improve the yield, the reliability, the

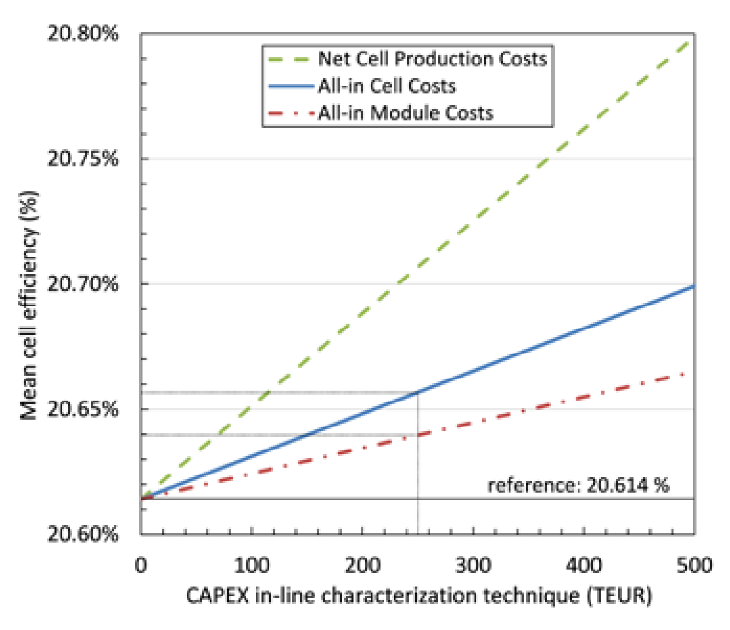

Figure 8. Break-even analysis of an in-line characterization technique, integrated into a 500MWp/year monocrystalline PERC cell production line. For the 'net cell production costs', the 'all-in cell costs' and the 'all-in module costs', the three lines indicate the respective gain in mean cell efficiency to be reached by the characterization technique in order to break even in respect of the additional expenditure for the characterization technique. These break-even points are calculated for a Wp-cost equivalence of a cell line without the characterization technique (the reference), and of a cell line enhanced by a characterization technique with a depreciation period of five years.

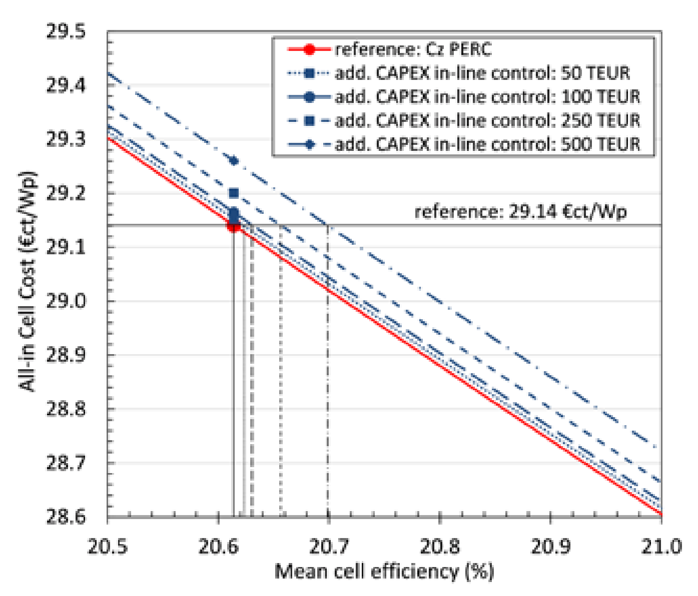

Figure 9. Sensitivity analysis of the mean cell efficiency influence on 'all-in cell costs' (including wafer, SG&A and capital costs). The red line shows the costs associated with the Cz PERC reference cell, and the red dot indicates the reference cell efficiency of 20.61%. The dashed blue lines represent the costs including the additional capex for in-line characterization. All figures are calculated for a 500MWp/year monocrystalline PERC cell production.

mean cell efficiency and the scattering of the efficiency distribution, and at what cost. Metrology suppliers have to demonstrate the benefits of their tools, either in the labs at research institutes (as in the Photovoltaic Technology Evaluation Centre PVTEC at Fraunhofer ISE) or directly in the industrial application. There are scientific approaches for identifying the stage of the production chain at which more quality assurance is advisable [36]. Giving feedback during or directly after a particular process step is clearly desirable, though not comprehensively possible, because the quality of a process may depend on, or may be assessed only after, subsequent processes. As regards the cost aspect, less expensive and more versatile metrology tools are required.

> "Less expensive and more versatile metrology tools are required."

From a technological point of view, there are several challenges at present. Thermal donors hinder the precise determination of the base resistance and hence of the emitter sheet resistance. The approaches discussed above to address this issue need to be improved and implemented. Another challenge is how to deal with the highly reflective surfaces of diamond-wire-cut wafers in the inspection tools.

Since imaging in-line metrology is still a young field, there are several challenges which have to be overcome. The image data need to be reduced, defects need to be detected reliably, and both robust and sensitive sorting criteria need to be derived; only then can the imaging metrology deliver its maximum potential benefit. Specifically, crack detection in photo- and electroluminescence images, for multicrystalline silicon wafers and cells in particular, needs to be improved. In addition, metal finger interruptions need to be reliably detected. With the growing interest in PERC cells, several challenges specific to this cell concept have arisen.

The first difficulty lies in separating the front and rear defects. In the electroluminescence image, for example, there are visible contrasts which might originate either from interruptions of the metallization fingers on the front side, or from incomplete formation of the back-surface field of the line-shaped rear contacts. Because of the preferred printing direction, the front fingers and rear LCOs are aligned with one another, provided the samples are not rotated after the rear-side printing step.

A second PERC-specific metrology task is the thickness determination of the passivation stacks. The thicknesses of the individual films can be determined separately from reflectance or ellipsometric measurements [37].

To the authors' knowledge, no tool currently exists for the in-line quality control of LCOs with typical dimensions below 50µm on the whole wafer, which presents a third PERC-specific challenge. The future will show whether the openings will need to be controlled as more and more PERC cell manufacturers enter the market.

After the introduction of monofacial PERC cells into industrial production, the likely next step will be to apply an aluminium grid instead of a full-area metallization at the cell rear, and hence convert the device into a bifacial solar cell with a potential increase in electricity yield. For this concept, the measurement of the *I–V* characteristics is again the biggest issue from the metrology point of view. It is not yet clear, either for calibration laboratories or for industrial production, whether it is sufficient to illuminate the samples from one side only, or whether this needs to be done from both sides separately or from both sides simultaneously. The construction and design of the measurement chucks, and especially the reflectivity in the infrared region, are of particular interest when measuring and reporting *I–V* data of bifacial cells. The rear inspection and the separation of front and rear defects (paste residuals, finger thickness and interruptions, etc.) are further issues to be addressed in the case of bifacial cells.

After the rear of a silicon solar cell has been improved by introducing the PERC concept, it is likely that the front of the cell will limit the conversion efficiency. Consequently, another probable step to be taken is to implement a selective emitter, which has already been discussed a couple of years ago [38]. As the highly doped structures and the metallized structures become ever narrower, the process stability and its precision must increase adequately. In order to align the highly doped structures and the metal grid, it is certain that new solutions and more quality control will be required.

Only time will tell if the currently hyped trend of 'Industry 4.0' will in fact become established, or if it will disappear into oblivion. It is certain, however, that intelligent machines and tools talking to and interacting with each other lead to improved quality and reduced cost. A prerequisite for this is the collection of data by in-line metrology tools, but the possible growth in in-line metrology will not happen on its own – it has to be elaborated step by step.

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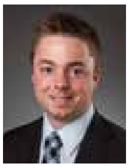

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