Solving all bottlenecks for silicon heterojunction technology

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Abstract

Silicon heterojunction (SHJ) solar cells are the archetypes of 'full-surface passivating contact' solar cells; such contacts are required in order to achieve typical open-circuit voltages of up to 730–750mV. Although SHJ technology has fewer manufacturing steps and enables higher efficiencies than standard passivated emitter and rear cell (PERC) technology, the market has been slow in taking it up. This paper discusses some of the obstacles that have been overcome in the last 10 years, and shows why the technology is now readier than ever for a competitive mass-market launch. The reasoning behind this is based on: 1) improvements at the solar cell level, leading to >24–25% efficiencies in R&D, with screen-printed contacts; 2) the availability of high-quality, low-cost, thin n-type c-Si wafers; 3) improvements in metallization and interconnection solutions; and 4) the availability of cost-effective mass-production tools. Many research groups and industries currently demonstrate R&D 6" cells that typically reach 23–24% efficiency. Several new manufacturing or demonstration lines with production tools are in operation, running on average 24-hour production of 6" cells with an efficiency level of 23% (five busbars). When the excellent temperature coefficient and bifaciality of the modules are taken into account (leading to more kWh per nominal W), SHJ has the potential to outperform traditional technologies in terms of electricity cost. However, the CAPEX is still significantly higher than that for PERC lines and creates a hurdle when growth in capacity (MW/year) is favoured for a given capital. This paper indicates how it should be possible to further reduce manufacturing costs once a true volume learning curve is started, by acting both on the CAPEX and on the costs of consumables, in particular silver and indium, on which today's popular transparent electrodes are based. Finally, there will be a brief discussion of how the technology could be upgraded, either to full back-contacted approaches or to multijunction structures, forming a natural extension to the PV learning curve.

Introduction

Silicon heterojunction (SHJ) cell technology is based on the simple structure and typical processes illustrated in Fig. 1; it aims to take the best of both the c-Si world (perfect absorber) and the thin-film world (coatings on large area). After initial developments by various research groups, Sanyo (now Panasonic) introduced the heterojunction concept for the a-Si:H(i/p)/TCO front stack and rear n^+/Al back side [1,2]. A few years later, IMT Neuchâtel's PV-Lab introduced a rear side with a-SiH(i/n) and transparent conductive oxide (TCO) [3]. Sanyo was the first to push the concept to large-scale manufacturing, and demonstrate high-efficiency solar cells. A review of the key elements of the technology can be found in recent papers [1,4].

"State-of-the-art n-type c-Si wafers no longer require gettering or thermal donor killing to enable high-efficiency cells to be fabricated."

In the last decade, an increasing number of research groups and companies have been working at industrializing various versions of the technologies [5–10]. In line with expectations, in terms of production cost for current manufacturing [11] several obstacles remained, precluding a full mass introduction. Some of these are described below, along with how they have been overcome just recently, which explains the high number of new players in the field of SHJ cell manufacturing.

Material quality

For a long time, access to high-quality n-type wafers was costly. In consequence, additional processing – such as gettering, thermal donor killing or hydrogenation – was required in order to obtain sufficient material quality for high-efficiency solar cell production. Today, however, the situation is different. In step with the improvement in quality of p-type wafers, the quality of n-type wafers pulled using the standard Czochralski (Cz) method has significantly improved over the last five years. This advance has stemmed from better control of the oxygen content as well as from optimized pulling techniques, with faster cooling allowing a reduction in thermal donor concentration. As a result, state-of-the-art n-type c-Si wafers no longer require gettering or thermal donor killing to enable high-efficiency cells to be fabricated. This has been demonstrated by values of the lifetime/resistivity ratio (typical quality criteria with lifetime expressed in ms and resistivity in Ωcm) greater than unity along the entire ingot [12].

For a thickness of 180μm, such n-type wafers are now typically 5–8% more expensive than p-type [13]. The difference compared with p-type essentially arises from the limited number of pullings (e.g. three instead of five) using the same crucible; fewer pullings can be made to avoid

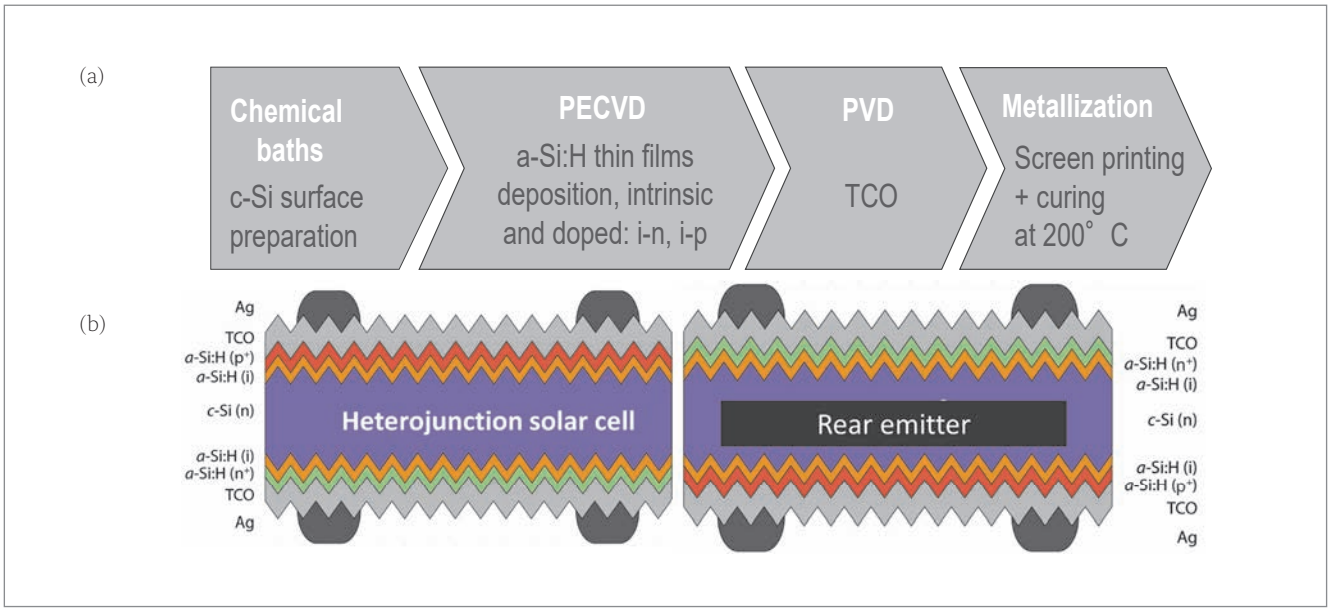

Figure 1. (a) A typical process flow for standard SHJ. The plasma-enhanced chemical vapour deposition (PECVD) and physical vapour deposition (PVD) steps on both sides can each be performed in a single tool. Alternatively, catalytic (CAT)-CVD and plasma-assisted evaporation (PAE) can be used for the deposition of a-Si:H and TCO layers respectively. (b) Schematics of the front-junction (left) and rear-junction (right) configurations. Note that in both cases, providing that high-quality surface passivation and low local contact resistance are obtained, the sheet resistance of the TCO is not as crucial as in, for example, thin-film modules, because of the high injection of charge carriers under operating conditions that contribute to lateral charge transport.

excess (metallic) impurities which accumulate in the melt, and which cannot be gettered during the low-temperature SHJ process.

In the case of SHJ technology, on the other hand, the low-temperature and stress-free processing make it easier to handle thinner wafers than with standard silicon technology. Moreover, the efficiency is independent of the wafer thickness down to around 100µm: the short-circuit current (J_{sc}) loss due to the thinner wafer is compensated by an open-circuit voltage (V_{oc}) gain, enabled by the ultralow surface recombination. This characteristic is illustrated in Fig. 2, which shows the efficiencies of SHJ solar cells from the CEA-INES pilot line. Note that for 'standard' technologies with lower V_{oc}, due to a poorer surface passivation, the situation is different, as current losses are not compensated by V_{oc} gains. At the moment, wafer producers are able to offer a price reduction of 1.2–1.5¢/wafer per 10µm of thickness reduction [13]. A 130–140µm high-quality n-type wafer is therefore available at the *same price as (or an even lower price than)* 170–180µm high-quality monocrystalline p-type wafers used for passivated emitter and rear cell (PERC) production.

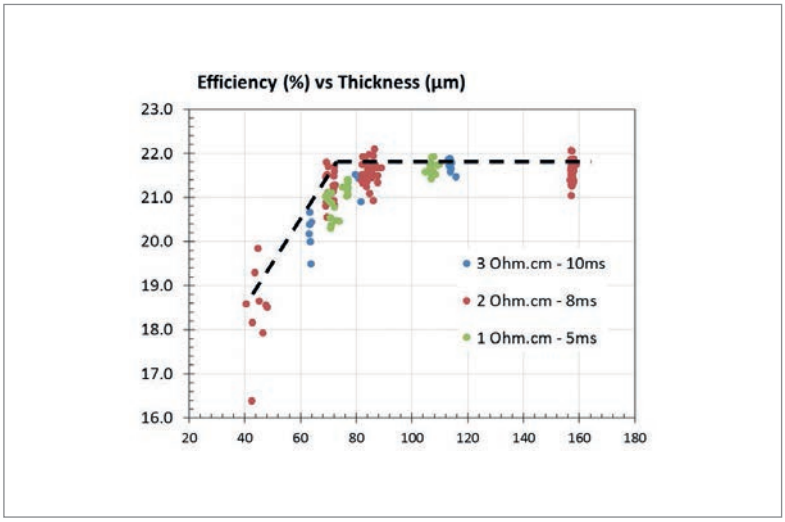

Figure 2. Illustration of SHJ cell efficiency as a function of the wafer thickness for devices made on the CEA-INES pilot line. There is no efficiency loss for wafer thicknesses down to 100µm. The efficiency reduction at a lower thickness is linked to surface and handling processing issues for thinner wafers (which could still be optimized).

Metallization and interconnection

Two reviews of metallization and interconnections for heterojunction technology were given by Geissbühler et al. [14] and Faes et al. [15]; some of the key elements are summarized here.

- Ten years ago, the first low-temperature pastes (annealed at typically 200°C) had limited conductivity (resistivity as high as 20µΩcm), and two- or three-busbar cells needed high volumes of Ag paste. Thanks to the developments by paste manufacturers, there has been a big improvement in low-temperature Ag pastes, with resistivity down to 5–6µΩcm, bridging the gap with high-temperature pastes (demonstrating a typical resistivity of 3µΩcm).
- Additionally, SHJ benefits markedly from the multi-busbar approach (five busbars as a first step, but ideally eight or more), which can be implemented by either gluing or soldering the ribbons. In respect of more advanced solutions, multiwire (equivalent to >15 'busbars') approaches are highly attractive (Fig. 3(a)), as they allow even lower Ag paste consumption, with effective finger lengths shorter than 5mm.

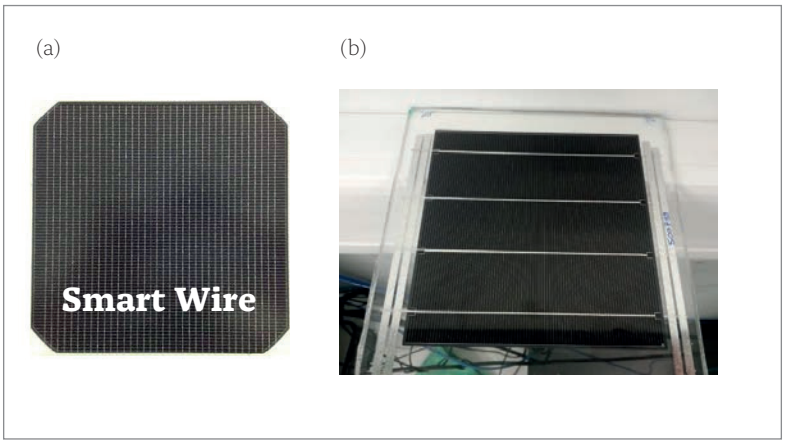

Figure 3. (a) New-generation Smart Wire Connection Technology (SWCT), enabling effective finger lengths of <5mm. (b) Cu-plated four-busbar SHJ solar cell produced at CSEM, with a certified efficiency of 24.15% (designated area efficiency, for an area of 225cm^2).

"SHJ technology has the lowest number of process steps."

- Alternatively, one can replace Ag by copper plating; several groups and companies have reported excellent results with plating [14,16–18], as illustrated in Fig. 3(b). Such approaches can be combined with shingling approaches with a limited number of cuts (one to three cuts per cell), noting that the front TCO acts as an excellent barrier to copper.

As an example, the smart-wire approach (Fig. 3(a)) is typically based on 18 to 24 wires, with a diameter range of 250–300μm, attached to a thin, highly transparent carrier foil [19]. This geometry allows a minimum amount of printed Ag paste for the front and rear metallization (25–45mg per side, with the possibility of reducing this to 10mg [20]). This 'soft' process does not lead to microcrack generation, even with thin wafers. Modules based on this technique have frequently passed all accreditation tests [21]. Remarkably high module fill factors in the range of 80% (Fig. 4) are made possible, and the technique should currently allow the lowest total cost for the metallization and interconnection of SHJs [15].

In conclusion, certified and reliable metallization and interconnection approaches with inexpensive materials are now available. Further advantages are discussed later in this paper.

Heterojunction process simplicity

The SHJ process has had the reputation in the past of being difficult to control, as it is based on equipment and processes that are not familiar to

the traditional c-Si community. The mindset is changing, however, since there are many arguments to demonstrate the simplicity and ease of control of this process. The following points are worth noting:

- From the thin-film solar, flat-panel display and glass-coating industries, low-cost coatings per m^2 have been achieved for PECVD (e.g. from industrial parallel-plate reactors handling, in parallel, 10 plates of 1.4m^2 [22], or of even up to 5.6m^2 [23]), as well as for sputtering (PVD), e.g. through more and wider-band magnetrons.

- SHJ technology has the lowest number of process steps – five to seven, depending on the tools and processes.
- It is possible to precisely control the homogeneity of the thin layers with good tool design, and the process can be made robust against, for example, layer thickness variations [24].

- There are now at least 20 research institutes and pilot or production lines demonstrating efficiencies above 23% as baseline efficiencies for cells on 6" wafers. Lab records reaching 25.1% for two-side-contacted devices have been reported, and up to 26.7% for interdigitated back contact (IBC) configurations [25,26]. Some reference values are given in Table 1.

In the authors' experience, a well-configured set of tools can already produce efficiencies above 22% in the initial processed cells, and a continuous process improvement taking advantage of the

Figure 4. A 72-cell (M2 wafers) module with 412W. The measured *FF* is 80.18%, with a front-side aperture area efficiency of 20.88%.

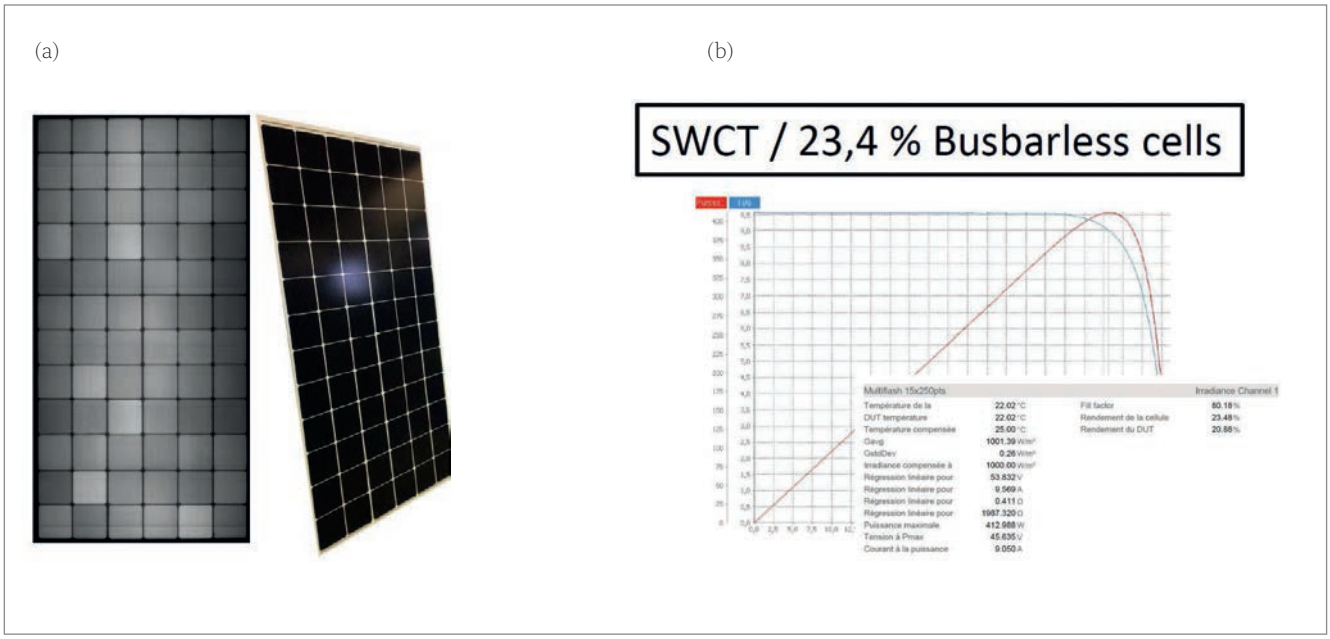

Table 1. Examples of high-efficiency SHJs from various players. The top six are laboratory devices, whereas the bottom six are produced in industrial production/pilot lines. ('BBx' denotes x number of busbars, and 'BBo' denotes busbar-less, i.e. with no current losses from the busbars.)

Efficiency [%]	Company/Institute	Cell type/Specs	Reference
26.7	Kaneka	IBC, 79cm^2, n-type, certified	[27]
25.6	Panasonic	IBC, 144cm^2, n-type, certified	[28]
25.1	Kaneka	100cm^2, n-type, certified	[25]
24.7	Panasonic	102cm^2, n-type, 98µm, certified	[29]
24.2	CSEM/EPFL	4cm^2, n-type, SP, certified	[30]
23.8	CSEM/EPFL	4cm^2, p-type, SP, certified	[30]
24.1	CSEM/CIC	220cm^2, n-type, BB4, Cu-plated, certified	[10]
24.0	Meyer Burger	244cm^2, n-type, BB0, SP, certified	[30]
23.9	CEA-INES	244cm^2, n-type, BB5, SP, certified	[31]
23.7	CIE	244cm^2, n-type, BB5, SP	
23.4	Hanergy	244cm^2, n-type, BB5, SP	
23.4	SIMIT	n-type, plated	

Figure 5. Meyer Burger's HELiA PECVD tool, which uses reactors based on the 'plasma box' concept. This guarantees perfect layer homogeneity, reducing contamination, and facilitates reactor cleaning [35]. Wafer carriers see only one deposition chamber, ensuring that no contamination is introduced by the carriers. (SP = screen printed.)

numerous published results will rapidly lead to efficiencies greater than 23%.

Manufacturing equipment

More and more sets of equipment are now available for production, such as the HELiA PECVD tool from Meyer Burger, shown in Fig. 5.

"An efficiency gain at the cell level and an energy yield gain at the system level *should more than offset the extra CAPEX* for achieving a low cost of solar electricity."

The amorphous silicon layers can be deposited by PECVD with different reactor designs or by CAT-CVD (hotwire), whereas the TCO layers can be deposited by PVD (sputtering) or plasma-assisted evaporation (PAE, otherwise known as RPD, denoting rapid plasma deposition). These techniques have all been proved in production. Even though CAT-CVD and PAE are known to reduce bombardment from high-energy ions, PECVD and PVD layers lead to equally good cell results with proper processes. Other coating techniques, however, have not yet been proved in production. Two other critical elements are:

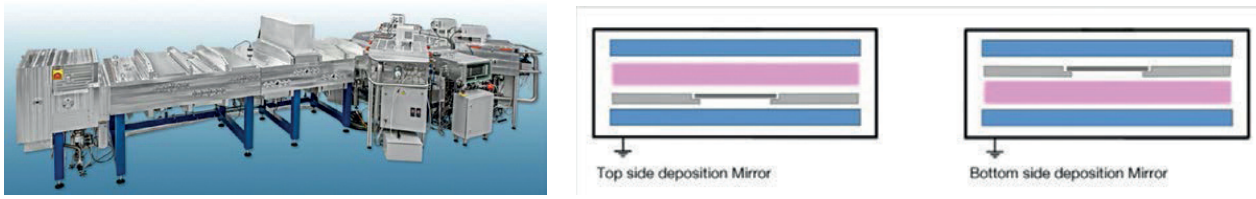

Figure 6. INDEOtec's R&D OCTOPUS II, incorporating with the mirror reactor concept. The wafers are placed once on a carrier and receive front and rear a-Si:H coatings while remaining on the same carrier.

- **Wet chemistry**, which is now well under control. The introduction of ozone cleaning can significantly reduce the cost of consumables [32,33].

- **Automation**, which is often underestimated, with many first lines having suffered from issues linked to wafer handling, queue time and sometimes low process control. Experience and production solutions suited to fully exploit these kinds of surface-sensitive device are hence needed. These are not available from all equipment vendors, but as demand grows, new solutions are being introduced [34].

Equipment pricing

In an emerging market, several equipment vendors are reluctant to release official numbers. Currently, the total of core production equipment (wet, PECVD, PVD solutions) should be in the range $7–13m/100MW, depending on the line suppliers, to which $3–5m must be added for the remainder of the tools (entrance control, automation, printing, annealing, measurement and sorting). Once the market develops, a significant price drop should take place, as well as simplifications to automation. Even at the current stage, it is worth considering the following elements:

- An extra CAPEX of $5m/100MW (for cell + module) compared with, for example, a PERC line would lead to about 1¢/W extra cost, when depreciated over five years, which ought to be the case in a sustainable business (i.e. if capital is available and if the market has been in existence for at least five years).

- An efficiency gain at the cell level and an energy yield gain at the system level *should more than offset the extra CAPEX* for achieving a low cost of solar electricity, as will be shown in the next section.

Various approaches to reducing CAPEX, beyond purely manufacturing volumes of tools, include: parallelization of processing reactors, single-carrier processes for PECVD and PVD, in-line processing, and shorter cycling times through suitable system design. For instance, in INDEOtec's approach, a single hollow carrier allows the deposition of the front and rear a-Si:H, by keeping the wafer on the same carrier, saving on space and automation (Fig. 6).

Table 2 gives an overview of the activities of some of the companies and institutes involved in SHJ technology.

SHJ producers	Ramping-up	Piloting	Equipment suppliers
CIE	Ecosolifier	CEA-INES	Applied Materials[1,2]
Hanergy	Enel/3sun	Kaneka	Ideal Energy[1]
Hevel	GS Solar	Meyer Burger	Indeotec[1]
Panasonic	Jinergy		Jusung[1]
Solar City	Neo Solar Power		Meyer Burger[1,2,3]
Sunpreme	Tongwei		Ulvac[1,2]
			Von Ardenne[2]
			Singulus[4,2]

[1]PECVD or CAT-CVD; [2]PVD; [3]Modules; [4]Wet chemistry.

Table 2. Overview of some industries involved in the field of SHJ technology.

Consumables

The three major cell consumable costs are related to the wet etching and cleaning (currently reported by Singulus at <0.5–0.6¢/W with ozone cleaning [32]), the Ag paste and the TCOs. Ag paste typically comes at a similar price per kg to that of conventional paste, with a conductivity that is lower by a factor of around 0.6–0.7. For a screen-printing pattern equivalent to (for example) a front PERC, a bifacial SHJ (which operates at higher V_{oc} and slightly lower current) will require around twice as much paste, because of differences in paste conductivity. In the case of a six-busbar bifacial configuration, ~180mg Ag/cell is required, equating to ~1.5¢/W (for a paste cost of $600/kg). This would fall to 0.95¢/W for a multiwire configuration [15], and to almost zero with improved printing patterns for multiwires (10mg/side [20]). With regard to the TCO target

costs, manufacturers typically charge $520–900/kg for In-based target processing, including the price of In (currently at ~$220/kg); for 3.5g of target usage for TCO on both sides, this corresponds to 0.80–1.25¢/Wp.

Potential advantages and requirements

On the assumption of a 40µm thinner wafer and a $1\%_{abs.}$ higher efficiency, when the indicative prices given earlier are used, the wafer price would be 6.26¢/W for n-type SHJ (130µm), as opposed to 6.9¢/W for p-type wafers (170µm), i.e. 0.64¢ less per W.

With improvement to the cleaning technology, it can be assumed that cleaning costs will come in line with those for standard technology. Little effort has been made so far to benefit from the low-temperature process for the metallization of SHJ. With a growing market, pastes with lower Ag content, such as Cu-based paste [36], should quickly improve, and could lead to significant price decreases and advantages over high-temperature metallization, where Cu, for example, is particularly not acceptable.

Finally, the TCO costs can be further cut by taking different approaches, such as lowering the target manufacturing cost (–20%), reducing the rear-side TCO thickness (–25%), and possibly substituting one TCO by ZnO (–30%). In the long run, the TCO costs would be offset by the reduction in cost of the metallization, and the technology will fully benefit from the reduced wafer thickness.

At the module level, a glass–glass configuration is favoured for bifacial modules. To ensure a long lifetime, some manufacturers propose the use of an edge sealant. Depending on the type of screen-printing paste, it is possible to use soldering, gluing or a multiwire assembly for cell interconnection. Compared with a standard busbar soldering and EVA encapsulation material, alternative schemes (e.g. polyolefin – PO – encapsulation material) can ensure higher reliability, usually costing $2–3 more per m^2 for the encapsulation material, edge sealant and conductive adhesive or contacting wires. Already at the $/W level, the extra cost will be fully offset by the efficiency gain if a 1% higher efficiency is assumed, corresponding to an increase in module wattage of $10W/m^2$, which is already typically observed nowadays.

Levelized cost of electricity (LCOE)

Table 3 illustrates some of the effects expected and measured for SHJ modules. The better temperature coefficient can lead to 2–6% additional energy gain compared with a PERC module with –0.38%/°C,

and 6% being an estimation for bifacial one-axis tracking solar parks in a hot climate. Comparing the best datasheet guarantees for SHJ (Panasonic) and PERC (LONGi) over 20 years would yield a gain of $1\%_{rel.}$ in energy. Notably, as for all technologies, some sets of modules can show greater degradation, as is also being reported for PERC modules, which can suffer from various light-induced degradation mechanisms [37]. On the other hand, SHJ modules with properly processed cells show a slight increase in fill factor and V_{oc} under light soaking [38]. Because of their high bifaciality of up to 93%, an additional 2% more energy can be collected compared with standard modules with 82% bifaciality [39]. Finally, with the SHJ's higher voltage, and absence of metal impurities in the junction (leading to a better diode ideality factor), contrary to a diffused screen-printed junction, the low-illumination behaviour should allow 0.3–1% more energy (because of a lower relative voltage drop), depending on the climate. Note that this last factor can be influenced by the edge losses of SHJ cells, which, if not properly addressed, will tend to be higher than for devices with a diffused junction. With regard to this last aspect, a selection of the right coating sequence, carrier opening (e.g. in sputtering) and process parameters (e.g. coating of the edge of the wafer) should be optimized to reduce the edge losses to a minimum. Note that efficiencies of 24% or thereabouts have already been demonstrated on full wafers.

Depending on the mounting configuration, high-quality SHJ modules could therefore deliver 5.5–10% more energy per rated watt over 20 years; in the case of an equivalent module design with 6" cells, this gain should be supplemented by a 10W power gain per m^2. For large parks, assuming total system costs of 70¢/W and module costs of 25¢/W, there is a further gain to be had on the area- and engineering-related cost (here estimated at $50/$m^2$). If a conservative 7% increase in energy yield is assumed on the basis of Table 3, this means that the SHJ modules could be 6¢/W more expensive but still lead to the same LCOE. The above-mentioned gain, discussed in Haschke et al. [40], is illustrated in Fig. 7, where passivated emitter, rear totally diffused (PERT) bifacial modules and SHJ bifacial modules are compared in the United Arab Emirates (UAE) [33].

Parameter	Expected EY gain vs PERC	Remarks
Impact of TC-P_{MPP} (-0.20 to -0.27%/°C)	2-6%	2% cold climate, 4% hot climate, 5-6% for 1 axis track bifacial or for BIPV
No PID or other degradation	1.2-3%	Based on best data sheets from manufacturers -0.3%/year from year 2 vs. 0.45%/year for best PERC
Bifaciality (f_{bifi})	2%	Assuming 20% rear illumination f_{bifi} SHJ = 93%, f_{bifi} PERC = 82%
Low illumination	0.3-1.0%	Estimates for V_{oc} of 740mV (SHJ), 680mV (PERC) for resp. high, low average irradiance
Total	**5.5-10%**	

Table 3. Potential percentage gain in energy yield (EY) by SHJ technology relative to PERC. ('BIPV' denotes building-integrated photovoltaics.)

Source: Courtesy A. Richter, Meyer Burger [41].

Figure 7. Field data collected from PERT bifacial modules and SHJ SWCT bifacial modules.

From lab to fab

Some recent results on SHJ cells were shown in Table 1; these include some of the most recent 2cm × 2cm screen-printed devices made by CSEM/EPFL. Certified efficiencies of 24.24% and 23.76% for n- and p-type wafers respectively have been achieved (designated area – da – measurements) using the process flow in Fig. 1. For n-type, similar results have been obtained on Cz-Wafers. Table 1 also indicates various results on industrial cell sizes with similar process flows to those described in this paper, as well as the figures for back-contacted record cells.

Cells in pilot and production lines

There are now more and more players in the field, and several 50–200MW lines have been deployed, several of which are operating on a 24/7 basis, as shown in Table 2. Besides Panasonic, plans for GW lines have been announced by several manufacturers, some with first-phase constructions. There will be a need for volume, as with all c-Si technologies, in order to compete with the absolute lowest manufacturing costs in terms of $/W. At an intermediate production level (100–500MW),

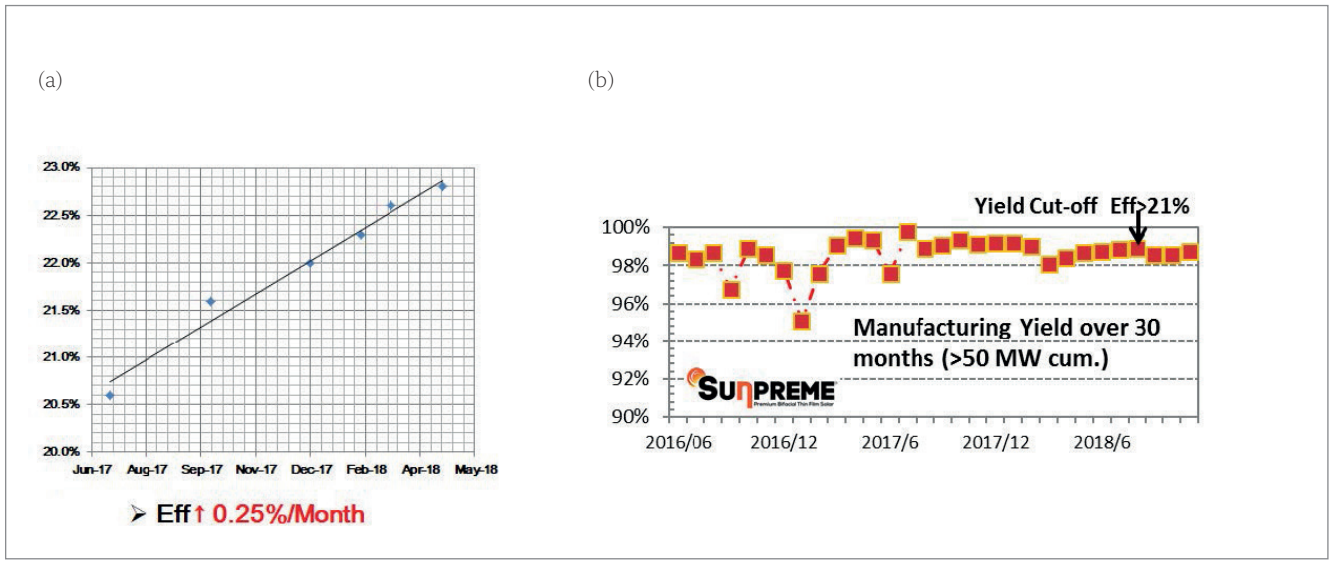

Figure 8. (a) Ramping-up of production at CIE (China), showing the significant efficiency increase (BB5 SHJ solar cells) over the first year (courtesy CIE). (b) Production yield for over 50MW produced cells, with a yield of around 99% in 2018 (for >21%, average 22.2%, five busbars).

there is still room for a competitive market entry in terms of cost of energy, by considering energy yield benefits.

At the 6"-cell level, several pilot lines have achieved efficiencies in the range 22.5–24%; for instance, Fig. 3(b) shows cells with 24.15% after plating (four-busbar measurements). In its demo line in Germany, Meyer Burger has demonstrated runs yielding an average efficiency of 23.65%, and certified 24.17%-efficiency best cells in the busbarless (BB0) mode (a popular industry standard, taking no account of either the shading from busbars or some of the resistive losses in the fingers, corresponding to ~0.5–0.6% efficiency gain compared with a five-busbar cell) [12]. Note that these are pilot-line cell results, whereas some of the high-efficiency PERC cell results rely on localized passivating contacts not representative of

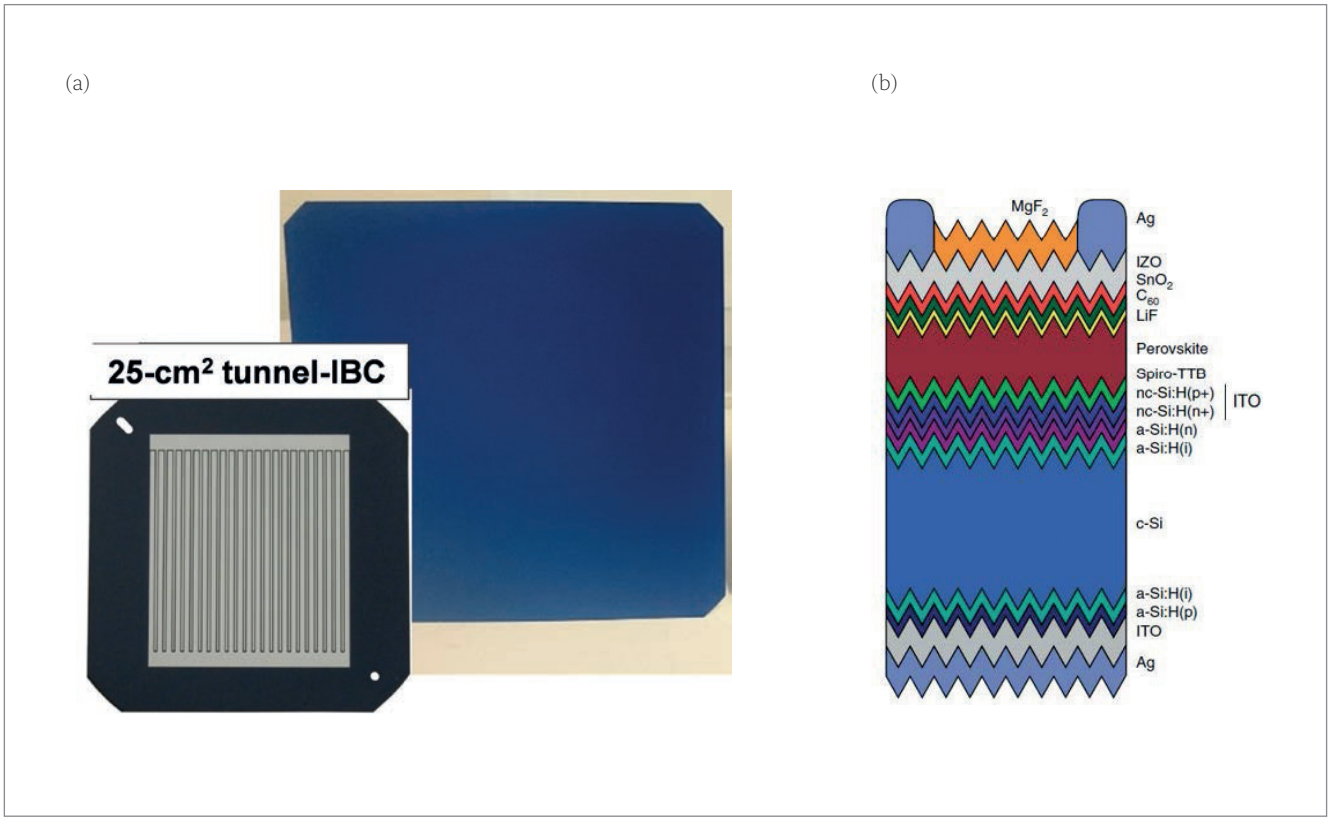

Figure 9. (a) New-generation IBC-SHJ, created at CSEM [42] using the tunnel process, yielding an efficiency of 24.8%. (b) Schematic of the perovskite on textured SHJ cell concept [45].

production status, and not necessarily compatible with low production costs. On the basis of continuous process improvements, CEA was able to demonstrate a 23.9%-certified five-busbar SHJ using Meyer Burger production tools. With line optimization and further improvement in printing and TCO, efficiencies in the range 24–24.5% should be targetable.

Table 1 illustrates that lab results can readily be transferred to production tools; for instance, using multiwire technology, certified modules with 341W (60 cells) and 412W (72 cells) of standard-size wafers (M2) have been obtained, with *FF*s reaching 79.7% and >80% respectively – remarkable values, illustrating the maturity of the technology. More recently, CEA and Meyer Burger produced a 348W standard 60-cell module with high efficiency by using half cells. As well as Panasonic, Sunpreme and Hevel, several production lines are now running with 6" cells, achieving high efficiencies, such as Hanergy at 22.2–22.3% and CIE at 23% average (all values reported in October 2018). All these companies are still on the efficiency learning curve: Fig. 8(a) shows the improvement in average cell efficiency from 20.5% to 22.8% in 10 months during 2017/18. After an adaptation of some equipment, average efficiencies are surpassing 23% (Oct 2018). The production yields have been reported by manufacturers or by pilot lines to be at high levels, coming close to 99%, as indicated, for example, by Sunpreme (Fig. 8(b)).

"SHJ is set to become one of the most attractive PV technologies."

Extending the learning curve

On the basis of the lab and pilot-line results, it can be expected that screen-printed, multi-busbar devices will reach, with full optimization, efficiencies in the range 24–24.5%.

Extending the efficiency curve

There are two ways SHJ could, in a next step, evolve towards a higher-efficiency product.

First, one can add a set of tools to realize back-contacted cells with a 5–8%$_{rel.}$ efficiency increase. Such a device structure holds the world record for c-Si-based PV, including 26.7% by Kaneka [26]. Although the processing steps required to achieve such an impressive efficiency result are probably not straightforward to industrialize, Fig. 9(a) shows an image of a 25cm² cell created using the tunnel junction approach, which drastically simplifies the processing of IBC devices [42]. It notably requires only one in situ patterned contact layer, and one alignment step for the metallization. Certified results of 24.45% [43], and more recent in-house results of 24.8% (25cm²), have already been obtained.

Second, SHJ solar cells are ideal as a bottom cell in multijunction devices; they were used in the record-breaking four-terminal III-V on Si (32.8% for two junctions, and 35.9% for three junctions) [44]. These cells also serve as an ideal bottom

"At the 6" cell level, several pilot lines have achieved efficiencies in the range 22.5–24%."

cell for perovskite/silicon tandem devices (Fig. 9(b)), with a recently certified efficiency of 25.24% [45]. Even more recently, Oxford PV announced a 27.3% efficiency, and even 28.0%, presumably with an SHJ bottom cell [46]. These approaches could lead to >30% efficiency 6" solar cells, even though there are still cost and reliability hurdles to overcome in order to achieve the status of a bankable product.

Conclusions

Over the last 10 years, there have been a number of significant improvements in the field of SHJ technologies. These include:

- The development of processes compatible with low-cost industrial production.
- The technology becoming widespread, with more and more groups achieving efficiencies above 23%.
- The development of advanced metallization and interconnections technologies.
- The improvement of n-type wafer material quality.
- The achievement of high efficiency on production tools.
- The availability of comprehensive production solutions.

If and when capital is available, SHJ is set to become one of the most attractive PV technologies. One can therefore assume that it is now ready for a true mass-production launch.

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