Etching, texturing and surface decoupling for the next generation of Si solar cells

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ABSTRACT

Si etch processes are vital steps in Si solar cell manufacturing. They are used for saw damage removal, surface texturing and parasitic junction removal. The next generation of Si solar cells, featuring thinner wafers and passivated rear surfaces, will pose more stringent demands on those steps. Surface decoupling (achieving different surface treatments on the front and the rear) has to be achieved while minimizing Si consumption. Plasma texturing is an emerging technique that appears very promising in that respect, as efficiencies as high as 17.4 % have been achieved on screenprinted multicrystalline Si solar cells incorporating this process.

Introduction

Bulk crystalline Si is presently the dominating photovoltaic technology and will probably remain so for the next two decades. The present solar cell processes make extensive use of Si etching steps [1,2]. It is expected that these types of processes will gain in importance in the next few years, but also that they will face more stringent requirements in terms of Si consumption and surface morphology as the wafers used in the industry become thinner and more fragile.

There are three steps in which Si etch is involved:

- Removal of the region near the surface of the wafers with many defects induced by the wire sawing process (saw damage)
- Texturing the front surface
- Removing the parasitic junctions formed at unwanted locations on the cell during the diffusion process

In this paper, we will first review the state-of-the-art in terms of Si etch processes in Si solar cell production. We will then sketch the trends and link them with new requirements for the Si etch steps, concluding with a discussion of alternative techniques to the traditional wet chemical processes and the challenges presented by these techniques.

State-of-the-art

Silicon substrates used in commercial solar cell processes contain a near-surface saw-damaged layer that has to be removed at the beginning of the process. A layer with thickness of 5 to 10µm has to be etched from both sides of wafers. The damage removal etch is often done in a 20-30 wt. % aqueous solution of NaOH or KOH at 80 - 90°C. This process is a batch process where the wafers are placed in a cassette and immersed in a bath with the appropriate solution. The reaction takes place on both sides simultaneously. For multicrystalline Si, one should monitor and control the etching process to limit the formation of steps at grain boundaries, which can lead to problems during metallization.

The wafer surface after such alkaline saw damage etch process is flat, and therefore shows a high reflectance. If solar cells are made with such surface, the currents will be low, leading to low conversion efficiencies; therefore, most industrial processes today include a texturing step, which has two beneficial effects. Firstly, rays reflected at the facets get a second chance to be coupled into the cell. Efficient surface texturing can reduce the reflectance from more than 35% to less than 10%, which is in practice lowered further by using an anti-reflection coating (ARC). Secondly, front surface texturing ensures that light rays are coupled into the solar cell under an oblique angle, making it less probable that they will escape from the front surface after reflection at the rear. This effect is especially important when using thin silicon substrates (<200µm).

If the substrate is monocrystalline, it is advantageous to make use of the anisotropic etching properties of Si in an alkaline solution. As the {111} planes get etched more slowly than other crystal planes, {111} facets are developed. On <100> wafers, this leads to pyramidal shapes at the surface that are particularly effective in reducing reflectance. In laboratory cells, an oxide etch mask formed by photolithography is sometimes used, resulting in a regular array of pyramidal pits (with facets at 54.7° to the horizontal plane) called inverted pyramids (see Figure 1), with reflectances as low as 8% without ARC. In industrial processes, however, masked processes are avoided. It is possible to achieve almost the same level of reflectance by maskless etching where one relies on random processes to create locally the different etch rates needed to initiate the pyramid formation. This process is carried out in a weak solution (weaker than for saw damage etching) of NaOH or KOH with addition of isopropanol to improve wettability [3]. The process results in a surface covered with randomly distributed upside pyramids, as shown in Figure 2. The process requires careful control over the etch parameters and solution composition (in particular to keep the isopropanol concentration constant in spite the evaporation effect). When the process is under control, uniformly distributed pyramids with a height of 3-5µm are obtained. This process step is also done in a batch wetbench, and results in texturing on both sides unless special precaution is taken to avoid such an outcome. From a manufacturability point of view, it is advantageous to combine the saw damage step and alkaline texturing in one single step, in which case a trade-off has to be found between process speed and quality of the texturing. After alkaline etch, a neutralization step in a dilute HCl solution is required.

Isotropic wet texturing requires the presence of surface defects to work effectively. On substrates without saw damage such as Si ribbons, acidic texturing either does not work or presents issues of uniformity and reproducibility.

Alkaline random texturing is not effective on multicrystalline silicon substrates due to its anisotropic nature. Some grains (typically those with an orientation close to <111> normal to the surface) remain untextured, leading to a high average reflectance. A very elegant technique of texturing multicrystalline silicon is to etch the wafers in an acid mixture based on HF and HNO_3 [4]. The HNO_3 tends to oxidize the surface, while the HF etches the oxide away. The etching process occurs preferentially at defects. Therefore, when saw damage is present, this etching process structures the surface in a way that is independent of the crystal orientation. This acidic isotexturing results in lower reflection than traditional anisotropic etching on multicrystalline material, and better conversion efficiency [4,5]. A SEM picture of the surface of an acidic isotextured wafer is shown in Figure 3.

This process was first successfully developed at IMEC, but similar developments were later on carried out at other institutes [6,7]. The process has by now become a standard for multicrystalline Si solar cells. For a sufficient lifetime of the etching bath, it is important to monitor the amount of Si etched and to replenish the solution accordingly, to ensure that the necessary reagentia are not depleted.

If properly monitored and replenished, the bath can be used for many thousands of wafers, and the chemicals consumption per wafer is very limited. Apart from the batch approach, such processes can also be done in in-line wetbenches, which are now available from equipment vendors. In both batch and in-line systems, the wafers are typically completely immersed in the solution, resulting in texturing on both sides. After acidic texturing, wafers are usually dipped in a dilute alkaline solution to remove a thin porous silicon layer that is formed during the texturing step (stain etch). This is followed by a neutralization step to remove all Na or K atoms from the surface before emitter diffusion.

It should be noted that isotropic wet texturing requires the presence of surface defects to work effectively. On substrates without saw damage such as Si ribbons, acidic texturing either does not work or presents issues of uniformity and reproducibility.

The P-diffusion process that follows texturing usually creates a junction all around the wafer. As a result, some regions are doped where doping is not desired and can actually be detrimental to the solar cell operation. Therefore, an Si etch process is often applied to locally remove the undesirable P-doped regions. A few years ago, the standard technique was plasma etching in a plasma reactor, where the cells were stacked on top of each other with (possibly) rubber sheets in between. The stack is then exposed to the plasma, removing about one micrometer of Si at the edges of each wafer. The parasitic junction at the rear remains, but nevertheless the step is effective in a conventional process as most of the rear surface is converted into p-type during the final BSF formation while the shunt paths at the edge are removed. However, because it involves extensive handling, significant forces applied onto the wafers and the need for gas abatement, this technique has to a large extent been replaced in the last few years by laser scribing along the cell edge. More recently, in-line wetbenches have been introduced that completely etch away the doped region at the rear of the wafer. The solar cells are transported just above the etch bath level (typically an aqueous solution based on HNO_3 and HF), so that only the rear side is etched, leaving the emitter at the front intact. This process is usually combined with phosphorous glass removal in the same wetbench, just prior to the rear side etch.

Quite a large volume of water is required for rinsing after wet chemical etch steps. The typical 5 litre/Wp for a conventional process is not only an environmental issue (proper waste treatment has to be foreseen), but can be a significant supply and cost issue, which is anticipated to increase in importance as water resources become scarcer. Optimizing the process towards minimal water consumption is therefore vital both from the environmental and from the economic points of view.

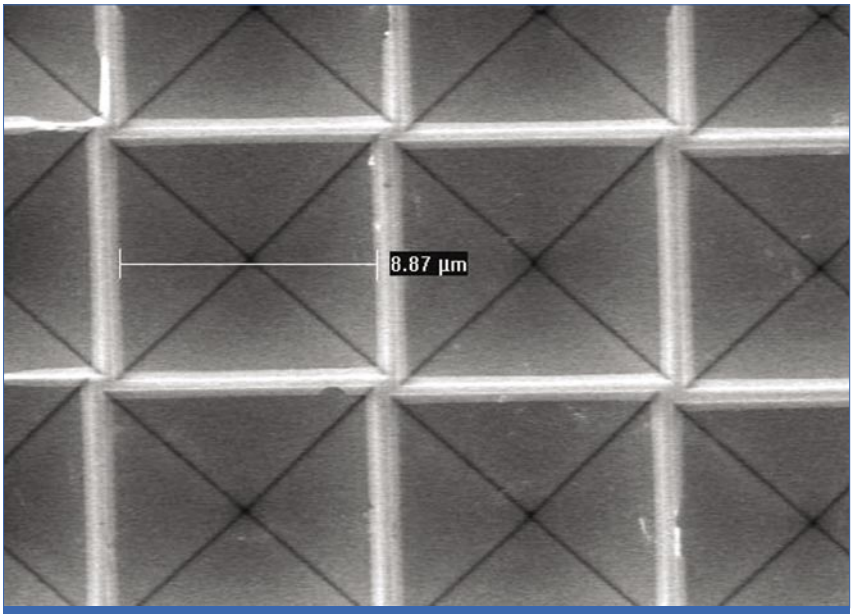

Figure 1. SEM top view of a silicon surface with inverted pyramids.

Surface decoupling

The conventional Al-BSF, formed by an alloying process during the screenprinting metallization step, provides only moderate surface passivation, with recombination velocities in the order of 1000cm/s. For very thin cells, however, recombination at the rear surface gains in importance, and substantially lower surface recombination velocities are required. Below a thickness of 200µm, the Al-BSF passivation is no longer sufficient and one observes a substantial loss in both V_{oc} and J_{sc}. Another issue with Al-BSF on very thin wafers is the wafer bowing induced by the different thermal expansion coefficient between Si and Al, which may lead to problems with cell handling and module manufacturing. A last drawback of the Al-BSF is the absorbance that takes place in the BSF region. A BSF is typically 5µm thick, and all photons absorbed in this region are lost for conversion. While small for standard thicknesses, this loss becomes very large as wafer thickness decreases and light confinement gains in importance. For all of these reasons, a new concept of rear structure is required to provide low recombination at the rear surface, with dedicated passivation layer and local contacts. Possible candidates for the passivation layer are silicon oxide layers, adapted silicon nitride layers, amorphous Si layers, and stacks of such layers. Prominent examples of solar cell concepts based on dielectric passivation at the rear are shown in Figure 4.

These structures are depicted with a textured front surface (needed for any high-efficiency cell) and a flat rear surface. In other words, the surface treatments of the front and rear of the wafers are

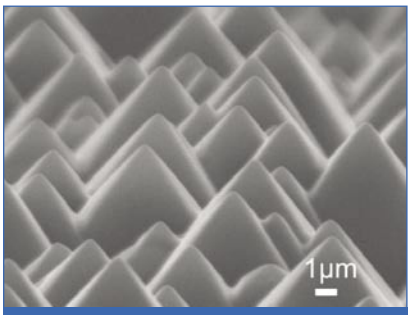

Figure 2. SEM picture of a monocrystalline Si surface with random pyramids, textured in an alkaline solution.

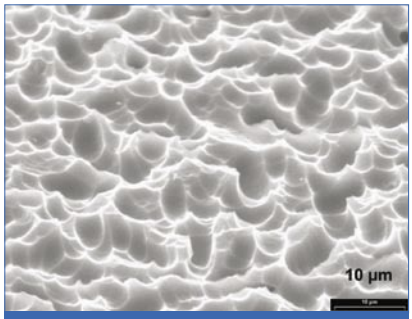

Figure 3. SEM picture of an acidic textured surface of a multicrystalline Si wafer.

decoupled – a significant feature of these new solar cell concepts, which is related to the quality of the surface passivation at the rear. It appears that it is much more difficult to achieve the high level of surface passivation required if the rear surface is rough. For surface passivation schemes that rely on lowering the density of interface defects, such as with intrinsic amorphous Si and silicon oxide, this is easily understood. A rougher surface has a much larger effective area and therefore effectively many more sites where harmful defects can be present, making exhaustive passivation difficult. For surface passivation layers that rely on a field effect, such as stoichiometric PECVD silicon nitride layers, this is not as obvious. One would expect that the surface passivation is much less dependent on the roughness than on the density of fixed charges in the dielectric, and this has been confirmed at lifetime test structure level [11]. However, in solar cell structures, a non-textured rear surface appears to be needed to reach low effective recombination velocities and high efficiencies.

Achieving surface decoupling in a practical way is not straightforward. One can possibly use similar in-line etch systems as for rear parasitic junction removal since this is an existing one-side treatment, but the requirements for the etch steps are different. If one starts with wet chemical texturing (which in all commercially available systems today occurs on both sides) and proceeds with one-side rear surface etching to polish the rear surface, the process is relatively long and one that tends to consume a substantial amount of Si, clearly an unwanted effect when the wafers are already very thin to start with. The development of practical and manufacturable one-side texturing process steps (alkaline and acidic) and of one-side saw damage removal process steps is desirable and would be directly implementable in many advanced process flows.

Alternatives to wet chemical etching processes

Etching silicon substrates can also be realized by means of plasma technology. In this technology a plasma discharge is created and molecules are partially dissociated into radicals upon electron impact. Those radicals, with or without the assistance of ions, etch the silicon. The radicals that etch silicon are typically halogens, of which the fluorine atom is the most effective.

A distinction has to be made between Reactive Ion Etching (RIE) and other types of plasma texturing. RIE relies on the ion bombardment that creates damage on the surface. This technique has proved to yield uniform and low reflectances [12], but the defects induced by the ion bombardment is a problem. A possible solution is etching the damaged region subsequently by wet chemical means. At IMEC, we have developed a process based on microwave-powered antennas [13]. These antennas are positioned above the substrates providing sufficient radical density to cause chemical etching on the surface. Ions do not play a role in this process unless an RF bias is applied. The gas chemistry is based on SF_6, N_2O and Cl_2. The process is self-masking, in that the residues of the etching process temporarily get deposited on the surface, leading to a locally lower etch rate and the formation of a texture. The etching process is isotropic, leading to the same texture regardless of the grain orientation. With the right process parameters, one can obtain a uniform, moderate reflectance (15-22% before ARC deposition) and a low surface area enhancement (required to maintain high V_{oc}). The features of the surface texture are much finer (about 10 times smaller) than those of alkaline or acidic textured surfaces (see Figure 5).

Plasma texturing should be seen as an enabling technology for advanced Si solar cell technologies.

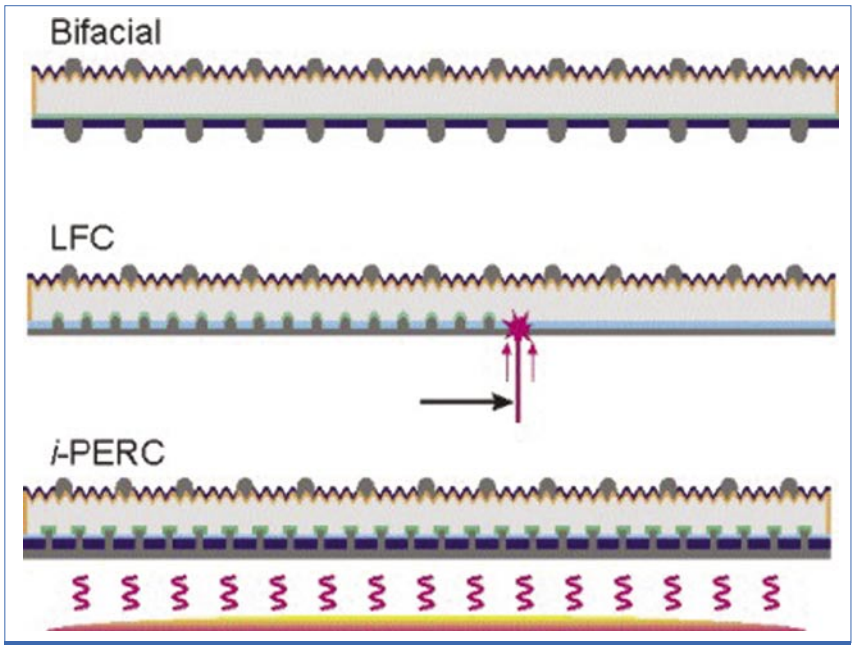

Figure 4. Three different concepts for industrial passivated rear surface solar cells: bifacial solar cells with fire-through contacts (as in [8]), laser-fired contact solar cells (LFC [9]), and selective alloying, thermally-fired local BSF solar cells (*i*-PERC [10]). All concepts feature a very good surface passivation with a dielectric layer at the rear and local contacts to the silicon.

When plasma texturing is applied as a replacement for acidic isotexturing in standard, thick (200µm) screenprinted solar cells, it yields similar or only slightly higher conversion efficiencies: the real benefit of plasma texturing is apparent in advanced structures and for very thin wafers. Since plasma texturing is inherently a one-side process, it is straightforward to achieve the surface decoupling discussed above, whereas it is a challenge with wet chemistry. Moreover, the process consumes only a minimum of Si (can be as low as 1µm). It is therefore possible to devise a process scheme removing the absolute minimum amount of Si required, e.g. a saw damage removal step removing ~5µm of the saw damaged region on each side, and then 1µm for texturing. Plasma texturing should therefore be seen as an enabling technology for advanced Si solar cell technologies. At IMEC, we achieved a conversion efficiency of 17.4% on a screenprinted multicrystalline Si solar cell with the *i*-PERC process, which includes plasma texturing [14].

Plasma texturing is also particularly appropriate for wafers produced without surface damage such as Si ribbons and epitaxial layers on low-cost Si substrates, for which no easy wet chemical texturing process is available. Plasma texturing has proved to bring a significant advantage on both types of substrates [15], [16 – *see IMEC paper, page 83*].

Before plasma texturing can be applied on an industrial scale, several issues have to be dealt with successfully. First, the process needs to be upscaled such that it provides the necessary throughput while providing low cost of ownership. Moreover, excellent uniformity has to be reached over large areas. Both issues are serious technical challenges and will no doubt require substantial development efforts. However, the history of successful development of vacuum in-line systems for the PV industry inspires confidence that it can be achieved. Another important issue is gas abatement. While replacing wet texturing by plasma texturing would reduce the amount of wastewater dramatically, the release of greenhouse gasses could offset that environmental advantage completely if not properly tackled [17,18]. SF_6, for instance, has a huge Global Warming Potential of 24000. Just a few percent of the SF_6 flow getting past the abatement system leads to a poor environmental balance, which is unacceptable for a PV product. This problem, however, is common to several processes in microelectronics and, increasingly, thin-film photovoltaics (reactor etching). Producers of gases and abatement systems have responded to the challenge and are now developing solutions that can lead to zero release of GWP gas, either by effective recycling of the fluorinated species, or by offering alternative gas systems with low GWP [19]. Typically, these installations only make economic sense for very large plants. Taking into account the soaring scale of solar cell manufacturing plants, this should not be a problem in the future.

Another possible application of Si etching by plasma is a shallow uniform etch for junction removal at the rear, advantageously combined with phosphorus glass removal in the same step. The feasibility of such a process has been demonstrated in in-line or quasi-in-line systems [20,21] but needs further development. The combination of three plasma processes (PSG removal, rear junction removal and silicon nitride deposition) in the same vacuum in-line chain is very appealing from a manufacturing point of view.

Finally, it should be mentioned that laser ablation is also being investigated as an alternative to etching of Si, for surface texturing [22] or the formation of special topographies enabling high efficiency structures [23]. The advantage of laser structuring is that it enables the formation of sharp and precise features on the surface without the need of prior patterning of a mask. However, the silicon in laser-ablated regions is damaged, and typically needs a subsequent wet chemical damage etch. Process speed (particularly if the complete substrate surface needs to be scanned) and cost are presently significant issues for laser structuring, although they may be solved in the future thanks to the fast progress in laser development.

Conclusion

Si etching steps are used extensively in present Si solar cell manufacturing, and it is expected that those steps will gain in importance in future technologies. The main processes used today are random texturing in dilute alkaline solution for monocrystalline Si, acidic isotropic texturing for multicrystalline Si, and one-side shallow etching for parasitic junction removal. It is anticipated that new processes will be introduced in the future that enable fast texturing and deep silicon etching on only one side, as surface decoupling is desired for many advanced solar cell structures. An emerging field is that of plasma-based Si etching processes for solar cells. Plasma texturing has proved particularly suitable for advanced solar cell structures and new low-cost substrates.

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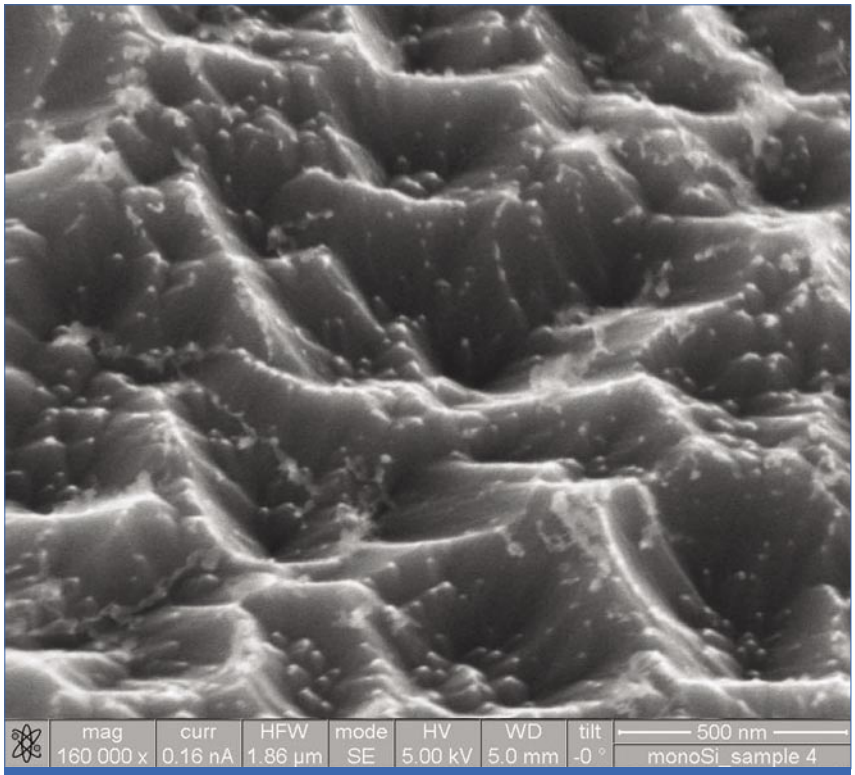

Figure 5. SEM picture of an Si wafer after the IMEC plasma texturing.

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Patrick Choulat graduated with a B.Sc. in material sciences at the Robert Gordon University of Aberdeen (Scotland) in 1994, and with a Master's degree in material sciences at Ecole National des Sciences Appliquées (INSA), France, in 1998. Since then, Mr Choulat has been working at IMEC (Belgium) as a development engineer in the field of photovoltaics. His work has mainly been dedicated to bulk Si solar cells for industrial applications. Image pending

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Joachim John received his diploma degree in physics from the Albert-Ludwigs-University in Freiburg in 1993. He received his Ph.D. in physics from the Federal Institute of Technology (ETH), Switzerland in 1997. From 1990 to 1993 he worked with the Fraunhofer Institute for Physical Measurement Techniques, Germany, doing research and development on semiconductor mid-infrared lasers. From 1993 to 1998 he worked first as a Junior Scientist later as a Senior Scientist on photovoltaic mid-IR sensor arrays at ETH, Switzerland. In 1998 he joined IMEC, Belgium, where he is presently leader of the Industrial Solar Cells team.

Jef Poortmans, Department Director Solar & Organic for IMEC, received his Ph.D. in 1993, after which he joined IMEC's photovoltaics group, where he became responsible for the Advanced Solar Cells group. He began activity around thin-film crystalline Si solar cells and organic solar cells at IMEC and he has been coordinating several European Projects in this domain. At the moment he is Program Director of IMEC's Strategic Program SOLAR+. Dr. Poortmans has authored or co-authored close to 350 papers that have been published in Conference Proceedings, books and technical journals.

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