This paper first appeared in the sixteenth print edition of the *Photovoltaics International* journal, published in May 2012.

Selective emitter (SE) technology – the transfer from laboratory to optimization in full-scale production

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ABSTRACT

The selective emitter (SE) concept features two different doping levels at the front surface of the cell. Both doping profiles are tailored individually to best suit their specific purposes, thus achieving both low contact resistance of the emitter electrode and low recombination in the emitter and at the Si/SiN_x:H interface. This paper details the experience gained since the first tools for generating an SE structure were installed two years ago. The approach taken is discussed and a presentation given of the physical concept and properties of SE technology, along with the different aspects that have to be considered when integrating SE into an otherwise unchanged production facility.

Introduction

In standard cell architecture using p-type wafers, uniform phosphorus doping of the front surface is applied to create the n-type emitter. The depth profile of the dopant concentration is chosen so that it allows a low contact resistance of the emitter electrode to the doped silicon, while at the same time attempting to minimize carrier recombination in the highly doped layer and at the interface between the silicon and the passivation layer. When screen printing the conventional silver paste for metallization, low contact resistance to the emitter is achieved best through applying a high dopant concentration to the emitter [1]. On the other hand, in order to reduce recombination at the front surface, it is essential that doping levels be kept low [2]. This conflict between doping requirements is the main source of electrical loss occurring in homogenous emitter designs.

A selective emitter (SE) separates the doping requirements by providing a highly doped area intended for metallization and a lightly doped area for reduced emitter and surface recombination. Thus, it becomes possible to minimize resistive and recombination losses.

While many SE approaches are discussed in the literature only a few are actually suitable for mass production. Considerations of process stability, tool cost, process cost

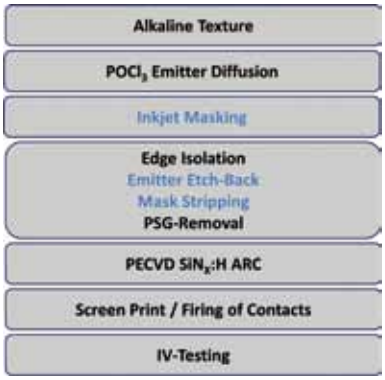

Figure 1. Process flow for cells with the etch-back SE structure. Three additional process steps are added to the standard production process, two of which are integrated into the wet bench that is used for edge isolation and PSG removal.

of ownership and ease of integration have led to only a handful of concepts being deemed practical [3]. This paper reports the experience gathered in almost two years of SE production at Sunrise Global Solar Energy Co. Ltd., a solar cell manufacturer in Taiwan. The production method used is based on the etch-back approach originally developed at the University of Constance, Germany [4].

> "A selective emitter separates the doping requirements by providing a highly doped area intended for metallization and a lightly doped area for reduced emitter and surface recombination."

Process description

The cell fabrication process begins with alkaline etching to produce a random-pyramid texture; after this, the wafers are subjected to a batch-type phosphorus diffusion using $POCl_3$ as the precursor to create an n-type layer at the front surface. The areas intended for metallization are then masked with an inkjet system. Edge isolation, emitter etch-back, stripping of the inkjet mask and PSG removal are carried out using a single wet bench. The wafers then follow the standard production process consisting of PECVD SiN_x:H anti-reflection coating (ARC), followed by screen printing and firing of the electrodes. A schematic of the process flow is shown in Fig. 1.

Choice of masking technology

Initial development work in the laboratory employed screen-printing technology for partial masking of the emitter. Several technological challenges – such as thermal treatment of the mask, ease of removal and alignment precision – prompted the adoption of a different technique for carrying out the masking step. Replacing screen printing with inkjet printing of hot-melt wax offered several advantages:

- No thermal treatment of the mask required; the hot-melt wax used freezes upon contact with the wafer.
- Superior alignment precision (±7µm); no gradual distortion of the mask from screen warping.
- Tight control over deposited amount of masking material; exact reproducibility, eliminating process deviations found in screen printing.
- Touchless technology, minimizing mechanical stress on the wafer.
- High throughput of up to 2400 wafers/hour in a single tool; in-line integration with subsequent wet bench.

The inkjet system had originally been designed for printed-circuit board applications. Apart from a few niche applications, it had not previously been used in the production of solar cells, but a few technical changes to the alignment technique and transport system made it suitable for crystalline wafers. Today, the inkjet system prints 25 wafers in a single cycle, making use of different alignment algorithms according to customer requirements.

Emitter etch-back technique

Etching back the emitter removes the very highly doped layer at the surface, also called the 'dead layer'. Removal of the dead layer leads to an increase in emitter transparency and facilitates surface passivation. Both effects increase short-circuit current (I_{sc})

Figure 2. Inkjet system (left) including loading/unloading section. Alignment system (right) recognizes wafer position for accurate placement of the printed mask.

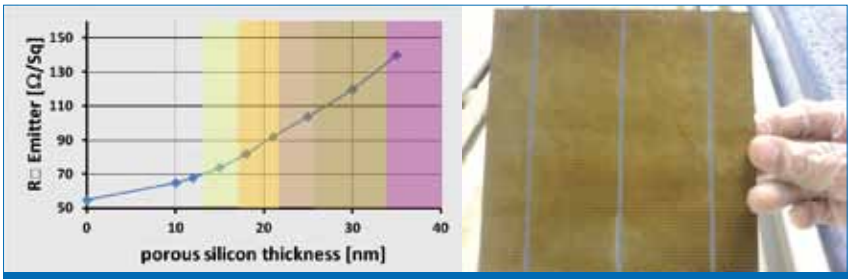

Figure 3. Left: Emitter sheet resistance vs. porous silicon thickness created in the etch-back process for an initial sheet resistance of 50Ω/sq. Right: Porous silicon layer after inkjet masking and emitter etch-back.

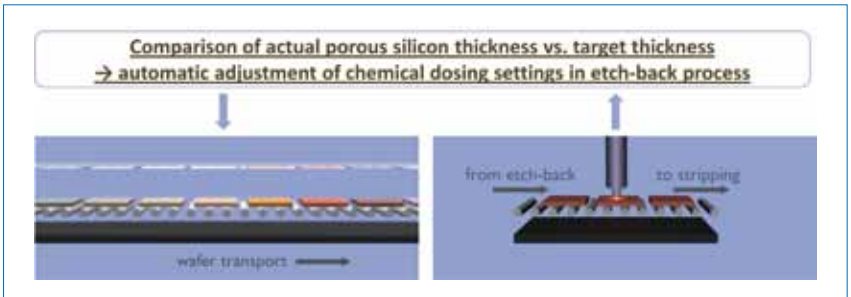

Figure 4. Schematic of the etch-back technique and process control. The thickness of the porous silicon layer is measured online immediately after the etch-back process. The measurement data is fed into a control system that adjusts the chemical concentration in the etch-back process if necessary. After the measurement, the porous silicon layer is stripped, along with the inkjet mask (not shown).

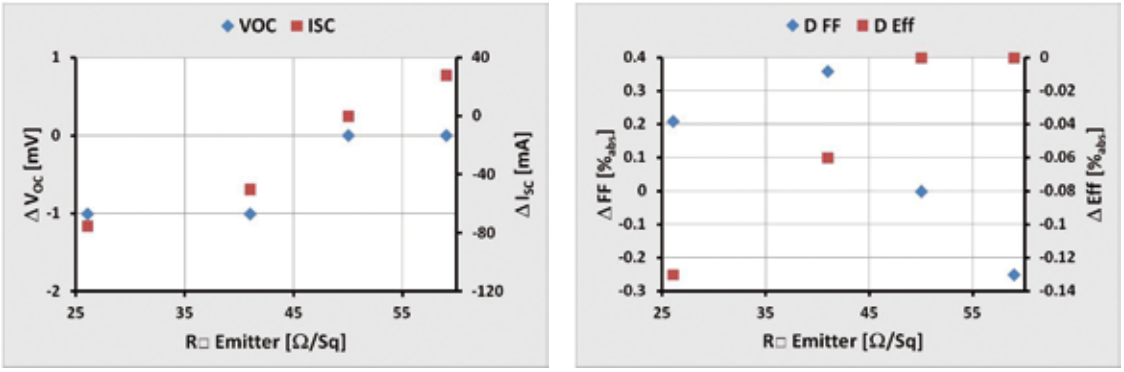

Figure 5. Dependence of V_{oc} and I_{sc} on initial emitter sheet resistance (left). All groups have been etched back to a sheet resistance of 80Ω/sq. In general, a higher initial emitter sheet resistance tends to produce a higher cell efficiency (right).

and open-circuit voltage (V_{oc}). To benefit from an etched-back emitter it is essential to have excellent control over the etch depth: etching too deeply will lead to an excessive increase in emitter sheet resistance, causing a decrease in fill factor (*FF*) and efficiency, while shallow etching will not fully remove the dead layer. In order to determine the etch depth exactly, a special technique is employed. During the process, the etch-back solution creates a thin layer of porous silicon whose thickness correlates with the etch removal. The more silicon is etched, the thicker the porous silicon layer created. The layer is removed later in the stripping process along with the inkjet mask using a caustic etch solution.

As a result of the growth of the porous silicon layer, the wafer will change its colour, enabling the operator to detect with the naked eye any process deviations and local inhomogeneous etching. The porous silicon layer thickness is measured online using an optical spectrometer in the wet bench, thus allowing the operator to exert precise control over the etch-back depth. In addition, a closed-loop feedback cycle is integrated in the control software and this automatically adjusts the concentration of the chemicals to achieve the desired etch-back depth. A schematic of the control method is shown in Fig. 4.

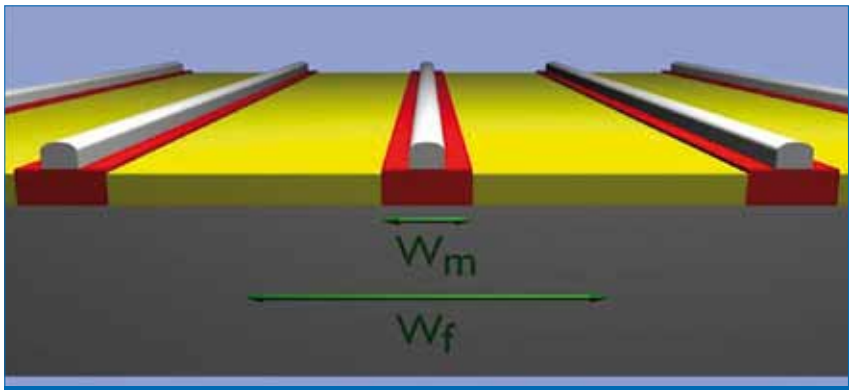

Figure 6. After masking and etch-back of the emitter there are two areas with high (red) and low (yellow) surface dopant concentration. Depending on the ratio of masking width (W_m) to finger pitch (W_f), the initial phosphorus diffusion process must be tuned to optimize cell performance.

Optimizing SE technology in production

Aside from the etch-back process parameters themselves, several parameters in the preceding and subsequent processes can be adapted in order to maximize the benefit of implementing SE technology. These parameters include emitter diffusion, mask design, etch-back depth, emitter passivation and design of the emitter electrode. Each technology will be discussed separately. Although many process parameters are interdependent, it is still helpful to consider the basic characteristics independently.

Adapting phosphorus emitter diffusion

The first process that had to be adapted in the production sequence was the dopant-depth profile of the n-type phosphorus emitter. The standard production process typically features an emitter sheet resistance of 60–70Ω/sq, diffused in a batch furnace system. While sheet

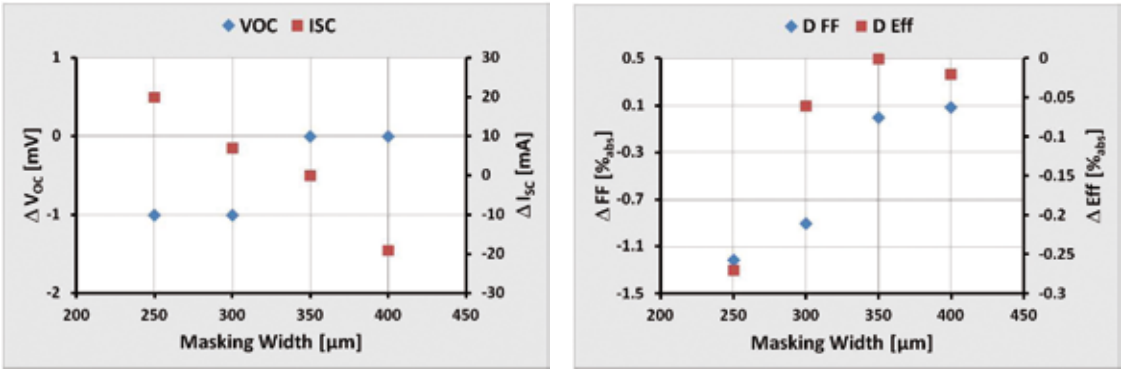

Figure 7. Influence of masking width on V_{oc} and I_{sc} (left) and on *FF* and cell efficiency (right).

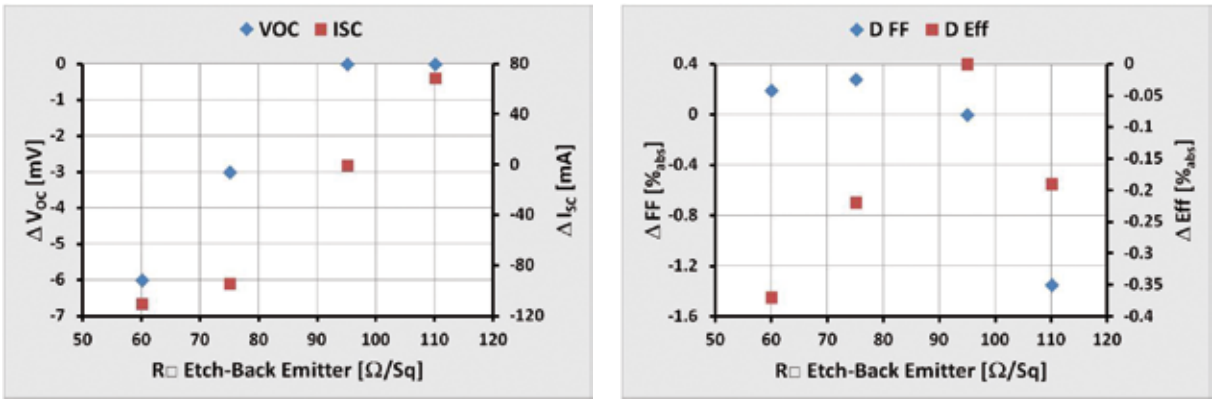

Figure 8. Influence of etch-back emitter sheet resistance on V_{oc} and I_{sc} (left) and on *FF* and cell efficiency (right). Initial emitter sheet resistance was 40Ω/sq.

	Eff [%]	I_{sc} [A]	V_{oc} [mV]	*FF* [%]	R_s [mΩ]	R_{shunt} [Ω]	I_{rev} [A]
Avg.	18.968	8.953	640	79.09	2.92	1358.59	0.126
Std dev.	0.0874	0.0335	1.5	0.2960	0.2	413.11	0.1487

Table 1. Daily average values of electrical parameters in Sunrise's production line.

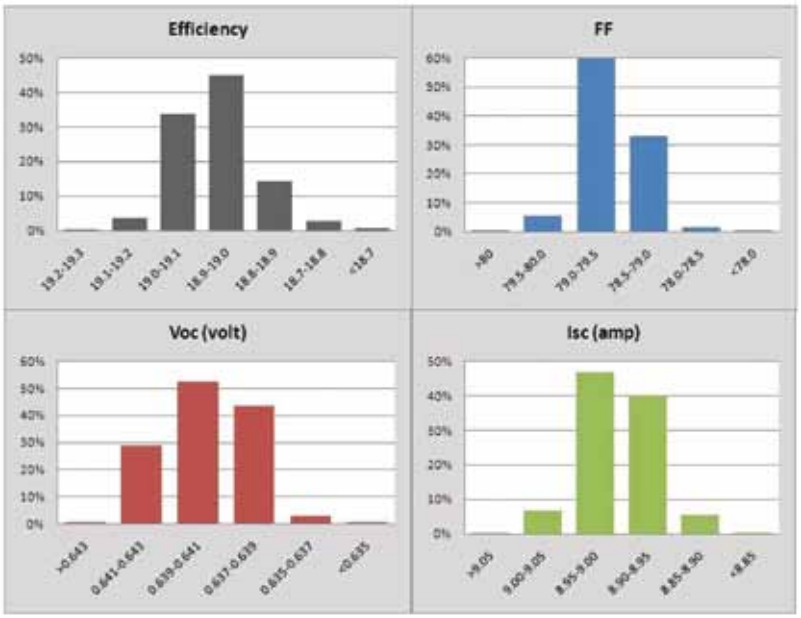

Figure 9. Distribution graphs for efficiency, *FF*, V_{oc} and I_{sc} of the etch-back SE cells produced at Sunrise.

resistance uniformity plays a critical role in homogeneous emitter designs, it becomes less important in SE technology. The first tests in production were carried out by varying emitter sheet resistances between 25–60Ω/sq. Although contact resistance of the emitter electrode to the emitter decreases with lower emitter sheet resistance, recombination in the emitter and at the SiN_x:H/n-Si interface increases with higher dopant concentration.

Typical findings show that, even though the emitter of all groups has been etched back to 80Ω/sq, a better cell efficiency is achieved when starting from a higher emitter sheet resistance before etching. The reason for this behaviour is well understood. To maintain high dopant concentration, part of the emitter surface is masked during emitter etch-back, and this area suffers from increased carrier recombination.

Depending on the ratio of masking width (W_m) to finger pitch (W_f), recombination in the masked area can offset some of the gain that an etched-back emitter will produce. Thus, the initial sheet resistance of the emitter should not be chosen too low, otherwise excessive carrier loss will occur in the area protected from the etch-back process. The slightly higher initial emitter resistance should not pose any problem in the region where the electrode contacts the silicon, because recent developments in Ag paste allow the metal to form a low-resistance contact with a more lightly doped emitter.

> "Typical findings show that a better cell efficiency is achieved when starting from a higher emitter sheet resistance before etching."

Masking width

In order to benefit from low contact resistance of the emitter electrode, it is essential that high dopant concentration at the Si/Ag interface is maintained. Thus, for screen printing, the emitter electrode should be correctly aligned with the areas masked before the etch-back process. Since the areas that are required for alignment tolerances are a source of electrical loss, it is important that these are kept as small as possible. Ideally, masking of the highly doped emitter before etch-back would be limited to just the area covered by the emitter electrode. This can be done in a laboratory environment, where overlay of masking and metallization can be very precise. In large-scale production, however, the positioning accuracy of the inkjet tool used both for masking and for metallization (screen printer) has to be taken into account when choosing the masking width.

Typically, during ramp-up of the process, a masking width W_m of 450µm was chosen. As operators and engineers gained more experience in overall process tuning, the masking width was able to be reduced. It was found that alignment accuracy becomes limited by gradual distortion of the screen during printing.

Normally, reducing W_m to 300µm and below does not lead to an increase in average efficiency on a mass-production scale. This is because there is higher likelihood of misalignment of the heavily doped area and the emitter electrode. This misalignment will cause two distinct effects:

1. Contact resistance of the emitter electrode to the emitter increases locally; cell series resistance increases, thus lowering *FF*.

2. Emitter electrode (Ag finger) contacts the lightly doped emitter, which causes increased recombination and leads to a decrease in V_{oc}.

Passivation of the contacts will be reduced because of lower emitter doping at the n-Si/Ag interface, causing increased recombination that leads to an increase in the emitter saturation current density j_{0e} [2] and a decrease in V_{oc}.

Choosing a masking width that is too narrow to allow accurate alignment of the emitter electrode generally leads to a larger spread in cell efficiency and a lower average cell efficiency. Apart from inkjet- and screen-printer alignment accuracies, distortion of the screen-printing mask over time has to be considered. In contrast to other SE technologies, the etch-back approach features a deep p-n junction. This is helpful as it avoids shunting of the cell in the case of minor misalignment, thereby retaining production yield. In 2011 more advanced equipment became available that allowed online monitoring of alignment precision, further facilitating process control [5]. An example of such equipment is the high-precision alignment camera in screen-printing tools.

> "To achieve the desired etch depth, measurement of the layer thickness is used to fine-tune the etch-back process in-line."

Etch-back process control

It is essential to exert very tight control over the etch-back process. This is realized through the generation of a porous silicon layer during the etch-back process, as mentioned earlier. To achieve the desired etch depth, measurement of the layer thickness is used to fine-tune the etch-back process in-line. The etch-back process is self-adjusted through the implementation of a closed-loop feedback controller. By using this cycle of direct feedback for process control, it is possible to achieve very high process stability in the etch-back process, resulting in high line yield. From knowledge of a simple correlation between etch-back depth and emitter sheet resistance (Fig. 3, left), the target sheet resistance of the emitter can be adjusted very precisely. Electrical cell data from a test in which the etch depth was varied are shown in Fig. 8.

If the etch-back is too shallow, the final emitter sheet resistance is low, resulting in only a small increase in I_{sc}. If the emitter is etched too deeply, the increase in I_{sc} will be offset by a low *FF* due to the higher emitter lateral resistance of the cell. The etch-back thickness optimization is strongly related to the final electrode pattern design as well. Moreover, in the case of multi-wafers, longer etching will cause excessively deep etching, commonly observed in the acid etching of multi-wafer material.

Recent result in mass production

Recent results of the implementation of etch-back SE technology in mass production at Sunrise are shown in Table 1 and Fig. 9. An average efficiency close to 19% is regularly achieved in large-scale production. Typically, over 90% of efficiency distribution falls within a 0.3% range, whereas 99% of the distribution falls within a 0.5% range. The distribution spreads and standard deviations of all the electrical parameters are quite small, showing that very tight process control is possible in a mass-production setting. Secondary electrical parameters, such as shunt resistance and reverse current, that are critical in module assembly are generally good.

Cell-to-module (CTM) loss in module assembly

SE cells inherently have higher short wavelength responses. It is therefore a common assumption that the benefit of higher efficiency SE cells will be lost at the module level because of EVA cut-off of the short wavelength light, resulting in a high CTM loss. However, such a problem is not specific to SE cells. Most higher efficiency p-type cells with homogeneous emitters typically rely on a lightly doped surface emitter, which is made possible by the front Ag pastes that are capable of making good contact to such a surface, resulting in a higher short wavelength response.

> "Applying a selective emitter to pursue high efficiency concepts has become imperative."

An SE cell typically has the additional benefits of a higher V_{oc} and *FF* owing to the low recombination in the emitter and at the Si/SiN_x:H interface, and low contact resistance of the emitter electrode, respectively. These cell features are generally preferable in modules. An improved spectral response at long wavelengths, resulting from better passivation at the surface, also partly contributes to the higher I_{sc}; such a benefit is completely retained at the module level.

The optimization effort during module assembly and superior module material (such as the use of narrower but thicker ribbons, more UV-transparent encapsulant such as silicone, and AR-coated front glass) can lead to considerably lower power losses. A CTM loss as low as 1.5% for monocrystalline SE cells, with efficiencies above 18.6%, has been achieved, resulting in 265W+ power output from a 60-cell module.

Outlook

In 2011 many cells were produced based on SE technology and different cell architectures, resulting in record efficiencies being achieved [6–8]. Applying a selective emitter to pursue high efficiency concepts has become imperative, since carrier surface recombination is now the dominant source of electrical loss in most monocrystalline cells. Recently, dielectric passivation of the rear surface has been shown to significantly increase electrical and optical performance of the cell, making reduction of front-surface recombination even more critical. For rear-side passivation, several concepts are currently under investigation or transitioning to pilot production, with an Al_2O_3 coating showing the highest promise. As soon as such cell architectures can be introduced into mass production, it will then be possible to exploit the full potential of SE technology to achieve the highest cell and module efficiency.

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