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Silicon solar cell fabrication in a CMOS line

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ABSTRACT

Solar cells are generally built in a process facility, often a turnkey line, where high throughput, minimum handling, and lowest cost are dominant factors. There are many complementary metal oxide semiconductor (CMOS) lines in the semiconductor industry – probably more than the number of turnkey lines – where yield, reliability, and device size and complexity are major issues, where millions of chips are made with very close tolerance, and the cost of importance is that of the finished chip. The possibility of using or converting a CMOS line for building Si solar cells has been considered by many in the past [2]. These lines have advantages such as sophisticated and highly developed automated equipment, frequent in-process metrology and quality control, and a high degree of flexibility as well as highly advanced shop floor control systems. The major disadvantages are cost and low throughput. This paper will discuss the differences, advantages, and disadvantages of CMOS and turnkey lines and show preliminary results for Si cells made in the CMOS line.

There are major differences between CMOS processing and turnkey processing, beginning with the starting material and including junction formation, electrode deposition, dielectric coatings, furnace processing, and the use of metrology. At IBM, a CMOS line has been used within the Research Division to explore typical CMOS processes as applied to building solar cells, studying techniques for enhancing the performance, and extending these enhancements to multicrystalline starting material.

Line comparisons

While many similarities exist between CMOS and conventional solar cell fabrication lines, there are also significant differences. Fig. 1 shows a step-by-step comparison of CMOS and turnkey processing as used for CMOS fabrication (left) or solar cell fabrication (right).

> "CMOS lots are generally processed in batches of 10–25 wafers, and the starting wafers all meet high specification standards."

CMOS processes start with polished wafers, usually 8- to 12-inch diameter round, as described in Fig. 2. Texturing is not used, and wafers are optimized for majority carrier properties. This sometimes includes a 'denuding' step in which annealing under specified conditions causes oxygen to precipitate in a zone 10–20 microns below the surface. This precipitated oxide acts as a gettering region to reduce unwanted impurities from the wafer surface. CMOS lots are generally processed in batches of 10–25 wafers, and the starting wafers all meet high specification standards. Impurity densities other than intended dopants are low, in total below $10^{12}cm^{-3}$, but oxygen is high ($>2x10^{17}$ cm^{-3}) to allow the denuding. There are no cracks or scratches and the surface roughness is less than 0.2nm.

Turnkey processing starts with smaller wafers, usually 125 to 156mm squares, that are rough cut, requiring saw damage etch as a first step. Texturing is carried out by acid solution for multicrystalline substrates or alkaline for mono-Si. Oxygen content is also high but there is no denuding step as the entire volume of the wafer is involved in cell operation, and creating a zone of high defect densities is detrimental to cell operation.

The minority carrier properties are key – lifetime and diffusion length in particular, while the majority carrier properties are only of interest for setting the wafer resistivity. There is a considerable variability in the starting wafer properties; impurity content, dislocation densities, and grain morphology vary across the wafer and along the ingot, and this variability contributes to the necessity of 'binning' of finished devices by efficiency categories. Impurity contents are several orders of magnitude higher than in CMOS wafers.

In CMOS lines, junctions are provided by ion implantation, generally phosphorus (but sometimes arsenic) for n-type layers and boron for p-type. Fig. 3 outlines features of ion implantation (I/I). Implantation is an expensive process but has significant advantages. Almost any desired element can be implanted and both the depth and dopant concentration can be independently controlled. A given element can be implanted using different species and ionizations such as B^+, BF_2^+, or BF_2^{++}, etc. The implant also causes 'damage'

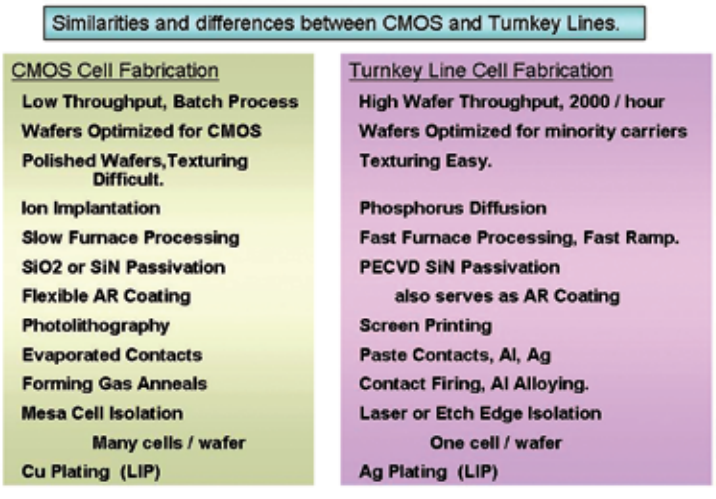

Figure 1. Comparison between CMOS and turnkey processing for fabricating Si solar cells.

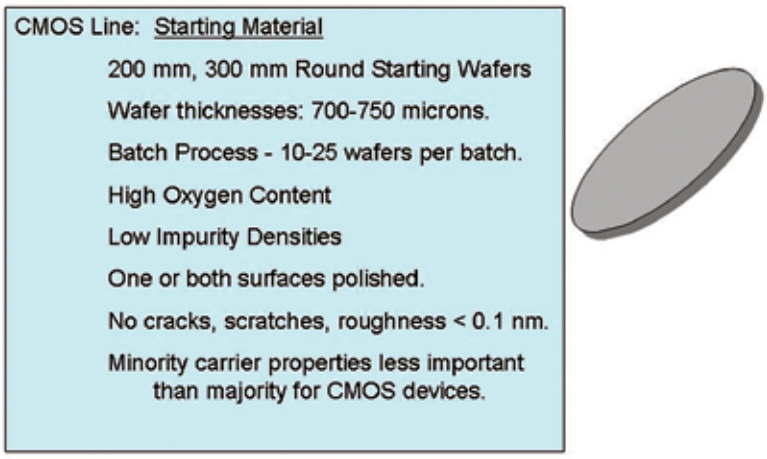

Figure 2. Properties of wafers used in CMOS processing.

in the form of displaced host atoms, and the implanted dopant does not 'sit' properly on substitutional sites, so a high temperature annealing is used to activate the dopant and minimize the damage. This can be furnace annealing or RTA (rapid thermal anneal), yielding a relatively low throughput. Selective emitter processing is straightforward using different doses and energies, but patterning is required to differentiate between the n^+ and n^{++} regions. Etch-back processes can also be used to create the selective emitter as is often carried out with diffused emitters.

"Dielectric coating technologies are one of the advantages of CMOS facilities."

Ion implantation can be adopted directly for solar cell fabrication, but the high cost and lower throughput prevent its widespread use. By contrast, emitter diffusion is fast and relatively low in cost, using $POCl_3$ or H_3PO_4 as phosphorus sources. Throughputs of several thousand wafers per hour are standard in turnkey lines. Dopant concentrations and depths are controlled by the dopant source and the high temperature/time of the diffusion, but are not as easily controlled as in implantation. Low cost and throughput are the major advantages of diffusion for solar cell build.

Furnace annealing in CMOS lines is used in many process steps such as dopant activation, silicide formation, and oxidation. However, conventional CMOS furnace processes tend to be slow, with slow ramp-up and ramp-down rates and lengthy dwell times at peak temperature, although rapid thermal anneal can be used for some process steps. Annealing is done in batches of 10 to 50 wafers and process times can be several hours. In turnkey lines, only the emitter diffusion involves a furnace, along with high-temperature contact firing near the end. These steps are usually continuous as opposed to small batches, resulting in the aforementioned thousands of wafers per hour.

Dielectric coating technologies are one of the advantages of CMOS facilities. CMOS devices utilize a variety of coatings, from SiO_2 and SiN to HfO_2, TiO_2, TiN, and others. A variety of deposition processes are available: LPCVD (low-pressure chemical vapour deposition), HPCVD (high-pressure CVD), PECVD (plasma-enhanced CVD), spin coating, evaporation and sputtering. There is great flexibility in the use of coating materials, thicknesses, multi-layer stacks, and deposition methods. On the other hand, turnkey manufacturers might argue that only PECVD of SiN is required. Nevertheless, improvements in anti-reflection and passivation might be obtainable making use of the greater flexibility and alternate dielectrics.

Contacts for CMOS processing are applied by e-beam and thermal evaporation or sputtering. These are relatively expensive and slow methods for applying metal coatings and a great deal of waste is encountered, since the metal layer is deposited over a wide area and not simply the desired contact areas. Photolithography is used to define the contact areas, requiring expensive optical equipment and multiple photoresist layer depositions and removals. The deposited metal layers are thin, generally less than 1 micron, and build-up of layer thicknesses to minimize sheet resistances is required. One advantage of contact processing with photolithography is that contact dimensions can be varied over a wide range, as wide as desired down to several microns in finger width.

An alternative being investigated is direct metal plating onto the device structures, and modern CMOS chips may utilize a mixture of deposition techniques and plating. These plating techniques are directly applicable for solar cell build.

Contacts in turnkey lines are made with screen-printing of Al and Ag pastes fired in RTA-like thermal processes. The Ag is fired through the SiN coating, while the Al is alloyed into the rear surface to form both a contact and a back-surface field (BSF). The grid pattern is formed by the screen. In CMOS manufacturing, there is no electrically active back contact, except in some cases for mounting purposes. However, ion implantation is easily adapted for rear surface processing, for example, implanting boron for the BSF in $n^+/p/p^+$ cells with a wide choice of doses and depths. Al or another metal would then be applied on top of the implanted BSF: Al is a common metal in CMOS processing, and alloyed Al to form the BSF would be easy to implement in CMOS lines.

Metal plating is common in both turnkey and CMOS lines. The plating, often light-induced plating (LIP), is used to build up the thickness of the screen-printed contacts for turnkeys and to increase the thickness or provide connections between contact

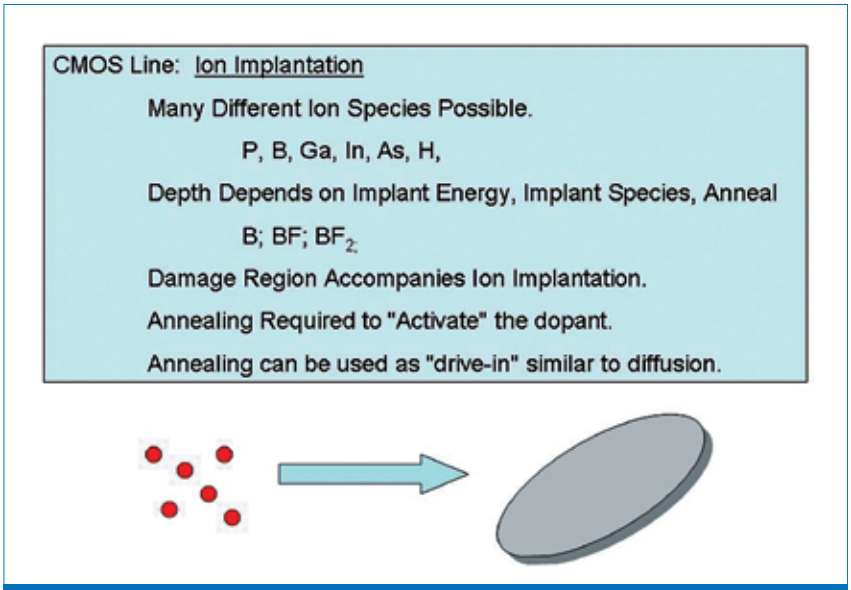

Figure 3. Ion implantation processing for CMOS and solar cells.

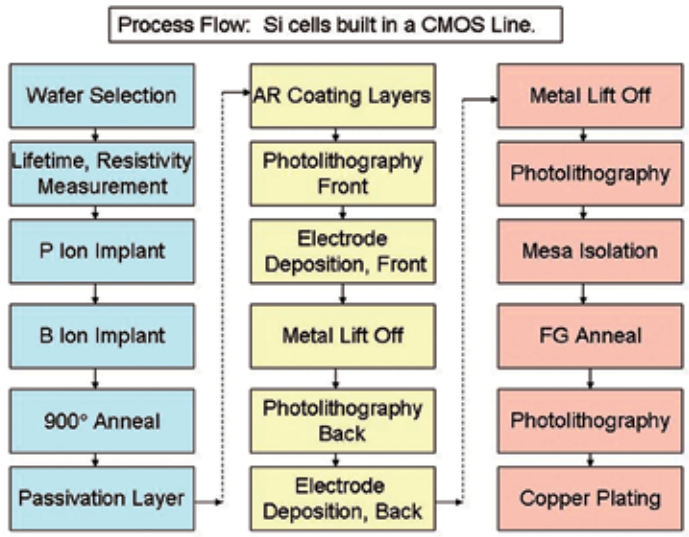

Figure 4. Process flow for fabricating Si cells in a CMOS line.

levels (M1, M2, M3, etc.) in CMOS devices. The success of metal plating in CMOS fabrication, particularly Ni, Ag, and Cu, can easily be extended to solar cell processing.

Another major difference between CMOS and turnkey lines is the use of metrology and statistical process control. CMOS manufacture makes use of extensive metrology at almost every step along the process. Starting material meets stringent resistivity, flatness, slip, surface roughness, and particle control, much of which is done at the wafer manufacturer. Single film thicknesses are measured by single wavelength ellipsometry or reflectometry and more complex layer stacks with spectroscopic ellipsometry. Sheet resistances are measured by scanning four-point probe or Eddy current mapping, surface roughness by AFM, and particle counts by optical scattering. Optical inspection is used at every critical process step, especially to inspect surface cleanliness after opening patterns in photoresist and dielectrics with RIE or plasma etch, which can leave polymer residues. Records are kept of thousands of key parameters of wafers and statistics are used to ensure process repeatability and integrity. Each wafer is identified by a unique code and traceability is of high importance.

> "Sheet resistances are measured by scanning four-point probe or Eddy current mapping, surface roughness by AFM, and particle counts by optical scattering."

Solar cell fabrication in turnkey lines generally uses less metrology in the interest of cost and throughput, and wafers presently have no traceability. Process control is addressed by the final cell results and their analysis, while wafer and process variability are manifested in the efficiency binning. The value and importance of wafer quality control and metrology techniques to assess quality is beginning to receive wider recognition [1].

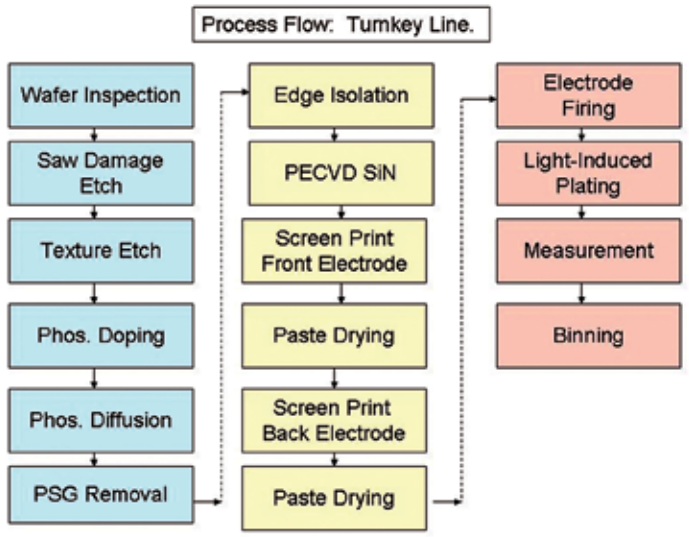

Figure 5. Process flow for fabricating Si cells in a turnkey line.

Examples of process flows for fabricating solar cells in CMOS lines and turnkey lines are shown in Figs. 4 and 5. The major differences, as has been mentioned, are in the emitter junction formation, BSF formation, use of photolithography instead of screen-printing, evaporated or sputtered electrode material, and plating. Mesa isolation in CMOS processing is equivalent to edge isolation in turnkey processing. Differences also arise between different turnkey processes; some make use of $POCL_3$ diffusion sources and belt furnaces, while others utilize H_3PO_4 mists and batch furnaces, and edge isolation is carried out in different ways and at different stages. The phosphorus diffusion capability enables the use of gettering as an added process step in turnkey lines to improve starting material quality. Diffusion can be easily implemented in CMOS lines.

Wafer sources and process lines: a cost comparison

For assessing the costs of Si cells manufactured using a CMOS manufacturing line, a number of factors need to be considered. The first is what type of starting material will be used. Options include solar-grade square wafers, mono- or multicrystalline, UMG, or 'scrap' semiconductor-grade CMOS wafers. If scrap CMOS wafers are used, the wafers are nearly without cost as they would otherwise be thrown away or used as raw Si feedstock for new ingot build; in any case they are no longer usable for CMOS production. The second factor is tool usage according to manufacturing priorities in the CMOS line.

> "The CMOS line may be converted to only solar cell build and the equipment may be fully depreciated by prior CMOS manufacture."

If the line is to be used for both CMOS and solar cell fabrication, the solar production might bear some of the depreciation cost. However, the solar wafers can be loaded in front of the manufacturing tools, according to the process step to be applied, and wait until the tool is idle. Therefore, equipment depreciation is less of an issue, because this method helps maximize the utilization of the production machines which might otherwise lay idle.

Alternatively, the CMOS line may be converted to only solar cell build and the equipment may be fully depreciated by prior CMOS manufacture. This is the most cost-effective scenario for using such a line for solar cell fabrication.

Cost estimates for solar cell manufacture have been carried out for scrap CMOS wafers where multiple cells are made on a wafer and used in CPV approaches, and for mc-Si and UMG square wafers with one device per wafer as standard in the industry. The process yield had been assumed to be 95%.

The wafer manufacturing cost for such a setup is shown in Fig. 6, making use of scrap CMOS wafers and converting into power output for 15% efficient devices. One wafer contains several hundred cells, each 1 x 1cm^2, adding up to around 8W per wafer at one sun. The volume build concerns numbers of wafers manufactured per year (125k wafers in the case of 1MW), with around 8W per wafer.

For round wafers with a 200mm form factor and fabricating 1 x 1cm^2 dies can yield around 500 dies per wafer; the cost per Wp for various efficiencies is shown in Fig. 7. The cost improves with increasing efficiency as well as increasing volume.

The cost per Wp is within the range of US$0.15 up to US$0.6 which is fairly low, especially at high volume build. The chart in Fig. 7 reflects the same assumptions as outlined earlier. The wafers have several hundred cells and the efficiency range used for cost calculation is from 15% up to 18%. These cells are used in single sun application for the purposes of calculation; as expected, the cost figures improve with increasing efficiency. The die and chip cost are shown in Fig. 8, where the dies are the individual cells cut from the wafer and the chips are the finished solar cells made from the dies.

Both the die and the finished chip (1 x 1cm^2 solar cells) boast attractively low costs. The power per die or chip ranges from 15.1mW up to 18.2mW for the 15% to 18% efficiency range. The chips can be used in CPV applications with proper device design to obtain much higher power output per cell, depending on the concentration ratio.

The approach as discussed is capable of providing solar cell devices from semiconductor scrap at very low cost ratios. The cells can be used directly in CPV applications or mini module designs. Mini modules, with a larger number of cells, would be assemblies created using the 1 x 1cm^2 cells. Module assembly must be performed using high automation and technologies such as pick & place and PCB (Printed Circuit Board) in terms of connections, etc. A typical flow from scrap wafer to solar wafer and finished die/cell is shown in Fig. 9.

The use of UMG material or regular solar-grade material such as multicrystalline wafers will cause the cost curves to move up due to the higher wafer material cost. Using UMG or solar-grade material estimates indicate that cost per Wp figures fall to US$1 and below; however, this does not take into account equipment depreciation. All facility and operational as well as material costs must be included in order to achieve a realistic calculation.

There are certain requirements that must be realised in order to be able to manufacture these wafers in a regular CMOS manufacturing line. Solar wafers, in this scenario, must be handled by the CMOS equipment and must be adapted for handling square wafers, possibly with different form factors. The related cost is considered in the calculations. Fig. 10 shows the cost estimate for solar-grade and UMG material at several efficiency levels, using a form factor of 156 x 156mm for the processing of the cells.

The highlighted area in Fig. 10 shows that processing solar wafers in a depreciated CMOS line using adapted handling can be profitable, especially in the case of high volume production.

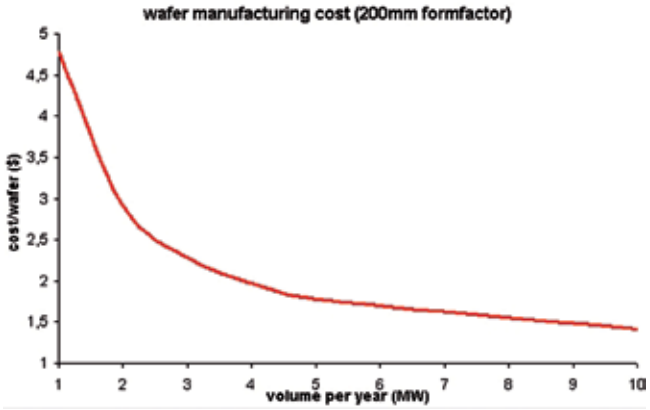

Figure 6. Wafer manufacturing cost curve vs. volume build.

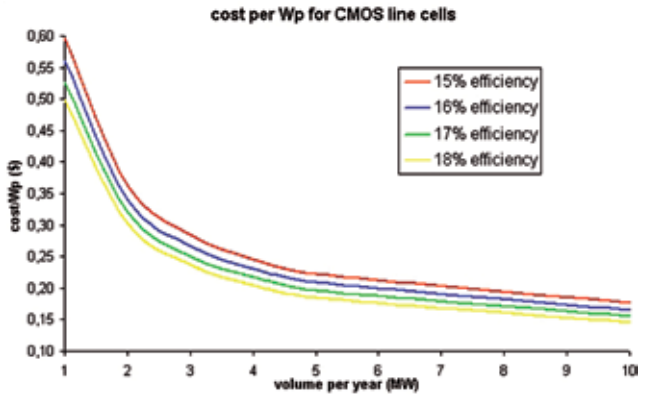

Figure 7. Cost per Wp vs. volume build.

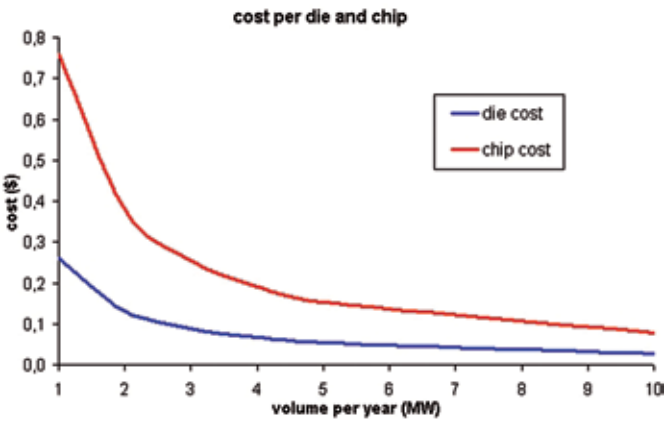

Figure 8. Die and chip cost curves vs. volume build.

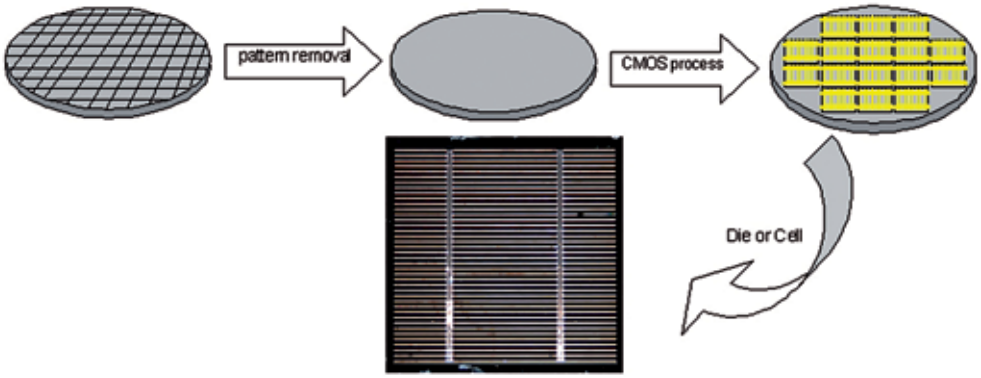

Figure 9. Typical flow in CMOS line from scrap to solar wafer.

Extension to thin solar cell processing and alternate cell structures

Thin solar cells take many forms, from thinner 'bulk' wafers to thin films of Si grown on glass, to amorphous Si and alternate materials such as CdTe, CIGS, and the new 'earth abundant material' cells known as CZTS (copper zinc tin sulphide). Process differences also become more divergent, involving roll-to-roll fabrication, nanoparticles, electroplating, evaporating, or spin-coating the absorber material and other layers in the cells.

The closest use of CMOS lines to thin cell fabrication would be in thin bulk Si where wafers of 50 to 100 microns in thickness are of interest. Processing of thinner Si layers mounted on foreign substrates is also possible. Fig. 11 shows some of the advantages and disadvantages of thin wafer processing in CMOS versus turnkey lines; wafer handling becomes a major issue in this regard. Although CMOS processing wins points due to process flexibility, it brings with it the disadvantage that the industry has little experience with processing of Si films on foreign substrates where tool modification and/or redesign might be necessary.

Alternative substrates such as metal, glass or graphite would be inappropriate were the line to be used for both the fabrication of CMOS structures and solar cells. This situation would be acceptable if the CMOS line were being converted into solar cell fabrication exclusively. Turnkey lines are already established with a minimum of handling and tools have been optimized to be applicable to solar cell processing.

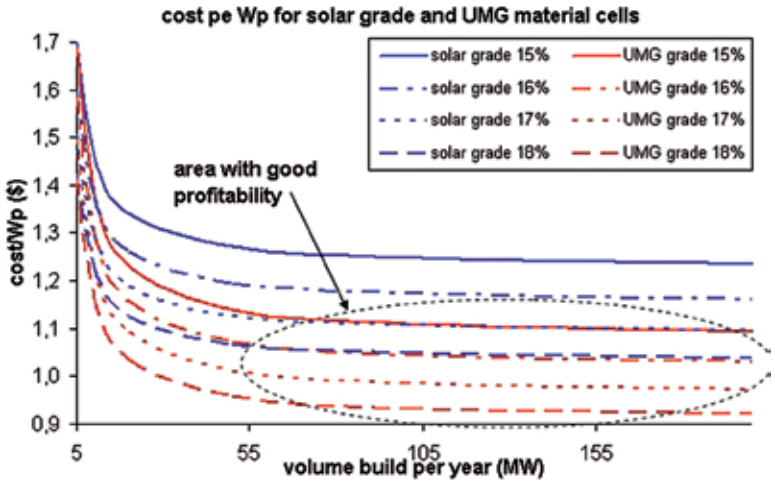

Figure 10. Cost per Wp vs. volume build for solar-grade and UMG material.

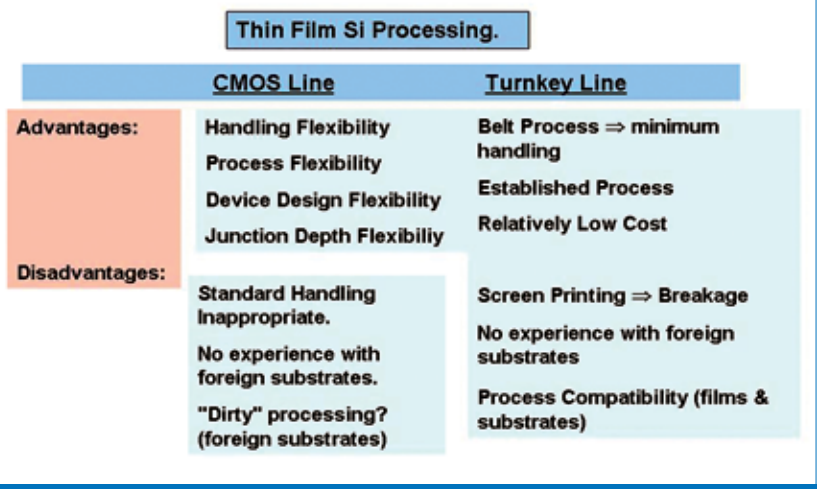

Figure 11. Advantages and disadvantages of CMOS and turnkey lines for thin wafer processing.

> "Laser doping, laser contact firing, and low temperature deposition of dielectrics for passivation and AR coatings are valuable for both CMOS and turnkey lines."

But despite the advances, some issues are problematic for both types of lines, such as those processes that have been designed for Si wafers and for which there has been little experience of dealing with cells on foreign substrates. Some alterations are necessary when using substrates such as glass, especially under allowable temperatures for junction formation and contact firing. Laser doping, laser contact firing, and low temperature deposition of dielectrics for passivation and AR coatings are valuable for both CMOS and turnkey lines.

CMOS lines are easily extendable to alternate Si cell structures such as HIT (heterojunction), IBC (interdigitated back contact) and amorphous Si or tandem cells. The processes and equipment used

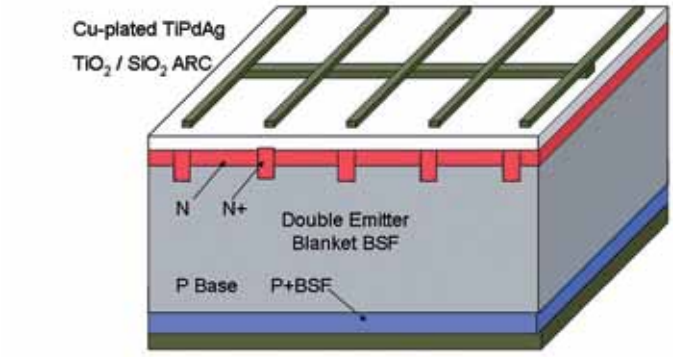

Figure 12. Device schematic, double emitter, blanket BSF device with thermal SiO2 passivation and high performance ARC.

to fabricate these cells such as PECVD and patterned junction formation are already available, while laser processing for monolithic integration can be readily implemented. The one missing piece for some structures in CMOS lines is TCO (transparent conducting oxide) deposition, but equipment such as CVD, sputtering, and spin or spray coating for the TCO is either straightforward to add or is already available.

Silicon solar cells built in a CMOS line – an example

For several years, Si solar cell research has been ongoing at IBM using the process sequence shown in Fig. 4. The starting material was 10Ω/cm p-type Si of 200mm in diameter and 700 microns thick, polished on one side and lapped/etched on the other. Wafers were selected for high minority carrier lifetime, which ranged from 400μsec to 1 millisec. Cells were made with either single or selective emitter ('double emitter' – DE) by phosphorus implantation, $1x10^{15}cm^{-2}$ dose at 10keV followed by 900°C anneal for 240 minutes. The BSF was made by $1x10^{16}cm^{-2}$ boron implantation at 80keV. The n^{++} dose for the double emitter contact area was also implanted at $1x10^{16}cm^{-2}$. Passivation was accomplished by a 10nm thermal SiO_2 and the AR coating was a double layer of either SiN/SiO_2 or TiO_2/SiO_2. The contacts were evaporated Ti/Pd/Ag with 10 to 20μm finger widths. Forming gas anneals at 450°C were used to activate the contacts. LIP Cu plating was used to build the fingers and busbars to 10-15μm thickness; busbars were 200 to 300 microns wide. Cells were isolated by RIE which created device mesas 3 to 5 microns deep. Cell areas ranged from $1cm^2$ to $4cm^2$ but some cells were made that were up to $20cm^2$ in area.

Fig. 12 shows a schematic of the cells made in this line. Most of these cells were double emitter with implanted emitter and BSF regions but for comparison reasons, single emitters and devices without BSFs were also made, while AR coating materials were varied and substrate materials down to 1Ω/cm resistivity were explored. Low resistivity semiconductor-grade substrates tend to have high oxygen content for denuding so that lifetimes in the lower resistivity material suffer from the boron-oxygen recombination centre.

Fig. 13 shows the internal quantum efficiency of cells made with and without the double emitter but without BSF in both cases. The single emitter doping level was 30Ω/⊗ with a peak doping of around $1x10^{20}cm^{-3}$. The band gap narrowing, low Auger lifetime, higher surface recombination velocity (SRV) and reduced diffusion coefficient combine to significantly degrade the short wavelength response and increase the J_O (junction leakage current), lowering the V_{OC} by 20–30mV. In contrast, the double emitter was 150–200Ω/⊗ with a peak doping

around $1x10^{19}cm^{-3}$, resulting in a flat response into the UV wavelength region.

The spectral responses of double emitter cells with and without a BSF are shown in Fig. 14. The effect of the BSF is clear from both the long wavelength response and the higher V_{OC}. On average, the BSF cells exhibited a 40 to 60mV higher V_{OC} than the non-BSF cells. Although the wafers are 700µm thick, the minority carrier lifetimes of 500 to 700µsecs in the finished cells result in an expected diffusion length of 1.2–1.4mm, allowing the BSF to participate in the cell output. The cells that have both DE and BSF exhibit nearly flat quantum efficiency throughout the visible wavelength range.

Currents as high as $40mA/cm^2$ have been obtained on these cells despite their lack of texturing and their highly polished surfaces. These high currents are a result of the use of high-performance double-layer AR coatings. Fig. 15 shows the reflectance spectra for SiN/SiO_2 and TiO_2/SiO_2 coatings. Simulations were used to optimize the thicknesses of the various dielectric layers. The SiN-based coatings average around 8% reflection over the solar spectrum below 1.1 micron wavelength while the TiO_2-based coatings average 4.9% over that range. The TiO_2-based coating has particularly low reflectance in the near IR just below the Si bandgap and in the visible down to blue wavelengths. The absorption loss due to the TiO_2 increases below the 0.35 micron wavelength where there are few terrestrial solar photons.

As this paper's aim was to investigate the properties of Si cells made with 'standard' CMOS processing, many experiments were carried out with and without DE and BSF, using different passivation methods, different AR coatings, and different contact methods (evaporation, sputtering and plating). Fig. 16 shows the results of a few of these runs, with particular emphasis on the AR coating options. The effect of the DE and BSF are clearly seen in improved V_{OC} and J_{SC}, while some variability appears in FF due to series resistance differences. The benefit of the higher-index TiO_2 coating (index µ 2.5) is also clearly seen. The main factor limiting the efficiency is the low V_{OC} value, which may be a consequence of damage or impurity inclusion during the implant. V_{OC}s as high as 0.625 were obtained in some devices at 25°C, probably 50mV less than expected. The use of diffusion, thinner wafers, and damage-/contamination-free implantation would raise these values.

Simulations using PC1D modelling have proven a good match to the cell results. Fig. 17 shows tables, charts, and graphs for the modelled and experimental results and displays reasonably close correspondence between the two. The model predictions of the benefits due to the DE, BSF, and improved AR coating are demonstrated in the cell results.

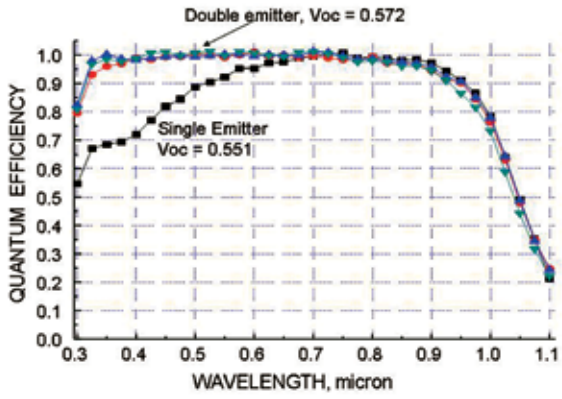

Figure 13. Internal quantum efficiency of single and double emitter (DE) Si cells with no BSF.

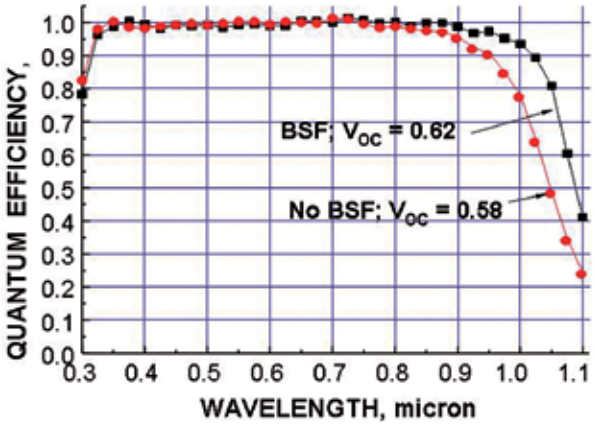

Figure 14. Internal quantum efficiency of double emitter Si cells with boron-implanted BSF.

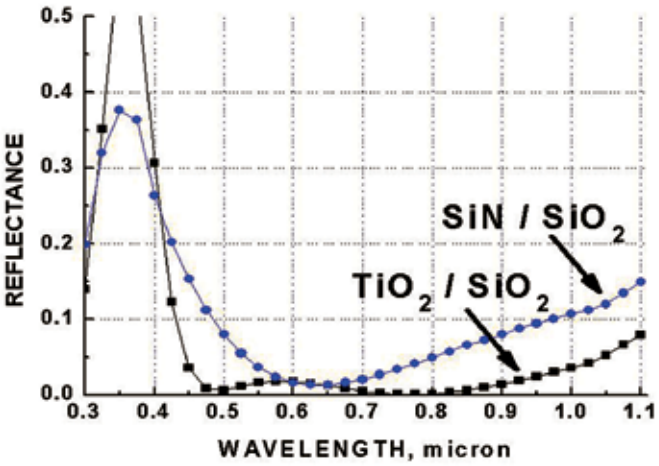

Figure 15. Reflection spectra of SiN- and TiO_2-based antireflective coatings.

The modelling can be used to predict the cell performance for devices manufactured in a regular semiconductor CMOS line, while advancements like the BSF, various passivation layers, selective emitter etc. can also be modelled, which helps the manufacturer to estimate future benefits and to determine if the advancement is beneficial in terms of cost and performance. A combination of the performance modelling with the regular cost estimation can yield a realistic cost analysis.

Evolution of CMOS lines to solar cell fabrication

CMOS lines have many advantages that make them suited to solar cell fabrication, including starting wafer quality control, precise and reproducible processing, a high degree of automation, extensive use of

Some Thick Film Si Solar Cell Results from a CMOS Line.

Device Lots with SiN/SiO_2 AR coating.

Device	Voc	Isc	FF	Effic.
SE, no BSF, SiN	.56	34.3	.78	15
SE, BSF, SiN	.605	35	.77	16.2
DE. BSF, SiN	.605	35.5	.78	16.8

Device Lots with TiO_2/SiO_2 AR coating.

Device	Voc	Isc	FF	Effic.
SE, no BSF, TiO2	.54	35.9	.74	14.3
SE, BSF, TiO2	.60	37.4	.77	17.5
DE. BSF, TiO2	.605	40	.75	18.1
DE. BSF, TiO2	.605	39.8	.775	18.7

Figure 16. Si solar cell parameters for cells with various processes and coatings.

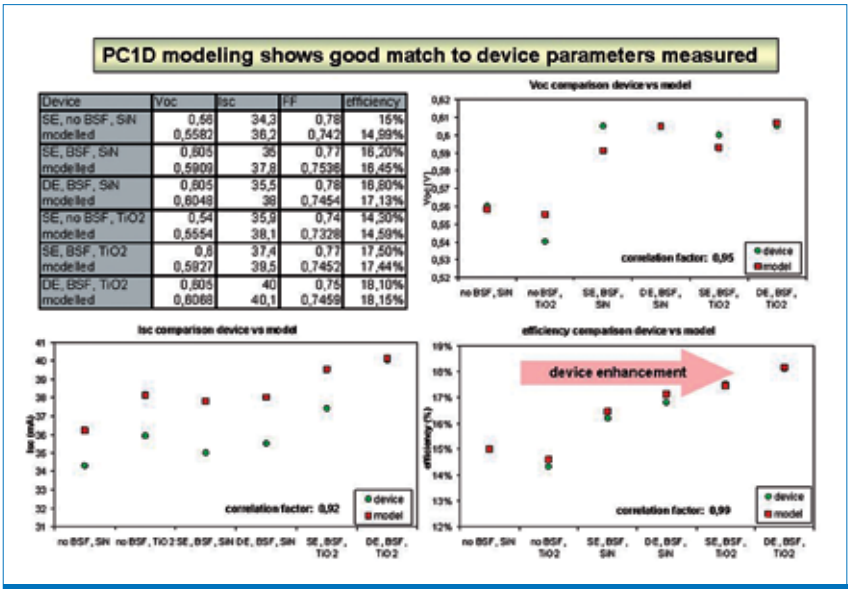

Figure 17. Comparison of experimental results and modelling with PC1D.

metrology, and highly developed process equipment. However, the adaptation of a CMOS line to cell fabrication requires a paradigm shift, as outlined in Fig. 18. Turnkey line cell manufacture could also benefit from several of these steps, but would require attention to such factors as acceptable cost per Wp, throughput, reduced binning distribution, and higher peak efficiency to ensure success.

The starting wafer variability is one of the key weaknesses in modern cell manufacturing, especially for cast multicrystalline wafers. Grain size, dislocation densities, resistivity, and impurity densities all vary from wafer to wafer and across the wafer, resulting in variability in minority carrier lifetimes, diffusion lengths, and shunting events such as conducting 'pipes'. Lifetime, diffusion length, and resistivity maps using photoconductivity decay, photoluminescence and eddy currents can show both the non-uniformities and the absolute values, allowing sorting of starting material and rejection of material which is sub-par [3].

> "The biggest paradigm shift would be in the furnace processing, where an in-line continuous wafer flow is considerably different from today's batch furnaces."

CMOS lines will have to adopt diffusion as the junction formation technology for the emitter and possibly for the BSF, though laser doping for LBSF (local back-surface field) could also be applied (as well as for the heavily-doped selective emitter regions). Adoption of phosphorus diffusion opens up the possibility of gettering for wafer improvement, which is useful for both line types. To maintain high throughput, gettering could be incorporated as a separate wafer preparation step prior to initiating the wafers into the line. Boron diffusion could be used for enhanced BSF compared to Al alloying; however, the low boron diffusion coefficient might require very high temperatures incompatible with the higher impurity levels in mc-Si wafers.

CMOS automation is presently set for round, thick wafers of 200 to 300mm in diameter. The line would have to be reconfigured for square wafers of 125 to 156mm on edge – these wafers are far thinner and more fragile, and wafer breakage of some fraction is inevitable. Any equipment would have to be able to withstand these broken pieces without incurring damage or reduced throughput.

CMOS lines are well equipped for dielectric layer deposition, notably PECVD SiN, and once equipment specifically designed for continuous wafer flow rather than batch fabrication is introduced, there would seem to be no barrier to entry for these dielectric deposition steps. The biggest paradigm shift would be in the furnace processing, where an in-line continuous wafer flow is considerably different from today's batch furnaces. Again, an equipment change would allow continuous flow, applicable also to etch and cleaning baths, which are now set for batch processing in CMOS lines.

Electrode deposition using plating would most likely be straightforward in CMOS, given that plating is already extensively used. Patterning that is now carried out with photolithography can be easily carried out by a variety of techniques including inkjet printing and stamping. Ni, Ag, and Cu plating are widespread in the semiconductor industry.

Laser processing is easily adopted into both CMOS and turnkey lines, with laser doping for both the selective emitter and the local BSF fast becoming well established. Benefits of laser applications include fast throughput, low wafer breakage, and self-patterning where the laser patterning is controlled by software and no physical patterning layer is required. The thermal budget is also reduced, lowering cost, improving the energy balance, and preventing temperature-induced changes in the wafer bulk.

It should come as no surprise that a CMOS line adapted for solar cell manufacture begins to look like a hybrid of a turnkey line. Many of the features of turnkey lines have to be utilized in CMOS cell manufacture in order to make it cost effective, especially those items which

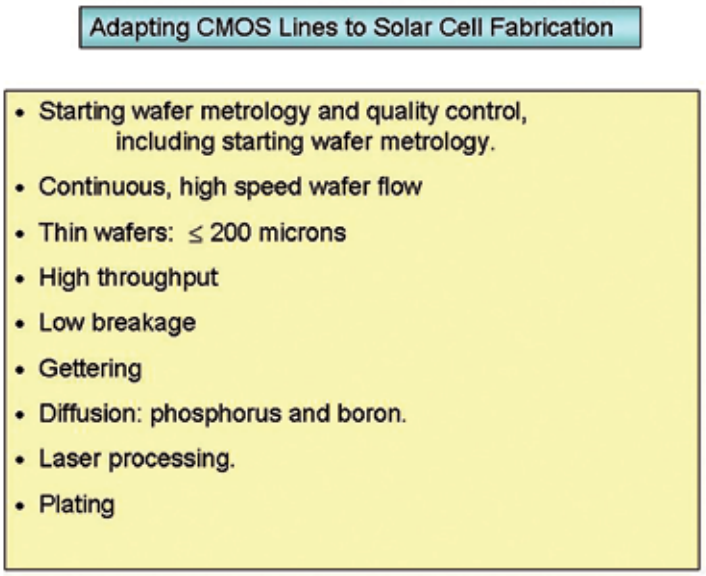

Figure 18. Conversion of CMOS lines for solar cell manufacture.

increase throughput and provide continuous wafer flow. However, features of CMOS manufacture such as starting wafer quality and selection, higher use of metrology, statistical process control and advances in automation would result in benefits to finished cell efficiency, binning distribution and average efficiency. A careful look at all the advantages and disadvantages of adapting a CMOS line to cell manufacture should be carried out with the goal of reaching an acceptable and hopefully reduced cost per Watt. A hybrid of CMOS and turnkey lines would incorporate the best features of both.

Conclusion

Similarities and differences between CMOS lines and turnkey lines as used for solar cell manufacture have been described in this paper. Both equipment and processing alternatives would need modification for large-scale Si cell fabrication in CMOS lines, with goals of greatly increasing throughput, accommodating the use of thin square wafers in place of thick round ones, and adapting processes and techniques that result in enhanced efficiency. CMOS lines and procedures such as starting wafer quality assessment and control and metrology for statistical process control could reduce binning distribution and increase average efficiency. Cost estimates suggest acceptable cost levels for Si cell technologies using scrap CMOS wafers for fabricating cells for low level CPV applications, or square form-factor solar and UMG-grade material using fully or nearly fully depreciated CMOS lines. The optimum process facility and set of procedures would make the best use of both CMOS and turnkey line features, adhering to the ultimate goal of high throughput and low cost per Watt.

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