

TCAD in the semiconductor industry and its advantages for solar cell manufacturing

Nick E.B. Cowern & Chihak Ahn, School of Electrical, Electronic and Computer Engineering, University of Newcastle-upon-Tyne, UK

ABSTRACT

Technology computer-aided design (TCAD) is pervasive throughout research, development and manufacturing in the semiconductor industry. It allows very low-cost evaluation of process options and competing technologies, guides process development and transfer to production and supports more efficient process improvement with minimal down time in the factory environment. This paper reviews the use of TCAD in the semiconductor industry and shows, with some illustrative examples, its important enabling role for the PV industry.

Introduction

Technology computer-aided design (TCAD) is a computer-based procedure used to predict the structure and performance of fabricated semiconductor devices. Within TCAD, 'process simulation' tools are used to predict the device structures formed as a result of a specific chain of processing steps, and 'device simulation' tools compute the electrical response of devices to boundary conditions, such as contact potentials/currents and compute energy inputs/outputs such as light and heat. TCAD simulation tools typically solve continuum equations for atomic or electronic transport. At nanometre length scales, techniques such as kinetic Monte Carlo are used to increase accuracy and gain insight into statistical variations, while at the atomic scale, first principle quantum calculations are used to determine fundamental parameters of materials and TCAD models. Structures computed by process simulation can be used in device simulation tools to explore the impact of process variations on device performance.

TCAD is widely used in the microelectronics industry to reduce process development time and costs, and to ensure optimal performance of fabricated devices. It is a key component of the International Technology Roadmap for Semiconductors (ITRS) and of every semiconductor IC manufacturer's research, development and production program. In recent years, TCAD models, especially those used to compute the effects of processing steps, have matured considerably as a result of widespread research in universities, institutes and companies over recent years [1,2]. Process models now require relatively little 'calibration' to specific Si-based technology processes.

At the same time, industry-standard device models have been extended to include opto-electronic interactions, thus enabling application to light-emitting devices and PV [3].

These advances have created a capability ripe for application in the PV industry, where the use of TCAD is rapidly

increasing but is not yet well established. As in the microelectronics industry two to three decades ago, the focus has mainly been on device modelling [4,5]. Little work is currently done (as of early 2011) to use integrated process and device TCAD to explore the impact of process changes on solar cell efficiency. Such investigations are often done using in-line processing experiments and expert intuition, despite difficulties in picking out true optima because of the many trade-offs between process parameters, and experimental fluctuations arising from processing variability and drift.

“Little work is currently done to use integrated process and device TCAD to explore the impact of process changes on solar cell efficiency.”

In this paper we look at the ways in which TCAD can accelerate enhancements in cell efficiency, often at very little or even negative cost – impacting strongly on industrial competitiveness, just as occurred historically in the semiconductor industry. This is illustrated using four examples: integrated process and device TCAD optimization of doping in an LGBC c-Si cell process; study of 3D current crowding effects in a cell with passivated rear side and local contacts; 3D simulations of emitter wrap-through (EWT) and metal wrap-through (MWT) cells; and a brief look at modelling light absorption in a textured thin-film solar cell.

Application of integrated TCAD to an established c-Si cell technology

This section explores the potential of integrated process and device modelling to optimize the processing of front-contacted solar cells with respect to

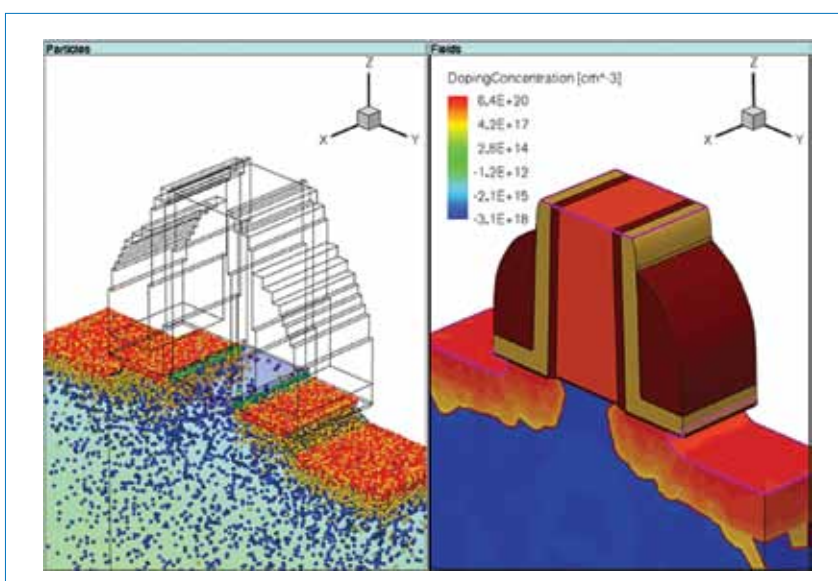


Figure 1. Atomistic 'Kinetic Monte Carlo' simulation of dopant atoms (left) and corresponding doping distribution (right) in a deep-submicron planar silicon MOS transistor.

Image courtesy of N. Zografopoulos, Synopsys.

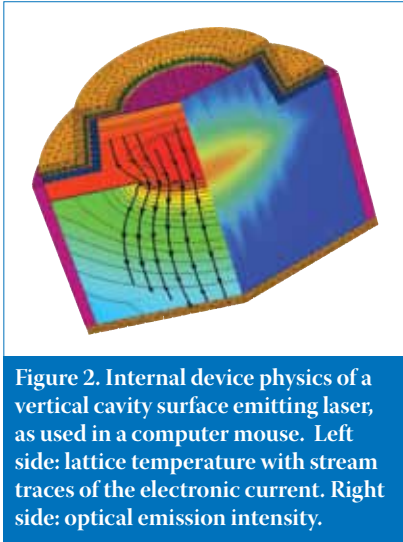


Image courtesy of Stejlan Odermatt, Synopsys.

Figure 2. Internal device physics of a vertical cavity surface emitting laser, as used in a computer mouse. Left side: lattice temperature with stream traces of the electronic current. Right side: optical emission intensity.

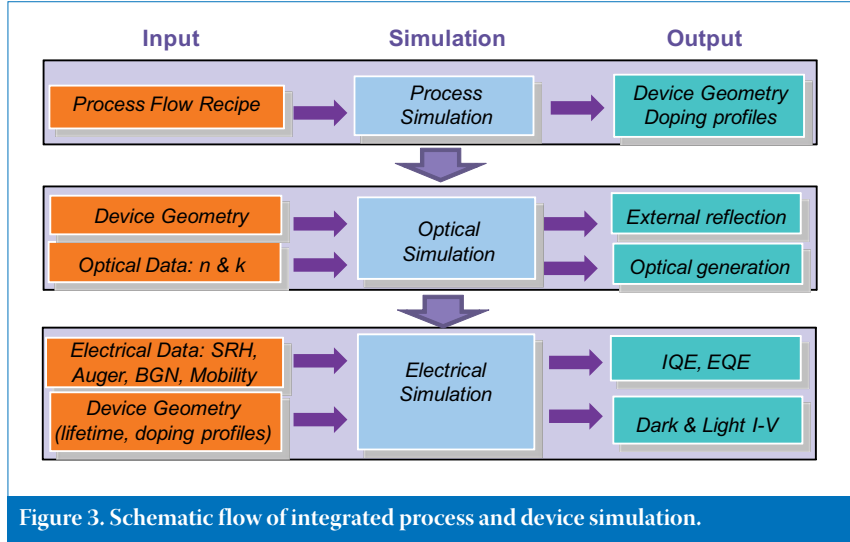


Figure courtesy of Synopsys.

Figure 3. Schematic flow of integrated process and device simulation.

efficiency. The example illustrated is a well established, well characterized technology: the laser-grooved buried contact (LGBC) solar cell manufactured by the UK National Renewable Energy Centre (Narec). Process simulations are compared to short-loop process experiments; integrated process and device simulation is then used to develop conclusions on trade-offs and potential further process optimization of the LGBC process [6]. Overall efficiency enhancements of ~1% appear possible, even before improvements such as local rear-side contacts are added.

The procedure used is similar to what is needed to explore a novel technology. We first discuss the modelling of the fabrication process and then use the resultant simulated structures as input information for device simulation of the operation of the fabricated solar cells.

Process modelling

The structure of the LGBC cell is reproduced in Fig. 4. It includes a shallow emitter, passivation/antireflection coating, laser-cut grooves, groove diffusion and Al back-surface field and contacts.

The evolution of the wafer structure during processing is modelled in 2D using the 1–3D simulation tool Sentaurus process [3]. Some of the advanced process models implemented in this tool have originated from collaboration with our group. The tool also provides an interface for specifying custom physical models, by coding them mathematically in a TCL-based language. We use this feature to model the POCl_3 deposition process and the back-surface field (BSF).

The range of length scales in a PV cell presents a challenge for process simulation. A manufactured cell usually has an area of

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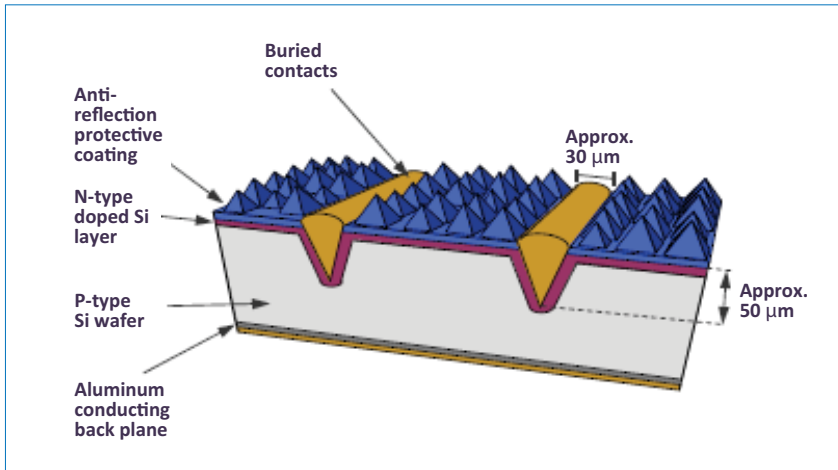


Figure 4. Schematic diagram of the LGBC solar cell structure.

are then translated or merged into the full simulation area for device simulation. Regions simulated are the shallow emitter, corner regions of the groove structure, and the BSF doping. Surface texturing used in manufactured cells is not explicitly modelled here, which influences some aspects of device simulation results. Modelling texture effects on light distribution is discussed in the last section of this paper.

The first step in the LGBC process is P deposition using a POCl_3/O_2 gas mixture. PSG is simulated as an oxide layer containing a high level of P, with calibrated interface states and P diffusivity. Fig. 4a shows the resultant trend in emitter sheet resistance versus deposition time. Measured values for planar non-textured

Figure courtesy of Narec.

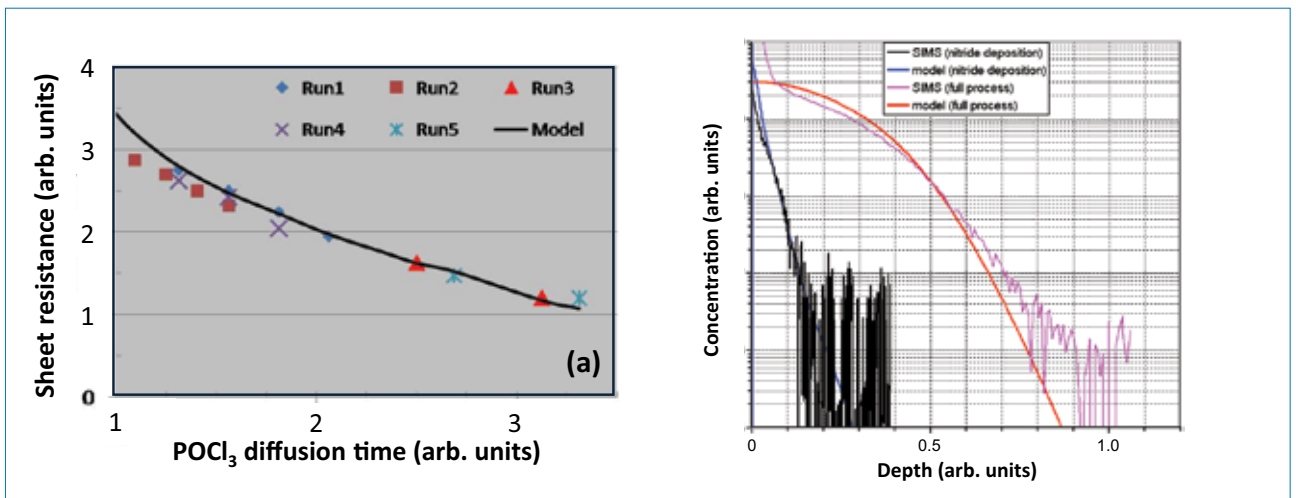


Figure 5. a) Emitter sheet resistance values after a thermal budget equivalent to the full LGBC process. Symbols show experimental data; the curve shows the simulation result. Indicated values are in arbitrary units. b) SIMS profiles and model simulations for the phosphorus emitter profile after nitride deposition, and after full thermal process.

100cm^2 or more, while diffusion features can be less than 100nm deep. We take advantage of the repeating finger structure to model an 'elementary' cross-section through the cell, extending laterally between the

mid-points of two adjacent pairs of fingers and vertically right through the wafer. To save further computation time, process simulation is restricted to areas where the dopant concentration varies. The results

wafers are well described by the model simulations, and SIMS measurements of P emitter profiles (Fig. 4b) are also in reasonable agreement. The resulting calibrated model is used to study the effects of different thermal cycles for the emitter diffusion.

The next few simulation steps see the nitride being deposited, the laser-cut groove structure is modelled, and a high temperature POCl_3/O_2 diffusion selectively dopes the groove region with a high P concentration. This completes the doping steps for the front side of the wafer; however, a further thermal budget arises from the subsequent BSF anneal. As a result the emitter and groove diffusion profiles broaden further. Fig. 6 shows the groove diffusion profiles obtained under the same annealing conditions as for the emitter diffusion in Fig. 5b. The calibration established for the emitter diffusion works equally well for the groove diffusion profiles, without any need for adjustments.

The following steps are used to model formation of the BSF and Al alloy back contact. Al is deposited and Al diffusion

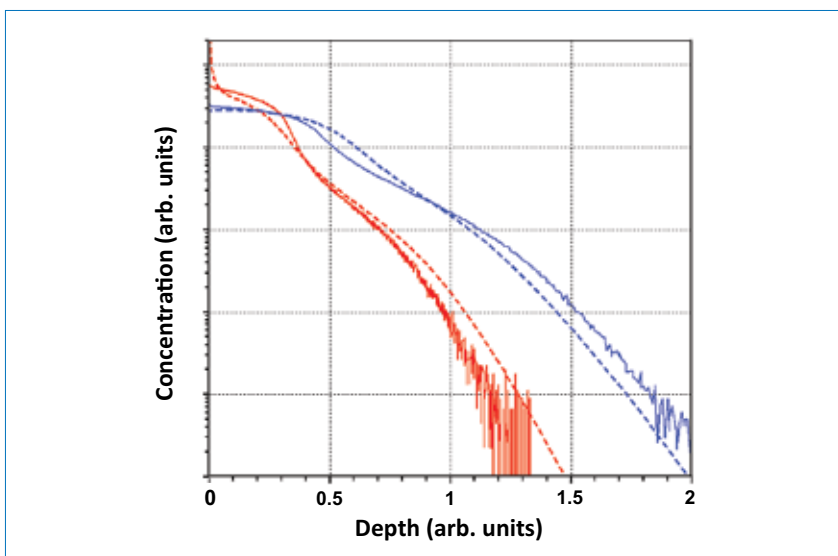


Figure 6. Experimental and simulated groove diffusion profiles after nitride deposition (red); at end of process (blue).

into the wafer is modelled by assuming that an Al-Si alloy has formed and the Al concentration on the silicon side of the alloy/silicon interface is equal to the solid solubility limit for Al in silicon at the diffusion temperature. During cool-down from the peak set temperature, diffusion is neglected and the Al doping profile is controlled by epitaxial regrowth of Al-doped silicon following the thermodynamic model derived and experimentally confirmed by Lölgen [7]. The p-type doping profile resulting from this thermal cycle is shown in Fig 7. This curve is an uncalibrated simulation and does not necessarily correspond to the true doping profile in the existing Al BSF process.

The proposal by Lölgen to incorporate B with Al for a higher concentration BSF [7] is modelled as an alternative process option. The model assumes that the thermodynamic properties of the liquid alloy are unaffected by the presence of B at the level of a few percent, and that, with such B concentrations in the alloy, B is incorporated during regrowth at its solid solubility limit in silicon, an order of magnitude higher than for Al [8].

Device simulation

The geometry used for device simulations of the LGBC cell, including the simulation grid, is shown in Fig. 8. The structure is contacted along the back side (base contact) and along the groove surface (emitter contact). Simulations using the Sentaurus device tool are performed as follows. Reflection and transmission of light at material interfaces and light absorption in Si are calculated using the transfer matrix method (TMM). Electronic transport is simulated largely using default device models at 300K. Doping-dependent recombination (SRH and Auger), carrier mobilities and bandgap narrowing are taken into account. The contact resistance of the groove finger is determined from room temperature measurements on fabricated cells with a range of dimensions. The front surface recombination velocity is set to 7500cm/s. The simulation assumes AM1.5 solar radiation incident normal to the cell surface.

Results for the total current in the cell are shown in Fig. 9. Most electrons flow upwards into the emitter and along into the groove region. Here, as Fig. 10 shows, they flow down around the groove, sinking into the contact at a rate limited by contact resistance. Before the current reaches the groove bottom, most electrons have entered the metal. Thus, contact resistance does not significantly bottleneck the emitter current at the groove dimensions used.

In addition to electron current arriving from the emitter, a small proportion of electron current (about one to three percent dependent on groove width and

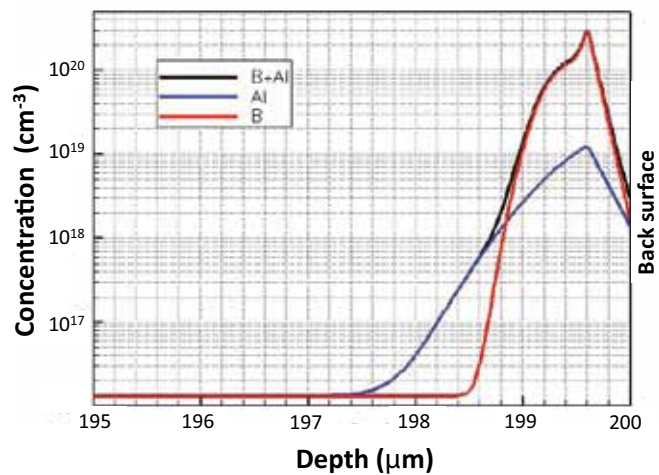


Figure 7. Simulated BSF doping profiles deposited using Al (existing process, blue curve), or Al:B alloy (black). The red curve shows the B concentration profile in the Al:B case.

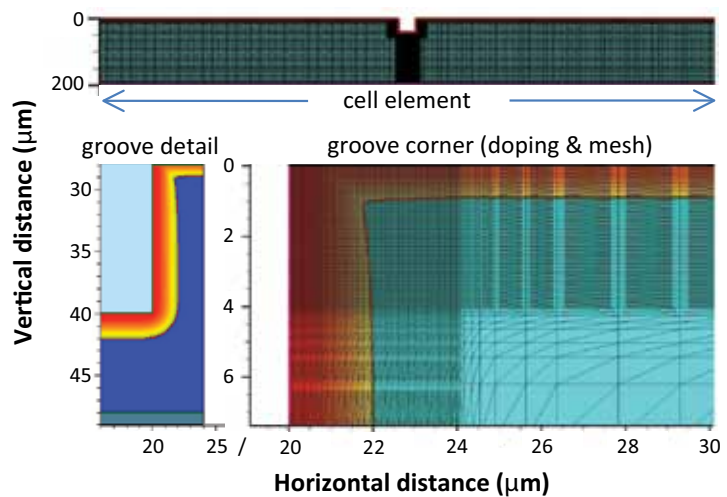


Figure 8. Geometry of simulated cell element (top) and details (bottom) showing the doping and mesh close to the groove. The emitter junction is marked by a solid line. The area below the groove (top) appears black due to the locally high density of mesh lines.

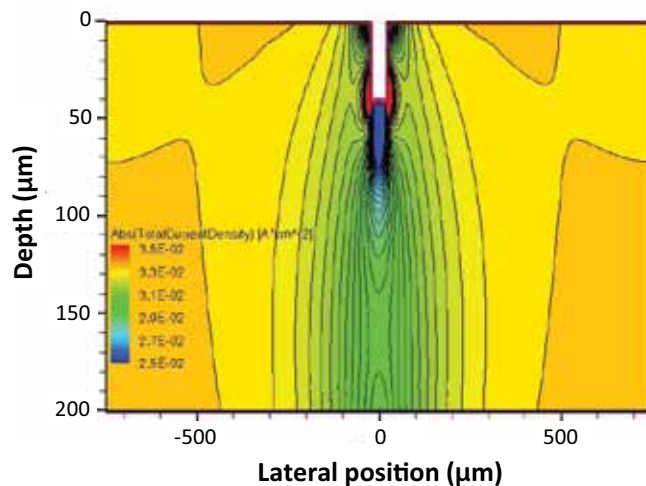


Figure 9. Simulation results for total absolute current in the full simulation unit cell (for a 200μm-thick wafer).

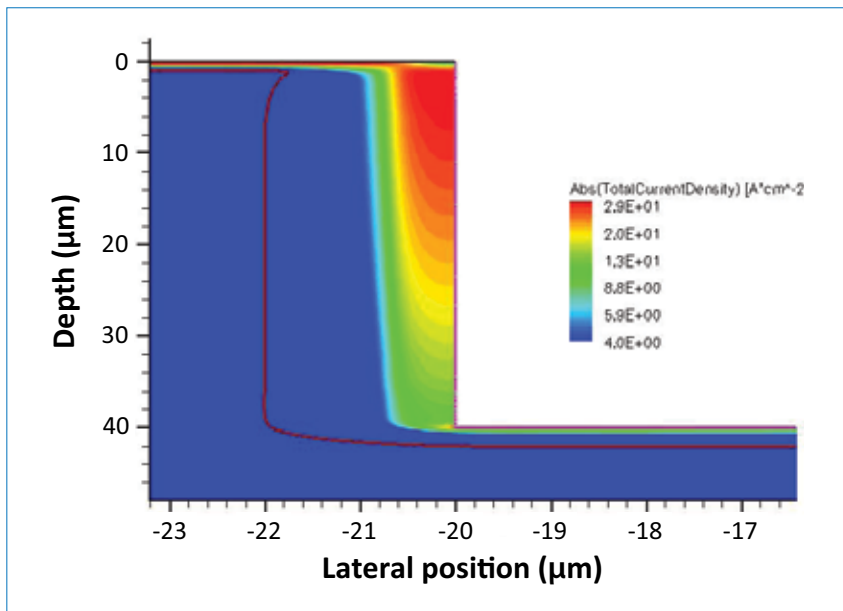


Figure 10. Current flow into the groove. Contact resistance causes the current to enter the contact over an extended area. The horizontal scale is expanded to 10× the vertical scale.

spacing) enters the groove directly from the base region. The impact of this current on the overall operation of the cell is quite small, and so the current flow in the base can be viewed as quasi-1D, while that in the emitter/groove region is inherently 2D.

Integrated simulations of the impact of processing on cell parameters

By sequentially running process and device simulations, the impact of a given series of process steps on cell parameters such as V_{oc} , I_{sc} , FF and efficiency can be evaluated. By varying input process parameters – diffusion temperatures, deposition thicknesses, groove width and spacing, etc. – an accurate picture of the process sensitivities of the cell technology can be obtained. This clarifies the potential optimum efficiency of the process, how closely this has been approached in current manufacturing processes, and what steps may be taken to improve efficiency further.

“TCAD, often used together with experiments, can help push the envelope of cell efficiency.”

In general, this approach can be used to evaluate both the impact of cell geometry and the impact of altering processing steps on cell performance. Here we focus on the impact of changes in processing steps. The effects of modifications to the emitter and BSF doping processes have been evaluated in some detail. Efficiency at AM1.5 illumination is shown in Fig. 11 as a function of P (n-type) emitter deposition time. This shows the benefit of a lightly doped, shallow emitter, if surface recombination is well controlled.

Finally, as illustrated in Fig. 7, adding B to the BSF enables a peak p-type doping concentration $> 10^{20} \text{cm}^{-3}$, an order of magnitude higher than with Al alone. Device simulations show that the resulting decrease in back surface recombination enhances the cell efficiency from a nominal 17.5 to 18.1% (an increase of 0.6%).

These results illustrate the cost-effective way in which TCAD, often used together with experiments, can help push the envelope of cell efficiency. This is true even for a process that is well established and appears at first sight to be fully optimized.

Simulation of cells with localized back contacts

The efficiency of cells with localized back contacts of varying size has been explored by Huang and Moroz [9], using the Sentaurus Device tool [3]. Their simulations allow for different reflectivities (Fig. 12) and different surface recombination

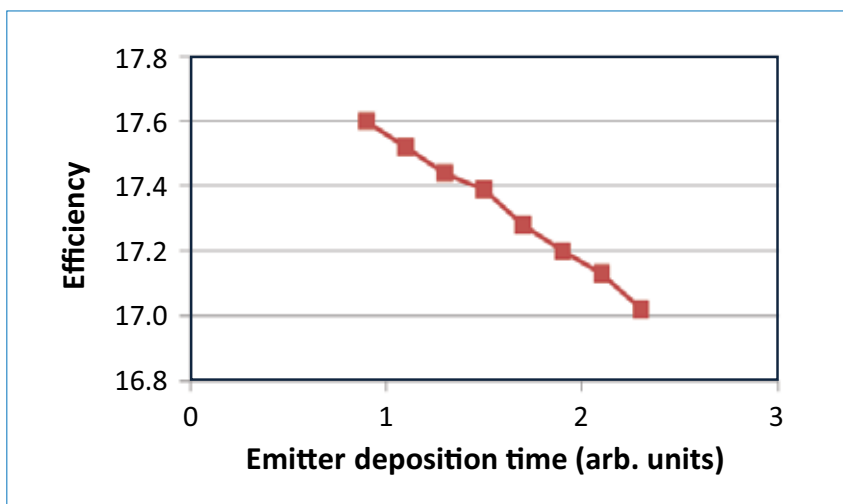


Figure 11. Simulated efficiency of the final fabricated cell, plotted versus the duration of the emitter deposition anneal.

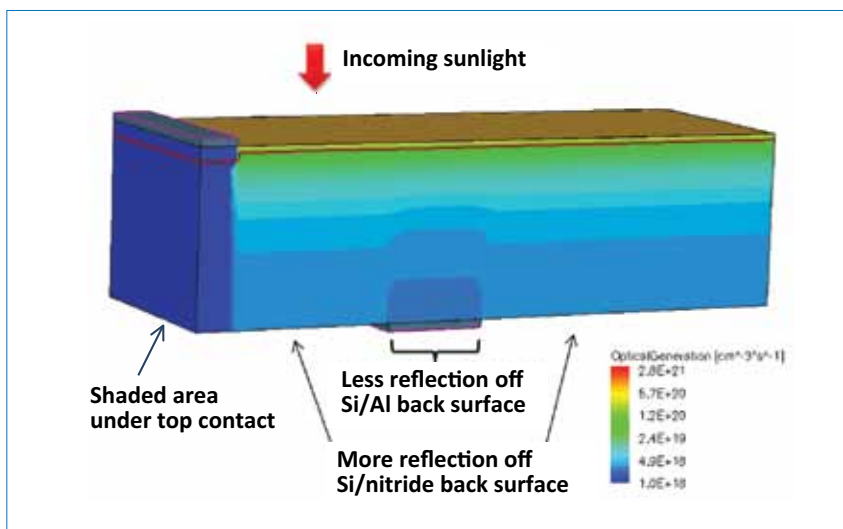


Figure 12. Optical intensity in the cell element as a result of front-side finger shadowing and different reflectivities at the back contact and back-side passivating Si/nitride interface.

Image courtesy of V. Moroz, Synopsys.

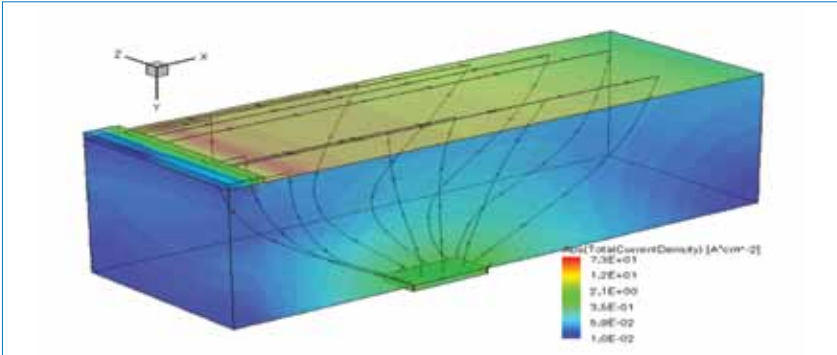


Figure 13. Streamtrace plot showing the current flow between front and rear contacts. The cell dimension (L×H×W) is 500μm×150μm×350μm. In this simulation the rear contact size is 70μm×70μm, and is 130μm away from the edge of the top contact. The substrate doping is 2.0×10¹⁶cm⁻³.

Image courtesy of V. Moroz, Synopsys.

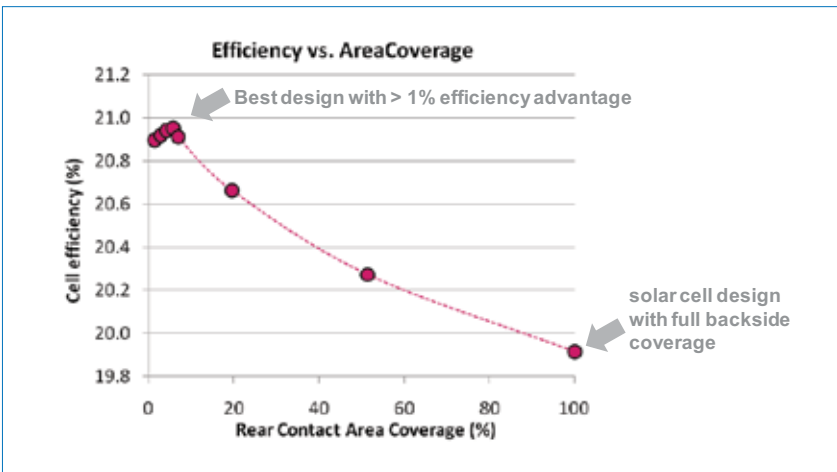


Figure 14. Simulated efficiency as a function of rear-contact area coverage. The cell with local contacts covering 5% of the back surface is 1% larger in efficiency than a cell with an unpatterned back side (100% coverage).

Figure courtesy of V. Moroz, Synopsys.

velocities for carriers at the back contacts and surrounding nitride passivation, and the effects of current crowding and contact resistance at the back contacts.

The simulated total current distribution arising from these conditions is shown in Fig. 13. Current flows three-dimensionally towards the back contact. To assess the impact of the back-contact area coverage, this is varied in a series of simulations from 100% down to about 1%. Fig. 14 shows the efficiency as a function of rear-contact

area coverage. The efficiency peaks at 5% coverage, reflecting trade-offs between several physical mechanisms. The resulting power conversion efficiency is a full 1% higher than for the conventional cell with 100% coverage.

Simulation of emitter wrap-through based architectures

This section looks briefly at TCAD simulation for cell architectures currently

being developed for production at a number of cell manufacturers. We outline applications to EMT and MWT cell architectures – these being current examples where TCAD can strongly accelerate introduction and optimization of higher efficiency solar cells from research and development to production.

A first discussion of EWT cell operation supported by 3D TCAD analysis has given insight into via resistance effects in the EWT cell [10]. Here we illustrate the application of 3D TCAD to evaluate trends in cell efficiency as functions of cell geometry and via processing (EWT versus MWT) [6].

A simplified EWT unit cell structure surrounding a single wrap-through cylindrical via of radius r is shown in Fig. 15. The simulation geometry represents one quarter of the repeating structure in a wrap-through cell, taking advantage of reflection symmetry about the x- and y-axes passing through the rows of vias. In the figure, only the silicon part of the cell is shown, viewed at an angle allowing the back-side diffusions to be shown. The emitter doping is shown in red and the base doping in blue.

This region is simulated using ~10⁶ finite elements, leading to random-access memory requirements for efficient simulation of ~10¹⁰ byte. Typical cpu times on a PC-based processor cluster with sufficient available memory are a few times 10⁵ seconds for a single I-V characteristic. Figs. 16 and 17 show the simulated hole current density and electron current density in the cell under AM1.5 front-side illumination. The current flow in the top-side emitter region is approximately radial (electrons flowing towards the via) while in the back-side region, holes flow towards the base contact and electrons flow towards the back-side emitter contact. In the region around the via, current flow is fully three-dimensional, with electrons flowing from the front-side emitter to the back side and more complex flows of electrons and holes in the via surroundings. Efficiency

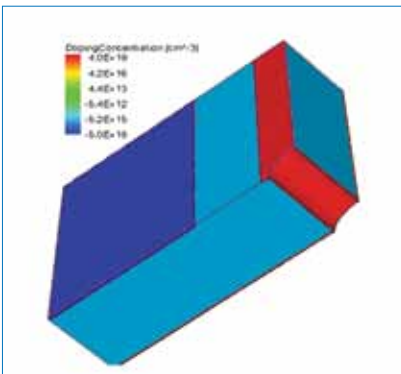


Figure 15. Quarter unit-cell of the EWT structure, inverted to show the back-side contacts.

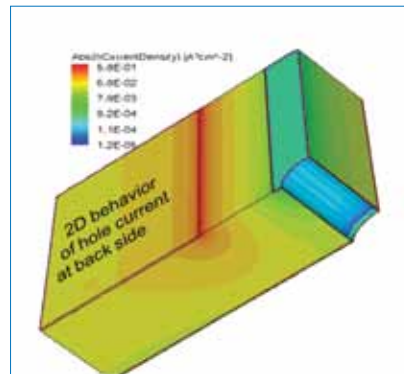


Figure 16. Simulated hole current density in the cell.

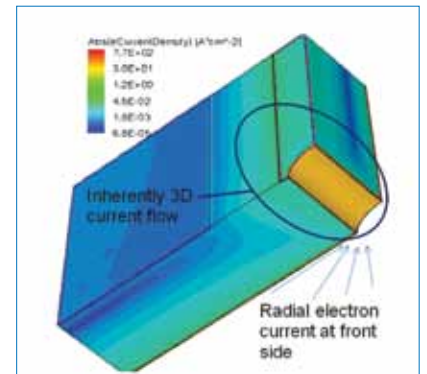


Figure 17. Simulated electron current density in the cell.

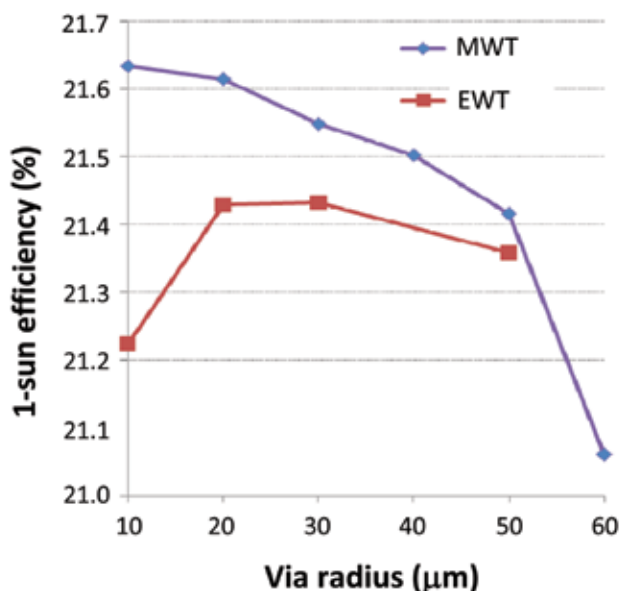


Figure 18. Efficiency versus via radius for the EWT and MWT. The EWT efficiency peaks at $r \sim 20\mu\text{m}$ due to a trade-off between shadowing and via resistance. The MWT efficiency (assuming perfectly conductive metal fill) continues to increase towards smaller via radii.

can be significantly limited by the rate of flow of electrons along the via to the back contact.

Efficiency as function of cell geometry and via technology

Fig. 18 shows the dependence of efficiency on via radius for (a) emitter wrap-through technology where electron current along the via passes through the surrounding emitter doping, and (b) metal wrap-through technology where current flows through the metal fill. In the metal wrap-through case we have assumed that the metal acts as a perfectly conducting contact with no break in continuity. In the emitter wrap-through case (without metal fill), efficiency peaks at an intermediate via radius, found here to be $\sim 20\mu\text{m}$, while in the metal wrap-through case, efficiency rises towards smaller via radii. The optimal radius is determined by a trade-off between via resistance and optical shadowing, and depends on the emitter doping characteristics.

Optical generation in textured thin films

This section takes a brief look at recent developments in simulation of light trapping and absorption in textured solar cell structures. The finite-difference time-domain (FDTD) method implemented in the Sentaurus Device has been used, together with imported atomic-force microscopy (AFM) data (Fig. 19) to simulate optical effects in glass/TCO/a-Si stacks – a key component of a-Si-based thin-film cells [11].

The simulated carrier generation rate in the a-Si film, deposited on textured TCO/glass, is shown in Fig. 20. Significant variations arise from interference and reflections at the rough topography. The absorption rate averaged over the simulation volume is substantially higher than for a planar structure. Such work will soon be combined with electronic simulations, as described in earlier sections of this paper, to enable highly realistic predictions of cell performance.

Summary and conclusions

TCAD is an essential component of semiconductor research, development and manufacturing. It is pervasive in the IC industry and large-area electronics and is now penetrating the PV industry via research institutes and start-up companies. This paper has reviewed how TCAD, using physically accurate process and/or device simulation, can be applied to a range of wafer-based and, increasingly, thin-film solar cell technologies. Simulations of an established LGBC process show good

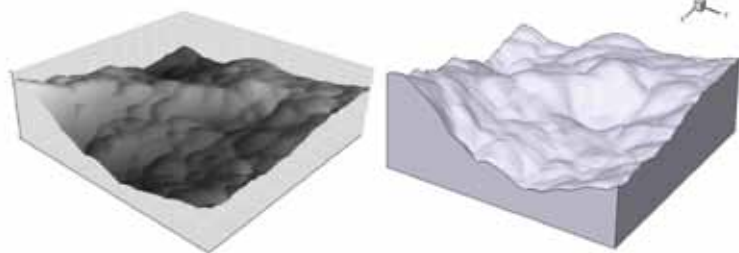


Figure 19. Transfer of TCO ($\text{SnO}_2\text{:F}$) topography measured by AFM (left) to simulation software (right).

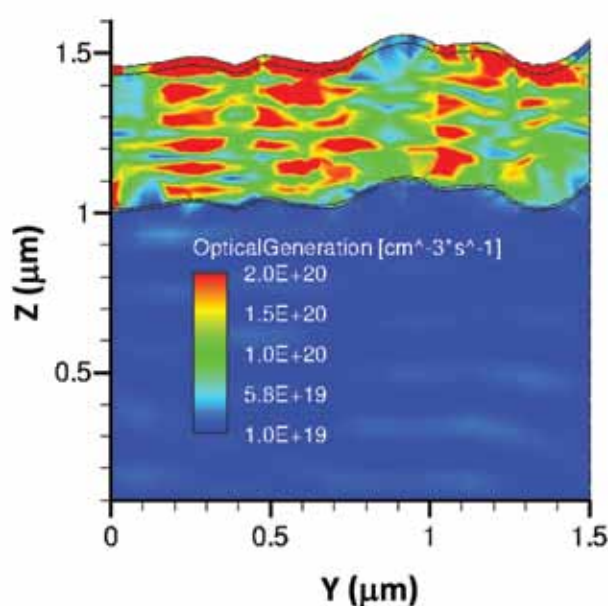


Figure 20. Optical generation rate in the a-Si:H absorber layer for $\lambda = 640\text{nm}$ and perpendicular incidence. The lower part of the figure is the TCO layer, which has been deposited on glass (not shown).

Images courtesy of J. Lacombe, Next Energy.

Figure courtesy of J. Lacombe, Next Energy.

agreement with observed efficiency trends as functions of processing conditions, and further potential improvements have been identified. 3D device simulations have been presented for cells with back-side passivation and for wrap-through cells with and without metal vias. Finally, we have reviewed some recent results on optical absorption in thin-film cell structures.

While experimentation is always required, TCAD can efficiently substitute for the very extensive in-line experiments and cell characterization studies needed to obtain equivalent insights without simulation. This approach will support faster development of advanced PV technologies from the imagination of inventors, through the laboratory scale into pilot and full production. Integrated TCAD – validated by process experiments – will become a critical component of future efficiency improvement roadmaps in the PV industry.

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References

- [1] FP6 ATOMICS Project Final Public Report [available online at http://www.iisb.fraunhofer.de/en/arb_geb/atomics/PublicFinalReport2.pdf].
- [2] International Technology Roadmap for Semiconductors [available online

at http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009_Modeling.pdf].

- [3] Synopsys TCAD pages [available online at <http://www.synopsys.com/Tools/TCAD/Pages/default.aspx>].
- [4] Basore, P.A. & Clugston D.A. 1997, “32-bit solar cell modeling on personal computers”, *Proc. 26th IEEE PVSC*, Anaheim, California, USA.
- [5] Altermatt, P.P. et al. 2009, “Highly predictive modelling of entire Si solar cells for industrial applications”, *Proc. 24th EU PVSEC*, Hamburg, Germany.
- [6] Ahn, C. et al. 2010, “Integrated process and device TCAD for enhancement of c-Si solar cell efficiency”, *Proc. 25th EU PVSEC*, Valencia, Spain.
- [7] Löfgen, P. et al. 1994, “Boron doping of silicon using coalloying with aluminum”, *Appl. Phys. Lett.*, Vol. 65, p. 2792.
- [8] Gee, J.M. et al. 1999, “Boron-doped back-surface fields using an aluminum alloy process”, Sandia Nat. Lab. Report SAND99-0591C.
- [9] Huang, J. & Moroz, V. 2010, “Mono-crystalline silicon solar cell optimization and modeling”, *Electrochem. Soc. Proceedings*, Vol. 33, p. 33.
- [10] Ulzhofer, C. et al. 2009, “VIRE effect: Via-resistance induced recombination enhancement – the origin of reduced fill factors of emitter wrap through solar cells”, *Proc. 24th EU PVSEC*, Hamburg, Germany.
- [11] Lacombe, J. et al. 2010, “Optical

modeling of light trapping in thin film silicon solar cells using the FDTD method”, *Proc. 35th IEEE PVSC*, Hawaii, USA, pp. 1535–1539.

About the Authors



Nick Cowern is a physicist and works as a professor at Newcastle University, UK, where he currently heads the nanomaterials and electronics research group.

His research interests involve experiments and theory of defects and diffusion in electronic materials and TCAD for nanoelectronic devices and photovoltaics. He previously held a principal scientist position at Philips Research Laboratories, Eindhoven, The Netherlands.



Chihak Ahn is a physicist and electrical engineer. He received his Ph.D. from the University of Washington, USA, and took a postdoctoral position at

Newcastle University, UK, specializing in multiscale modelling of defects and diffusion in silicon-based materials, and TCAD for nanoelectronic devices and photovoltaics. He has just joined Samsung Information Systems America.

Enquiries

School of Electrical, Electronic and Computer Engineering, University of Newcastle-upon-Tyne, NE1 2EQ, UK
Tel: +44 (0) 191 222 5636
Email: nick.cowern@ncl.ac.uk
Website: www.ncl.ac.uk/eece