The opportunity for wafer-based reduction in LCOE

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Abstract

As the PV industry strives to reach terawatt scale, addressing the last remaining cost centres of the crystalline silicon value chain will play a critical role in ensuring that the industry can continue to achieve lower systems costs, and provide the extremely low levelized cost of electricity (LCOE) required to drive the adoption of this form of energy. Wafer manufacturing remains the single largest cost driver in industrial cell production. While incremental improvements, such as diamond wire (DW) sawing, have helped to lower silicon consumption, wafer manufacturing has lacked the significant step change necessary for achieving dramatic cost reduction. Creating silicon wafers directly from the melt, without sawing, has long been recognized as a potential breakthrough technology for PV, as it would: 1) allow more effective silicon utilization; 2) eliminate ingot cropping, squaring and blocking and associated consumables costs; and 3) eliminate the most wasteful, high-cost step in wafer manufacturing – the sawing. This paper discusses Direct Wafer® technology, which achieves the long-sought cost and performance advantages compared with current ingot-based production methods; also discussed are the current technical achievements of this wafering process as it moves into commercialization. Wafers produced directly from the melt have been shown to deliver equal or better solar cell efficiency and module stability. Moreover, the ability to operate at the melt level provides significant opportunity for additional R&D achievements, opening a clear path for future industrial importance.

Background

The concept of manufacturing wafers without kerf – the sawdust-like by-product of slicing ingots – is not new. For decades the solar industry has consistently sought ways to eliminate waste and strip cost from the conventional process. Numerous early attempts were made to work at the melt level, but the resulting technical achievements could not compete with the incumbent approaches. While the traditional methods continued to make incremental improvements, the knowledge gained from the earlier work towards kerfless wafer manufacture provided the foundation for what has since emerged: a disruptive wafer production process that pulls silicon wafers directly from a molten bath, simultaneously achieving low cost, high throughput and superior performance.

Fundamentally, the *Direct Wafer process* is a furnace invention, a machine that allows a standard-sized wafer to be created in a single step. At an industry level, this method represents the first major advancement in furnace technology in nearly 50 years, the last being the development of the directional solidification (D-S) system in the early 1970s. That has since gone on to become the standard for multicrystalline ingot casting, while the Czochralski growth method, developed in 1916 and adopted for silicon by Bell Labs in the 1950s, has remained the dominant process for monocrystalline ingot pulling [1]. Both ingot casting and ingot pulling incur manufacturing costs associated with multiple steps, beginning with polysilicon purification and crystallization, then bricking, grinding and chamfering, and finally cropping, wire sawing and cleaning of the wafers. From a production-cost perspective, silicon usage, crystallization and wire slicing represent the three dominant parts of the traditional wafer-processing chain.

Polysilicon to wafer approaches

For half a century there have been two approaches to converting polysilicon into wafers. While these technologies have adequately met the needs of the PV industry, they endure as significant cost centres, limited by an inability to dramatically reduce the amount of input material required during fabrication.

Today the majority of silicon wafers for solar cells are produced by the directional solidification technique, also known as *ingot casting*. The standard process for the production of multicrystalline silicon consists of multiple steps:

- Heating up
- Melting of feedstock
- Crystallization phase and cooldown with reduced pressure
- Argon purging

The resulting ingots, with a total mass of 950kg, typically yield 36 bricks from a 6 × 6 sawing template. Typical crystal growth rates are in the range 10–15mm/h. The total cycle time – depending on the crucible size/loaded mass, the crystal growth velocity and the general furnace layout – is in the range 65 to 70 hours for current Gen6 furnace technology.

The silicon waste associated with the multicrystalline approach is significant, as opportunities for recycling are limited because of the high levels of impurities – such as iron, nickel, copper and carbon – at the top of the ingot, a result of the segregation coefficient (segregation coefficient = the difference in solubility of impurity atoms in liquid from that in solid). This top layer must be removed and scrapped, and the remaining ingot must still contend with impurities

from the crucible and coating which have diffused into the cast material and lead to poor quality at the bottom and sides of the ingot (the 'red zone').

It is possible for ingot casting to produce higher-quality mc-Si material (called *high-performance (HP) mc-Si* or *high-efficiency (HE) mc-Si*) through the 'half melt approach' [2–4]. This process maintains a temperature below 1,400°C at the bottom of the crucible to keep the lower portion of the Si feedstock from melting. This unmelted Si acts as a seed to initiate a multicrystalline grain structure with homogeneously distributed small grains. While this process has led to the production of mc-Si ingots with fewer dislocations, resulting in a higher-quality material, the process time is lengthened and the overall yield is reduced, given that the seed region cannot be used for cell production.

The monocrystalline silicon wafer material for the PV market is currently produced by the Czochralski technique (also called *Cz pulling*), which also consists of several steps [5,6]:

- Heating up
- Melting of feedstock and melt stabilization
- Dipping of the seed crystal and necking process
- Initial crystal growth to the desired diameter ('shoulder growth')
- Crystallization of the ingot with constant diameter ('body')
- Growth of the end cone before the crystal is pulled and the furnace is cooled down

Standard Cz pullers for silicon PV wafer production utilize crucibles of up to 22" in diameter, with up to 210kg of Si mass and a crystal length of up to 2.8m. It has been reported recently, however, that machine developments (especially in China) will lead to larger machines which use crucibles of 28" or 30" in diameter. These furnaces would have additional feeding systems to add Si feedstock into the melting process, yielding crystal masses of 325kg and crystal lengths of up to 4.0m. It is expected that these crystal pullers will also have the configuration for multi-pulling or continuous Cz (to potentially increase crystal growth throughput).

Ingot processing

The processing of ingots into wafers is shown in Fig. 1, together with a complete loss-and-recycle analysis throughout the wafer production chain. The bricking of D-S ingots currently uses a diamond wire (DW) cutting machine with a water-based fluid in a grid-like configuration. Each of the parallel cutting lines is as long as the side length of the final wafer, and the ingot, including its side slabs, is cut in one process. While the side slabs can be recycled, sawing itself accounts for approximately 6kg of kerf loss.

The raw-side faces of the newly sawn bricks reach final size and surface quality during a two-step process involving grinding and polishing; this results in an additional kerf loss of approximately 20kg. The inclusion-rich top and bottom sections of the bricks are cropped using a band saw or an inner diameter (ID) saw, and the top section (42kg) is discarded because of metal contaminants and materials with low segregation coefficients, carbide or carbon particles. The bottom section is recycled and used for the next growth run. The bricks are then ready for wafering (wire slicing).

Today, the preferred technique for wafering is the DW cutting technique. In contrast to the former slurry technique, the abrasive particles are diamond fragments which are bonded to the steel core wire, either by resin gluing or by electroplating.

The cost of diamond wire is a magnitude higher than that of standard wire, and the higher-speed cutting process operates so as to make the most use of the wire by regularly reversing the wire movement direction ('pilgrim mode'). The fluid used during the process to cool the cutting channels and to transport the cut material (kerf) is water based with additives. Whereas the DW

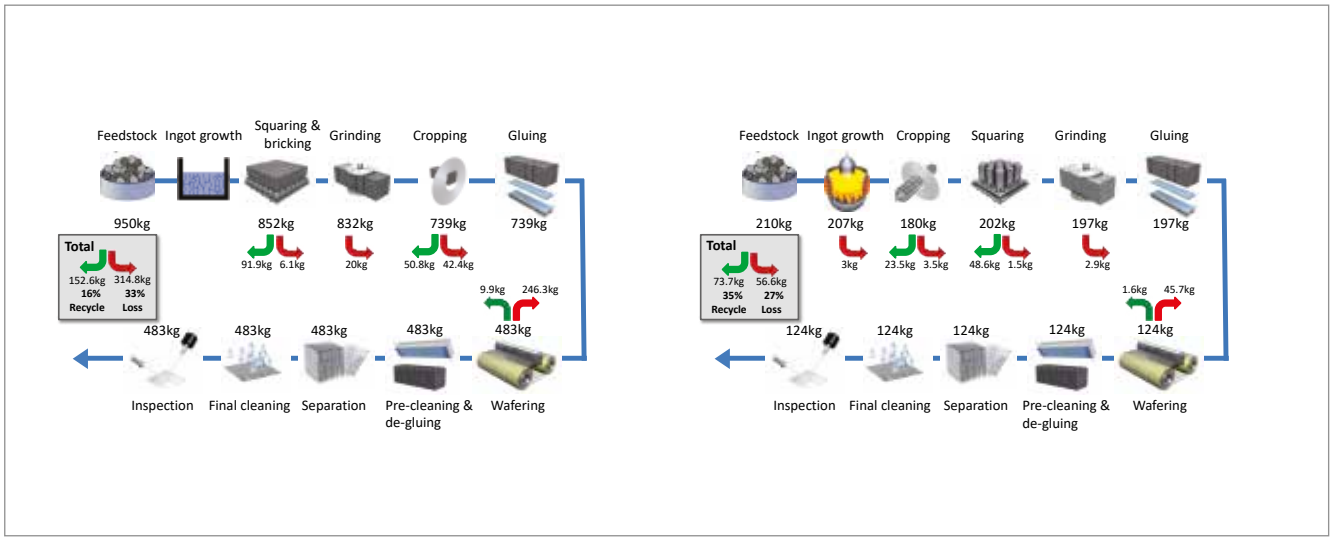

Figure 1. Silicon loss-and-recycle analysis throughout the D-S HP mc-Si (left) and Cz-Si (right) wafer process chains.

technique has been the predominant method for the cutting of monocrystalline silicon for many years, the major shift to DW cutting for multicrystalline silicon only began in 2017, but it has already become the main technique in 2018.

The final step, wafer cleaning, requires two processes. In the first of these, the cut wafers – still glued to the glass carrier beam – are cleansed to remove the cooling fluid. They are then de-glued in a mild acid bath, demounted from the carrier beam, machine separated and fed into the final cleaning system, which consists of spraying and rinsing in a hot ultrasonic or megasonic bath to wash the wafer surfaces. As a last step, the wafers are dried and transported to another area for a final quality check, sorting and packaging.

Direct Wafer approach

The Direct Wafer process, developed by 1366 Technologies, to make 156mm wafers [7] directly from a silicon melt eliminates the high-cost ingot-production steps described earlier. The key enabler of the Direct Wafer technology is a method for freezing a thin sheet of silicon on the surface of the melt, removing the sheet from the molten bath, and subsequently extracting the free-standing sheet. Within the same equipment, the sheet is then trimmed with a laser to form the final wafer geometry, and the clean trimmings are collected to be reused. The process, which uses heat removal perpendicular to the plane of the wafer, enables a high production rate of low-stress silicon within an extremely pure growth environment.

> "The Direct Wafer process to make 156mm wafers directly from a silicon melt eliminates the high-cost ingot-production steps."

The Direct Wafer platform was designed to produce industry-standard wafer geometry, to leverage cell and module manufacturers' existing investments, and to deliver a product that both drops into the current infrastructure and could benefit from the industry's collective performance and cost improvements.

In early 2009, 1366 first explored a proof of concept and several embodiments of the Direct Wafer method using molten tin as a model material at hot plate temperatures for rapid design iterations. Once a baseline was achieved with tin, a small-scale prototype silicon wafer furnace was built by the 1366 team. The initial wafers were transformed into small solar cells, measuring 2cm × 2cm, with an efficiency of 10%. In 2011 the first full-scale furnace was built to produce industry-standard-size 156mm wafers.

Table 1. Resulting net silicon utilization from a recycle-and-loss analysis for all considered manufacturing methods.

Manufacturing method	Net silicon utilization per wafer [g/wafer]
Cz-Si reference process at 10GWp (160µm)	15.65
HP mc-Si reference process at 10GWp (180µm)	17.07
Direct Wafer baseline process at 1GWp (180µm)	10.79
Direct Wafer roadmap process at 10GWp (130µm)	7.00

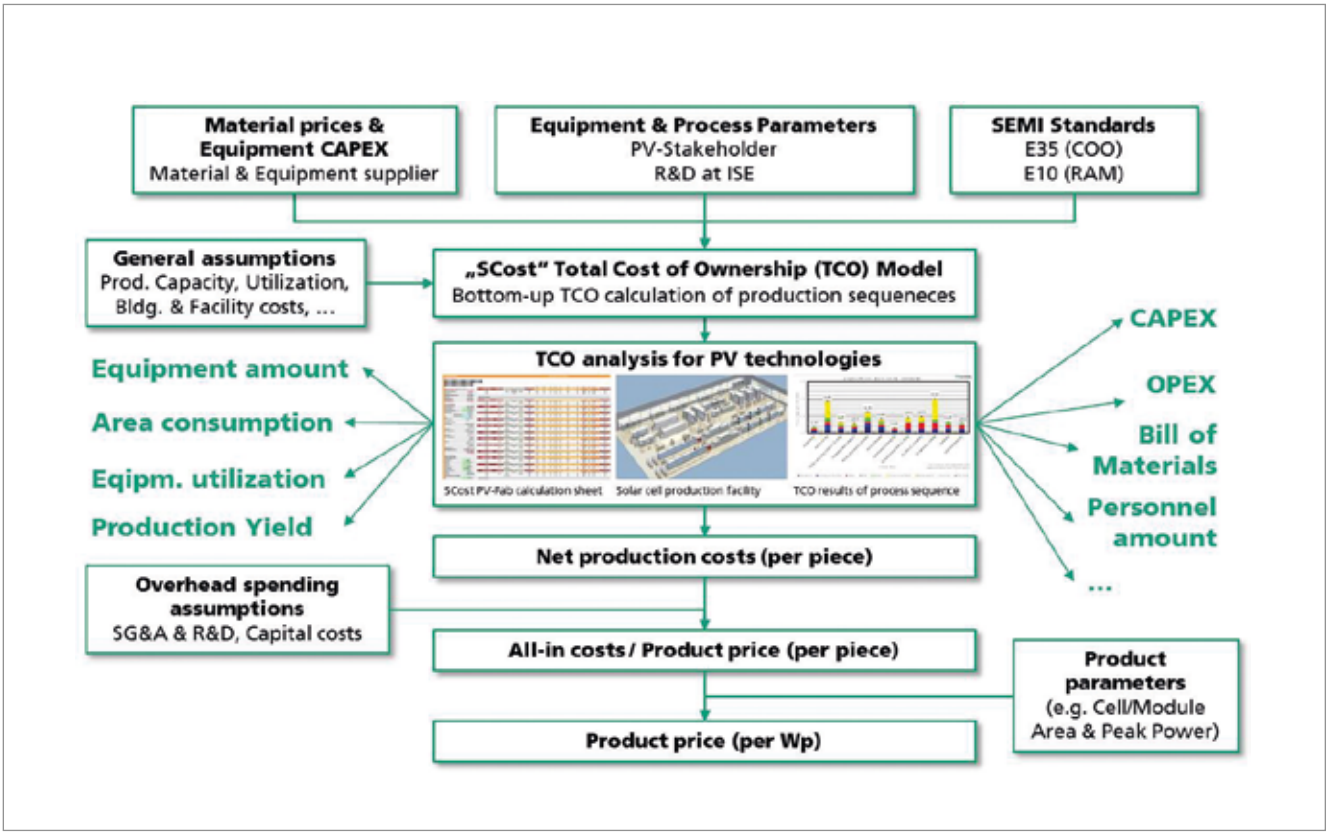

Figure 2. Methodology for the cost calculation using the SCost tool, developed at Fraunhofer ISE.

Having achieved reasonable electrical performance from the cells, 1366 opened a demonstration factory in 2013 to begin building full-scale manufacturing machines and continued to improve the furnace design. Three full-size production Direct Wafer machines currently operate in the demonstration factory, with each of these latest generation tools capable of producing 240 wafers per hour (15 sec cycle time, ~10MW per year). These demonstration machines provide the platform that is being reproduced for the first mass-production facility currently under way.

Total cost of ownership methodology

To provide an informed calculation of the cost-reduction capability of the Direct Wafer process, an economic analysis featuring a bottom-up calculation of the industrial PV value chain was conducted and adapted for individual production technologies. The underlying cost model is aligned with the SEMI standard E35 for the calculation of the cost of ownership (COO) for semiconductor and PV production equipment, as well as the SEMI standard E10 for reliability, availability and maintainability (RAM) [8,9]. The equipment- and process-related input parameters (e.g. process throughput or material consumption), as well as equipment capital expenditure (CAPEX), are gathered from various PV stakeholders, mainly directly from the equipment manufacturers, but also from PV companies using the equipment in actual production. Material input prices are primarily collected directly from the suppliers of the material. With the bottom-up total cost of ownership (TCO) model 'SCost', the process information from the individual process steps is put into complete process sequences, in combination with general production assumptions, such as the envisioned capacity and planned utilization of the production facility (as shown in Fig. 2).

The result of the TCO analysis of the process sequence is the net production costs per manufactured production item. The net production costs include all costs of production, and are divided into categories with the following cost components:

- **Equipment:** Production equipment and automation, including delivery, installation and qualification.
- **Building and facilities:** CAPEX, capital costs and operational expenditure (OPEX) related to fab building and facilities – HVAC, gas farm, DI water production, chemical supply, waste disposal, warehouse, offices, infrastructure personnel, canteen, etc.
- **Utilities:** Power, cooling, CDA, exhaust, DI water, water, N_2, etc.
- **Parts:** Spare parts and wear and tear.
- **Process consumables:** Solids, liquids, gases, etc.
- **Waste disposal:** Materials for fab internal disposal, costs for external disposal.
- **Labour in production:** Operators, technicians, supervisors, engineers, scientists.
- **Cost of yield loss (CYL):** Breakage and pieces not meeting quality requirements.

For capital cost, the weighted average cost of

Table 2. General model assumptions and calculation parameters.

Parameter	Value	Unit
Production output[a]	10,000	MWp/annum
Factory capacity utilization (320 days/annum, 24 hours/day)	7,680	hours/annum (87.7%)
Shift-dependent staff deployment to the production line[b]	4.0	FTE/position
Building[c] and facility[d] CAPEX: ingot and wafer production (building/facility)	200/950	$/m^2
Depreciation period (equipment/facility/building)	10/10/20	years
Silicon price	14.67	$/kg
Electricity price	6	¢/kWh
Capital costs (WACC after tax) for all stages	5.00	%
Equity/debt share	20/80	%
Cost of equity/debt (pre-tax)	10/5	%
Average tax rate	25	%

[a] Output with respect to assumed capacity utilization (higher utilization → higher output).
[b] Average number of employees per position to cover the total labour needs (including vacation and illness) with respect to the factory's capacity utilization (FTE = 'full-time equivalent').
[c] CAPEX calculated on total building area. Includes all costs for land, site preparation and building.
[d] CAPEX calculated on gross manufacturing area. Includes all required production facilities, such as HVAC, gas farm, DI water, chemical supply, waste disposal → facilities are ready for equipment hook-up.

capital (WACC) approach is used, including debt payments but also an assumed equity return for the company. Capital costs are calculated on the average employed capital of the company, including the fixed capital for production equipment, building and facilities, as well as for tied-up inventory capital in incoming and outgoing products, parts and process consumables and waste materials. Not included in the net production costs are overhead costs for selling, general and administrative (SG&A) expenses and for R&D, as well as capital costs associated with the corporate unit. For SG&A and R&D, market benchmark values are taken (as the share of revenues from annual reports from PV manufacturers); these are included in the 'all-in costs' component.

Finally, the main product-quality parameter included is the conversion efficiency of the cell or module; this is calculated from the peak power output (the power output under standard testing conditions – STC) and the area of the device.

The SCost methodology for the techno-economic assessment of PV technologies along the PV value chain is described in more detail in Nold et al. [10].

Table 2 gives an overview of the general model assumptions and the calculation parameters used in the TCO analysis.

Fig. 3 presents the results of the economic assessment of ingot and wafer production for a monocrystalline (Cz-Si) wafer and a high-performance multicrystalline wafer (HP mc-Si), as well as for the Direct Wafer baseline and roadmap approaches. Given today's capacities, the calculations were conducted on the basis of an annual output of 10GWp, with the exception of the Direct Wafer baseline, which assumed an annual output of 1GWp only, to represent initial scaling of the existing platform.

The poly-Si input material alone accounts for approximately half of the net wafer production cost for both of the reference technologies. Less poly-Si material is consumed for the Cz-Si wafer production, given that its internal silicon recycling rate is higher than that of mc-Si wafer production, and that more-aggressive thickness reduction is under way for Cz-Si wafers (also reflected by the lower net silicon utilization per wafer shown

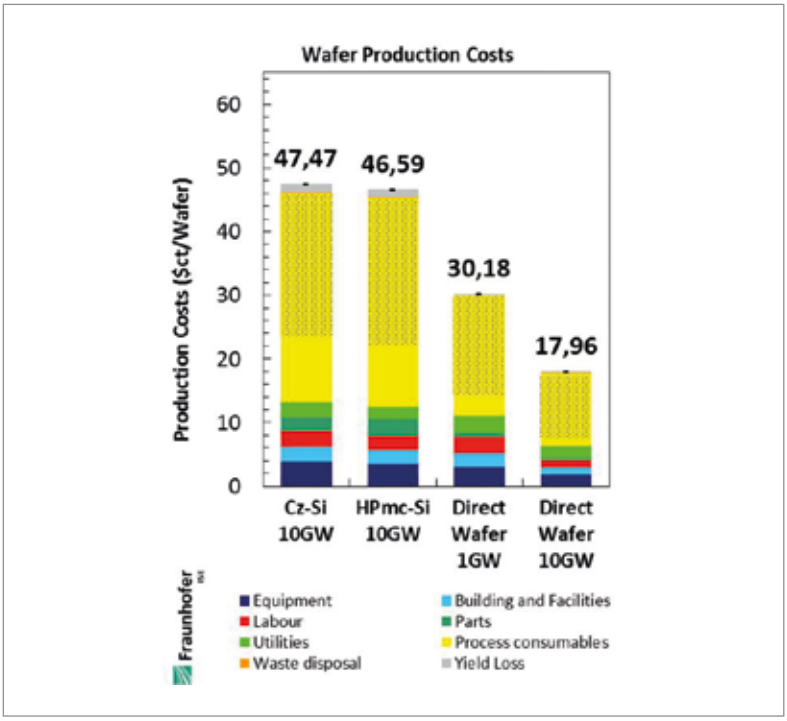

Figure 3. Results of the economic assessment of ingot and wafer production for Cz-Si and HP mc-Si wafers, and of the innovative Direct Wafer approaches (the poly-Si share of process consumables is indicated by the shaded area).

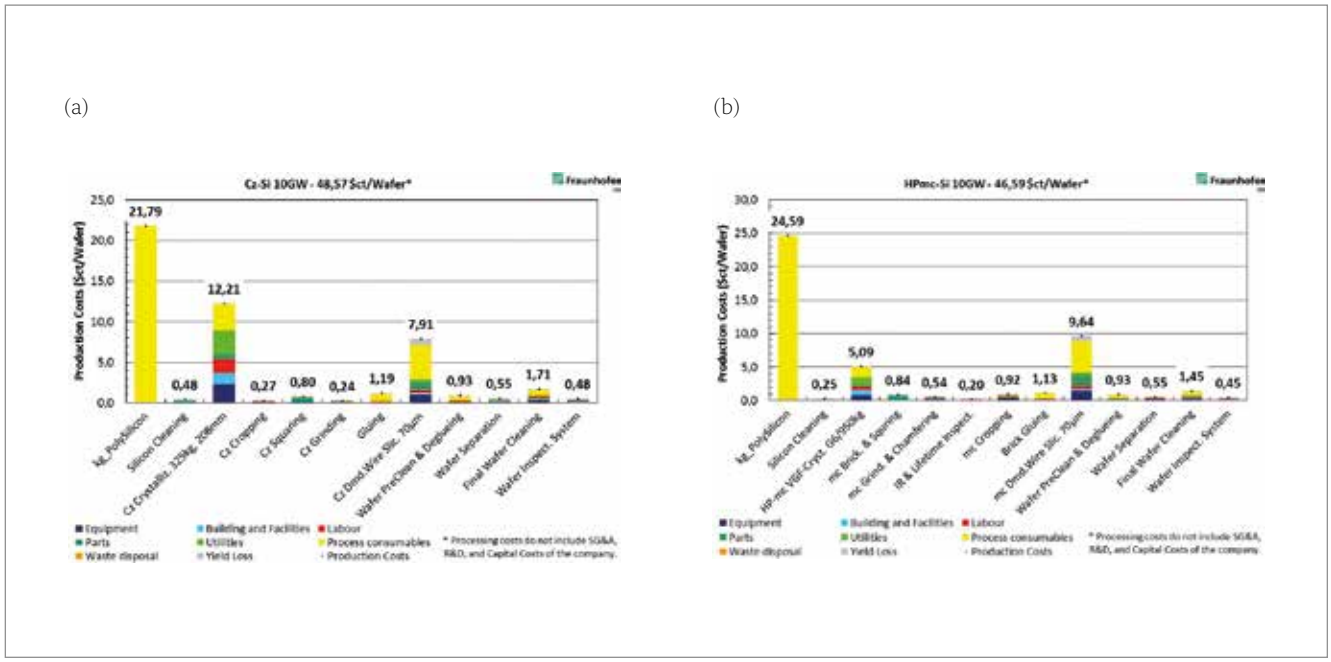

Figure 4. Cz-Si (a) and HP mc-Si (b) wafer net production costs (stepwise from left to right) for an ingot and wafer production with an annual output of 10GWp.

"The significant progress represented by the Direct Wafer process is particularly compelling with respect to the impact on the levelized cost of electricity (LCOE)."

in Table 1). Even though the crystallization equipment throughput for Cz-Si has increased, the equipment output for Cz-Si is still lower than for mc-Si. Thus, for the production of a Cz-Si wafer of the same size as an mc-Si wafer by D-S, more crystallization tools are required, resulting in higher Cz-Si ingot crystallization costs of 10.18¢/wafer, compared with 5.09¢/wafer for the HP mc-Si ingot (see Fig. 4). The slicing of mc-Si wafers is more expensive than for Cz-Si because cutting speeds must be decreased in order to cut through multiple different grain orientations.

Fig. 6 shows a comparison of the cost-assessment results with current wafer market prices according to the market analyst PVinsights. The red boxes indicate low, average and high wafer spot market prices in April 2018. As the Cz-Si wafers allow higher solar cell and module efficiencies than HP mc-Si wafers, higher wafer prices are achievable in the market, independently of the production costs.

Levelized cost of electricity

The significant progress represented by the Direct Wafer process is particularly compelling with respect to the impact on the levelized cost of electricity (LCOE). An analysis was performed (Fig. 7) using a combination of:

- the annual 10GWp all-in wafer costs established in this paper;
- the current PVinsights pricing to determine the cell and module conversion estimates for passivated emitter rear cells (PERCs) of 46¢/wafer and 60¢/wafer respectively for ingot-based manufacturing processes;
- the balance of system (BOS) data established by 'Bridge to India' [11].

The higher-efficiency mono (+1.6%$_{abs.}$ Ncell; –3%$_{rel.}$ cell to module) enables a system cost advantage of 3¢/Wp compared with HP mc-Si because of the near parity of wafer cost. This advantage is outweighed by the dramatic wafer cost reduction provided by innovation using Direct Wafer technology.

Quality and efficiency

The electrical quality and the subsequent efficiency potential of silicon wafers are determined by interactions between grain

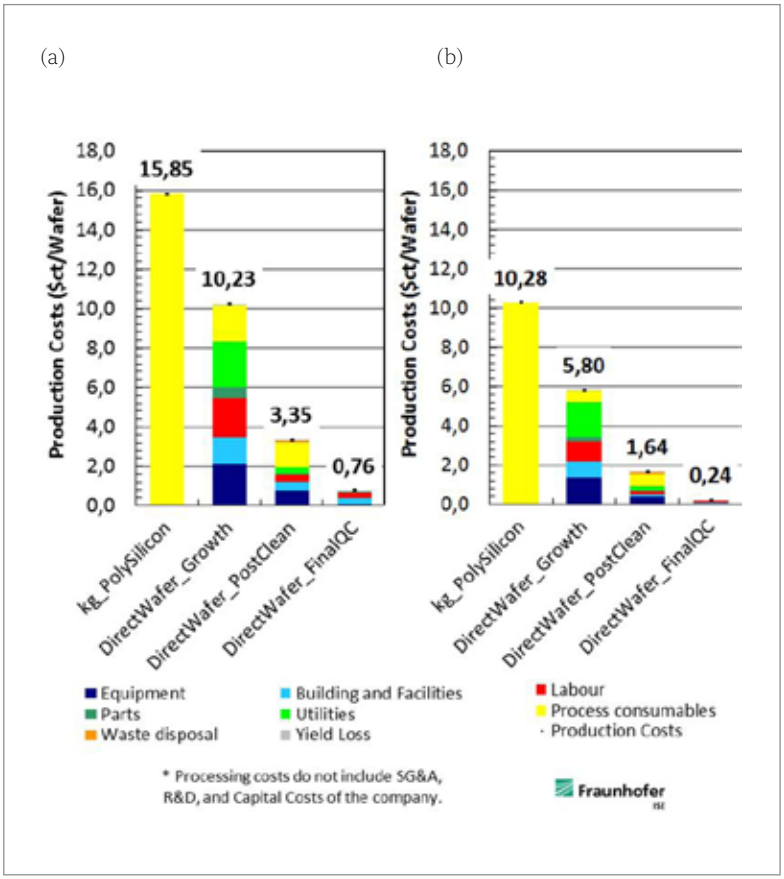

Figure 5. Direct Wafer net production costs (stepwise from left to right) for production with an annual output of (a) 1GWp (baseline), and (b) 10GWp (roadmap).

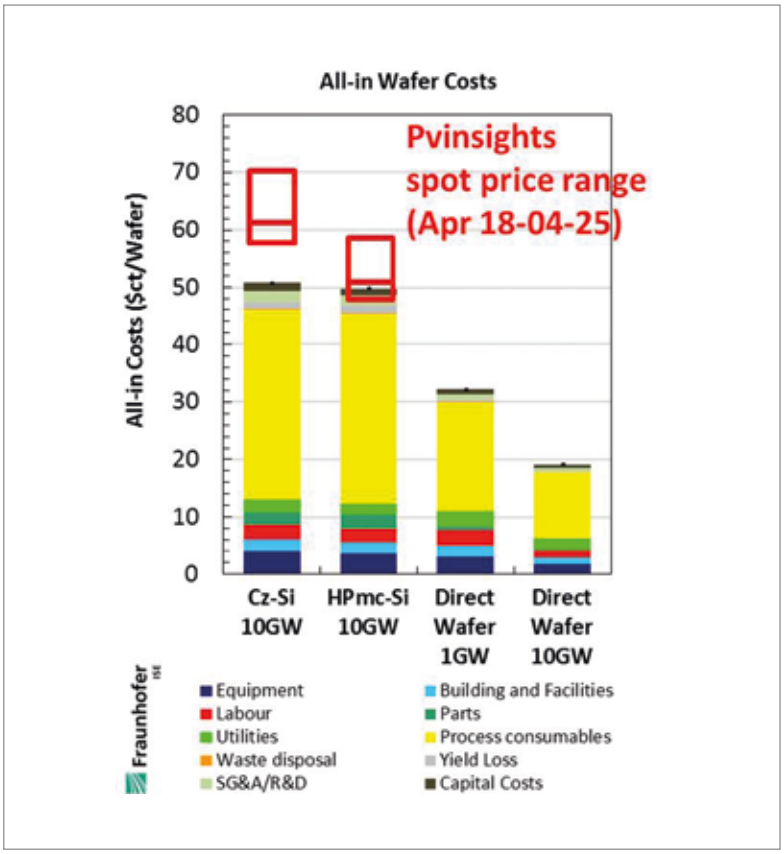

Figure 6. Comparison of the cost assessment results with current wafer market prices according to the market analyst PVinsights. The red boxes indicate low, average and high wafer spot market prices in April 2018 (DW-cut mono and mc-Si wafers outside of China).

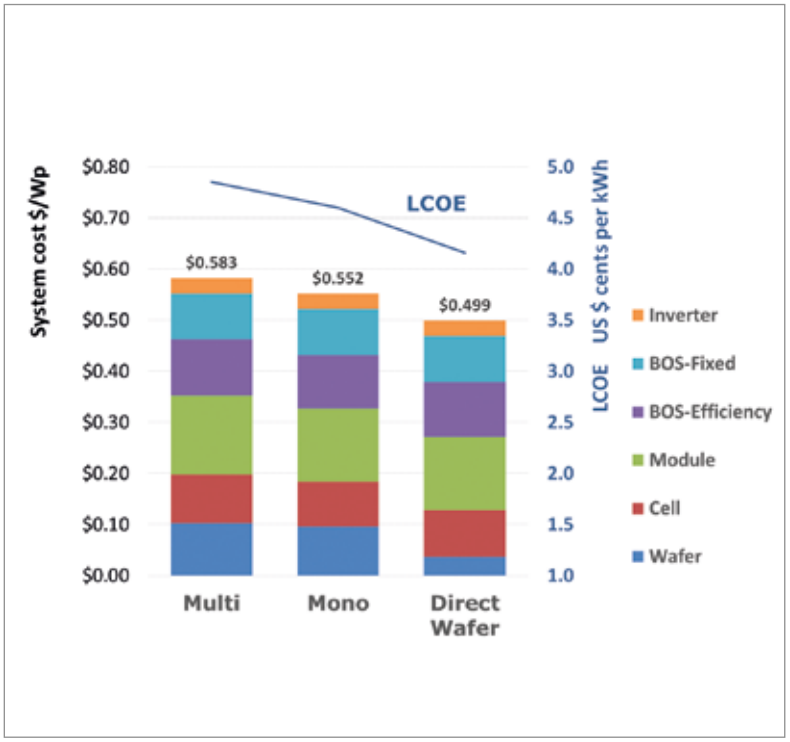

Figure 7. Comparison of LCOE assessment results using the all-in wafer costs established in this paper, PVinsights pricing and 'Bridge to India' BOS data.

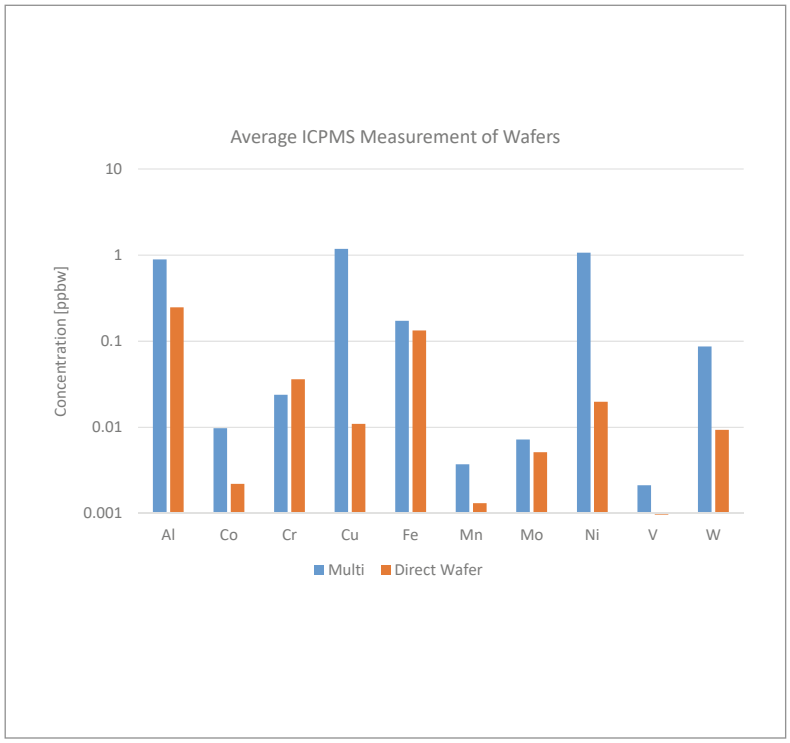

Figure 8. Comparison of impurity concentrations of wafers produced by mc-Si and Direct Wafer processing. Wacker Chemie AG provided hyperpure polysilicon as raw material, analytical services and technical consulting in the framework of its partnership with 1366 Technologies.

"Wafers formed directly from the melt have been shown to deliver solar cell performance the same as (or better than) that of ingot-based wafers in customer trials."

structure, dislocations and impurities. Contrary to the situation several years ago when the industry was focused on seeding mono D-S ingots, which struggled with dislocations, it has recently been shown that small grains in the D-S of seeded HP mc-Si actually help to lower dislocation density and produce higher-bulk-lifetime wafers. This is also true for the Direct Wafer method, which enables consistent control of the nucleation and growth for every wafer, so that the crystal structure is currently tuned for optimal performance with a uniform grain size between 0.5 and 1.0mm. These grain boundaries are perpendicular to the wafer surface and are well passivated by hydrogen during standard cell processing, which means that they do not play a significant role in bulk recombination of the finished cell. The beneficial effect of horizontal sheet growth, where the removal of heat is normal to the plane of the wafer, eliminates large thermal gradients in the wafer which would give rise to thermal stress and or high-density dislocations.

The interaction between the crucible and the silicon during an ingot's growth is known to be detrimental to performance. This interaction leads to the degradation of electrical properties along the ingot border, a layer referred to as the *red zone*. This layer is too poor in quality to be processed into wafers and must be discarded. Moreover, it is understood that because the ingots are held near their melting point for more than one day, significant in-diffusion from dirty materials occurs, impacting wafer quality, performance and passivation. The Direct Wafer growth process, however, occurs in a higher-purity environment, limits in-diffusion to just a few seconds, and delivers stable efficiency over growth periods exceeding six weeks. This long-term stability is made possible by a mechanism that prevents the build-up of impurities in the melt; this is in contrast to Cz growth, in which impurity build-up in the melt during ingot growth limits the number of ingots or the cumulative volume of silicon grown before impurities degrade performance.

In Fig. 8, inductively coupled plasma mass spectrometry (ICPMS) results demonstrate the various metals and levels detected on the basis of an average of the measurements of ten different wafers of each type. The purity advantages of the Direct Wafer growth environment are clearly visible.

The role of purity directly translates to wafer quality. The uniformity of wafer quality is visible in the module electroluminescence (EL) images in Fig. 9; the high-defect density areas found in standard multi wafers can be seen in contrast to the more uniform Direct Wafer module. A tighter cell efficiency distribution is also achieved in the case of Direct Wafer, demonstrated by a recent cell processing run of 24,000 wafers, which achieved 90% of all cells within three Ncell bins using 0.1%

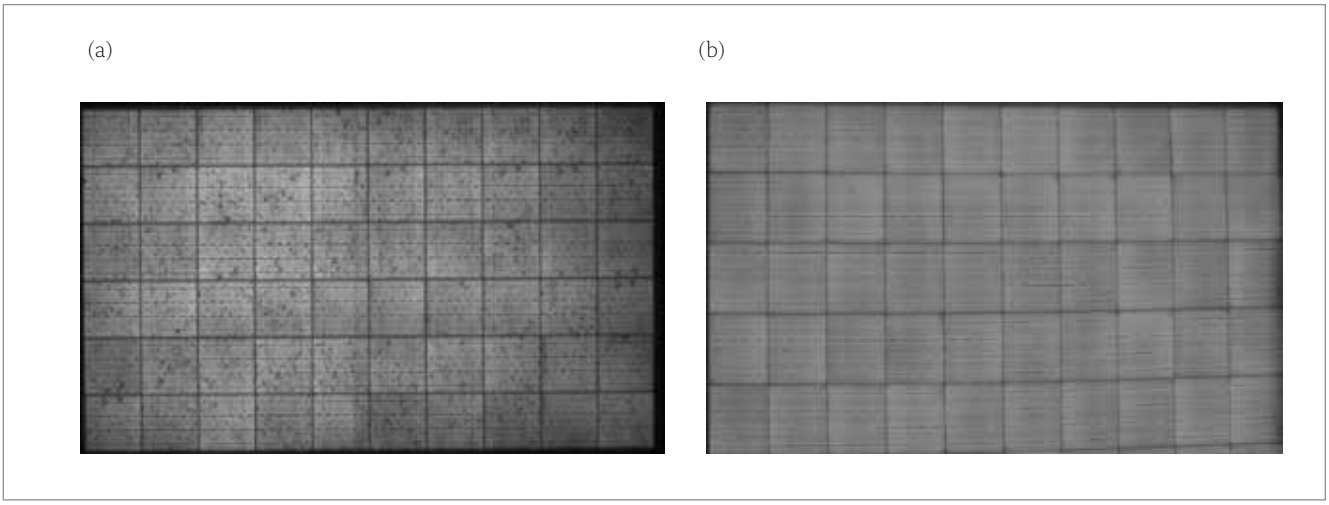

Figure 9. EL images of PV modules made with (a) HP mc-Si wafers, and (b) Direct Wafer products. The impact of dislocation tangles is evident in multi.

steps. The elimination of the low-efficiency tail common in ingot-based manufacturing reduces the sales and inventory challenges that result from the need to discard defective cells or the selling of lower-quality products at a discount.

Wafers formed directly from the melt have been shown to deliver solar cell performance the same as (or better than) that of ingot-based wafers in customer trials. With the demonstrations conducted on standard production equipment, these achievements are rapidly translatable to high-volume, day-to-day production. Direct Wafer products using a PERC cell architecture allow efficiencies well above 20%, and lot averages above 20.5% have recently been demonstrated using Hanwha Q CELLS' Q.ANTUM PERC process. This same combination of technologies has consistently demonstrated gains of more than 0.8% per year (Fig. 10), an improvement rate nearly double that for the average cell efficiencies obtained in mass production [12].

In May 2017 a 500kW commercial installation at Tatsuno Ikariiwa in Hyōgo Prefecture, Japan, was completed. The array features Direct Wafer products in 500kW of modules manufactured at a Tier 1 cell and module manufacturer. The modules' field performance has been compared against a similar array of modules using standard HP mc-Si wafers and a similar module bill of materials (BOM) from the same manufacturer. The array has demonstrated good stability in terms of performance for the first 12 months since installation, with a specific power ratio calculated using the highest-performing sub-array of HP mc-Si modules as references. Comparative monthly performance is summarized in Figure 11.

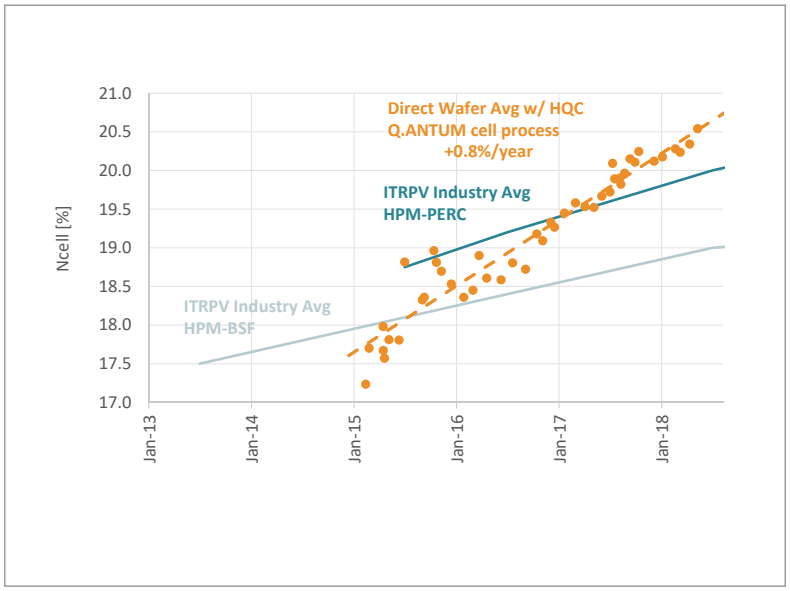

Figure 10. Evolution of the efficiency gains of Direct Wafer products in combination with Hanwha Q CELLS Q.ANTUM PERC process. Gains exceeding 0.8% per year have consistently been demonstrated.

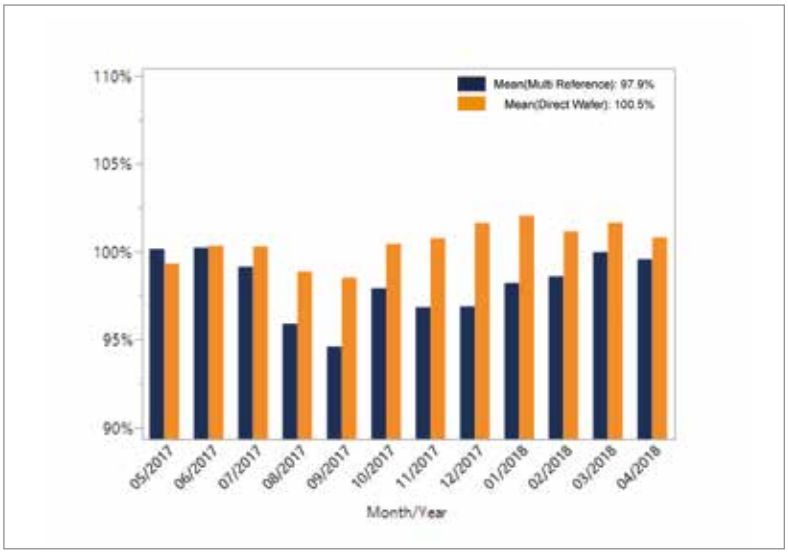

Figure 11. Module performance of Direct Wafer modules at a commercial installation in Japan compared with HP mc-Si reference modules. Data was collected from the installation of more than 1,700 modules of each type.

Direct Wafer technology roadmap

The eventual migration to thinner wafers and the maturity of the Direct Wafer process will undoubtedly bring additional optimization. The technology has the potential to help the wafer industry break free from its commodity standing to one of strategic importance and advantage through

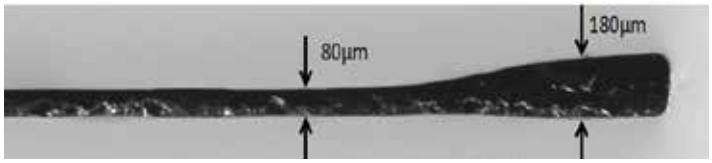

Figure 12. Example of locally controlled wafer thickness.

"Addressing the significant cost centre represented by the wafer is the key to achieving the LCOE reduction for terawatt solar."

the introduction of new wafer features impossible to achieve with conventional manufacturing.

To reduce the amount of silicon used and increase the efficiency achievable by PV wafers, manufacturers have pursued various methods of reducing wafer thickness. While wire sawing can be used to produce wafers thinner than the standard 180µm thickness, these thin wafers have lower mechanical integrity and break during cell fabrication, electrical interconnection and encapsulation in modules. Through the production of 3D wafers, the Direct Wafer process can meet the industry's anticipated need for thinner wafers without compromising wafer strength [13]. This is directly tied to the ability to work at the melt level, which allows local control of wafer thickness; local control can create a thick border where the perimeter of each wafer is of greater thickness than the remainder of the wafer, resulting in a strong, thin wafer that is able to withstand typical manufacturing stresses (Fig. 12). It provides manufacturers with a solution to reducing silicon usage without comprising existing standards or quality, and makes it possible to realize industry advancements in cell architecture or module features. Because the Direct Wafer process avoids the waste associated with sawing, the silicon usage can be less than 1.5g/W, and the crystalline silicon PV supply chain can achieve a wafer cost below 20¢.

The manipulation of dopant concentration has several potential advantages for cell performance, but it is impossible to alter dopant concentration when working with ingot-based silicon wafers. This is not the case when you are able to access the wafer during growth, allowing the introduction of a doping gradient through the wafer thickness. The Direct Wafer process has demonstrated that it is possible to grow wafers with a concentration of dopant six times higher at the wafer back side than at the front. This concentration characteristic has several important advantages [14]: higher voltages are achieved because of the higher concentration of dopant at the rear of the cell, and the higher lateral conductivity between the local contacts of a PERC cell can reduce the series resistance. The gradient in dopant can also provide a field effect, pushing the electrons to the front of the cell, for more efficient collection at the p-n junction. Simulations of the Direct Wafer approach have predicted an increase in cell efficiency of up to +0.7%, and initial tests have already demonstrated +0.3%.

Because of the continuous nature of the Direct Wafer growth method, it is also possible to grow wafers at constant resistivity over time through the use of strongly segregating dopants such as gallium. The process features a short time constant to reach a steady-state concentration in the melt in less than one hour, and is able to grow wafers at a constant bulk resistivity for 1,000 hours without the solute build-up that affects batch ingot processes, as described by the Scheil equation. The production of n-type wafers with a tight distribution of bulk resistivity has been demonstrated.

While the current equipment platform developed for Direct Wafer will support cost advantages over traditional processes, further improvements are already envisioned to increase the throughput of each Direct Wafer furnace; this will be possible without any changes to the physics associated with wafer growth. Equipment design changes can enable the growth of several wafers at a time for additional throughput and CAPEX reduction. An implementation of these design changes will allow 10GW production levels to be realized from a smaller number of furnaces, compared with even the relatively high throughput of next-generation G8 D-S furnaces. Direct Wafer production has a significantly smaller factory footprint because of the fewer steps involved, the inherent simplicity of the process, and the efficient use of materials and energy; it is a platform suitable for scaling to terawatt-level PV.

Conclusion

The concept of a wafer grown directly from molten silicon is not new, but its success had proved elusive. As a result, manufacturers focused instead on streamlining the supply chain to reduce costs, foregoing innovation and relegating the wafer to commodity status. Kerfless wafer technology, specifically the invention of the Direct Wafer process, introduces differentiation to the market, and allows cell and module manufacturers to break free from the constraints that have defined ingot-based manufacturing. Most importantly, operating at the melt level provides significant opportunity for additional R&D achievements, and provides a clear path for future industrial importance. Addressing the significant cost centre represented by the wafer is the key to achieving the LCOE reduction for terawatt solar.

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