

# Photovoltaics

International

THE TECHNOLOGY RESOURCE FOR PV PROFESSIONALS

## Edition 44

### Heterojunction

Helmholtz-Zentrum Berlin leads teams on TCO performance and cost improvements

### PERC

imec covers bifacial solar cell interconnection options

### Industry 4.0

International team makes case for inline metrology in terawatt production era

### Capacity expansion report

In-house analysis of unprecedented 500GW of expansion plans

### Bifacial

Fraunhofer CSP investigates PID in PERC-based bifacial cells

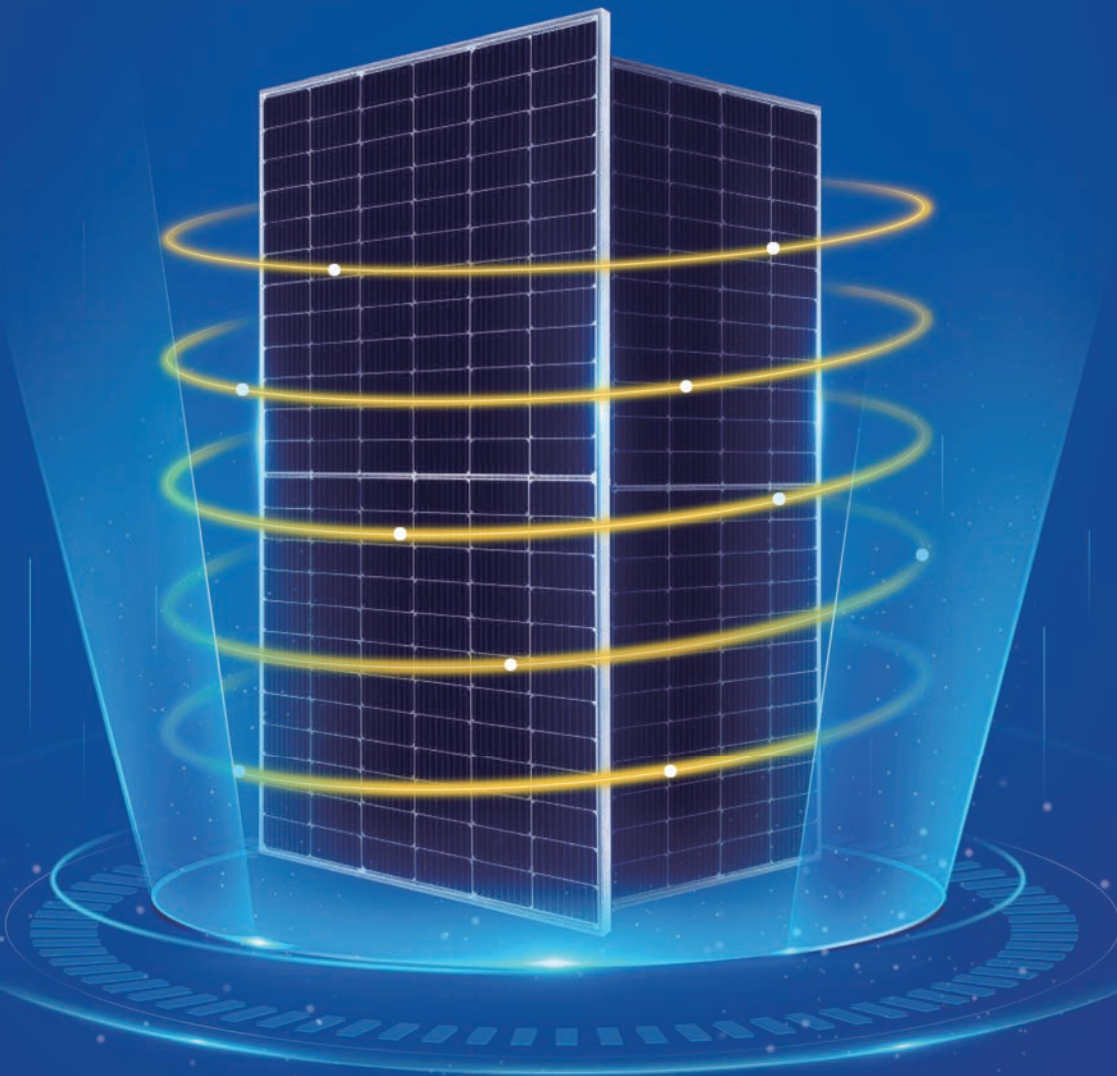
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E info@pv-tech.org  
www.pv-tech.org

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Editor in Chief: **Liam Stoker**  
Technical Publishing Director: **Mark Osborne**  
Commissioning Editor: **Adam Morrison**  
Sub-Editor: **Steve D. Brierley**  
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Cover image: Advanced 5 busbar cell interconnection of PERC cells at SNEC 2019. Photo by Mark Osborne, PV Tech & Photovoltaics International, Solar Media Ltd

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# Foreword

Welcome to Photovoltaics International 44. With the COVID-19 pandemic impacting people's lives around the world, we wanted to start with by thanking all the authors for this edition who contributed amid significant disruptions to their working and private lives during such terrible times. We would also like to extend our understanding of the situation to those who were unable to complete contributions to this edition due to such upheavals and look forward to collaborating again, hopefully soon.

Trying to fathom the impact COVID-19 will have on the PV industry is almost impossible currently. However, what is clear is that technological advancements and innovations continue at an unprecedented pace, whether evolving efficiency gains in mainstream PERC cell technology to next-generation developments with n-type architectures, through to tandem junction and multi-junction alternatives.

This is being supported by an avalanche of new manufacturing capacity expansion announcements that are expected to see large, multiple gigawatts of TOPCon and heterojunction facilities ramp in the next few years with the intention of significantly lowering production costs, while boosting conversion efficiencies.

All these developments are centre stage in this edition.

International Solar Energy Research Center (ISC) Konstanz does a good job of pulling together many of these aspects in a paper looking at how mature TOPCon technology really is and what are the next stages of mass production development (p.76).

A paper from Fraunhofer Institute for Solar Energy Systems ISE, looks at the progress in plated metallization (Ni/Cu/Ag or Cu/Ag) for TOPCon and HJ architectures (p.62).

imec provides an overview paper that supports further efficiency gains with bifacial cell interconnect technologies that have further benefits for the adoption of shingled bifacial cells and bifacial back-contacts (p.26).

In a partnership paper, Helmholtz-Zentrum Berlin, PVcomB and VON ARDENNE discuss approaches for optimizing the performance and cost of HJ cells with focus on transparent conductive oxide processing (p.86).

Although half-cut cell and multi-cut variations have been around for decades, larger wafer sizes are driving widespread adoption with PV modules achieving 500Wp performance, already in limited volume production. A collaboration between 3D-Micromac, Fraunhofer Center for Silicon Photovoltaics CSP, 3Cell Engineering and Leipzig University of Applied Sciences, highlights that thermal laser separation technology for half-cut cells provides a pathway for further reductions in electrical recombination losses, as well as on demonstrating improved performance and reliability of shingled modules (p.41).

A contribution by Aurora Solar Technologies, WAVELABS Solar Metrology Systems, 3Sino-American Silicon (SAS) Products and Solar Energy Research Institute of Singapore (SERIS), strongly advises that with terawatt levels of solar production needed for the global energy transition, advanced manufacturing concepts must be implemented to support these new volumes of production and inline solar cell metrology data provides a key support element (p.16).

Finally, a paper presented by Suntech reminds PV module manufacturers of the continued need for product durability, especially in high-humidity environments after extensive in-house testing (p.48).

Importantly at this time, be safe.

**Mark Osborne**  
Senior News Editor and Technical Publishing Director  
Solar Media Ltd.



# Editorial Advisory Board

Photovoltaics International's primary focus is on assessing existing and new technologies for "real-world" supply chain solutions. The aim is to help engineers, managers and investors to understand the potential of equipment, materials, processes and services that can help the PV industry achieve grid parity. The Photovoltaics International advisory board has been selected to help guide the editorial direction of the technical journal so that it remains relevant to manufacturers and utility-grade installers of photovoltaic technology. The advisory board is made up of leading personnel currently working first-hand in the PV industry.

Our editorial advisory board is made up of senior engineers from PV manufacturers worldwide. Meet some of our board members below:



**Prof Armin Aberle, CEO, Solar Energy Research Institute of Singapore (SERIS), National University of Singapore (NUS)**

Prof Aberle's research focus is on photovoltaic materials, devices and modules. In the 1990s he established the Silicon Photovoltaics Department at the Institute for Solar Energy Research (ISFH) in Hamelin, Germany. He then worked for 10 years in Sydney, Australia as a professor of photovoltaics at the University of New South Wales (UNSW). In 2008 he joined NUS to establish SERIS (as Deputy CEO), with particular responsibility for the creation of a Silicon PV Department.



**Dr. Markus Fischer, Director R&D Processes, Hanwha Q Cells**

Dr. Fischer has more than 15 years' experience in the semiconductor and crystalline silicon photovoltaic industry. He joined Q Cells in 2007 after working in different engineering and management positions with Siemens, Infineon, Philips, and NXP. As Director R&D Processes he is responsible for the process and production equipment development of current and future c-Si solar cell concepts. Dr. Fischer received his Ph.D. in Electrical Engineering in 1997 from the University of Stuttgart. Since 2010 he has been a co-chairman of the SEMI International Technology Roadmap for Photovoltaic.



**Dr. Thorsten Dullweber, R&D Group Leader at the Institute for Solar Energy Research Hamelin (ISFH)**

Dr. Dullweber's research focuses on high efficiency industrial-type PERC silicon solar cells and ultra-fine-line screen-printed Ag front contacts. His group has contributed many journal and conference publications as well as industry-wide recognized research results. Before joining ISFH in 2009, Dr. Dullweber worked for nine years in the microelectronics industry at Siemens AG and later Infineon Technologies AG. He received his Ph. D. in 2002 for research on Cu(In,Ga)Se<sub>2</sub> thin-film solar cells.



**Dr. Wei Shan, Chief Scientist, JA Solar**

Dr. Wei Shan has been with JA Solar since 2008 and is currently the Chief Scientist and head of R&D. With more than 30 years' experience in R&D in a wider variety of semiconductor material systems and devices, he has published over 150 peer-reviewed journal articles and prestigious conference papers, as well as six book chapters.



**Florian Clement, Head of Group, MWT solar cells/printing technology, Fraunhofer ISE**

Dr. Clement received his Ph.D in 2009 from the University of Freiburg. He studied physics at the Ludwigs-Maximilian-University of Munich and the University of Freiburg and obtained his diploma degree in 2005. His research is focused on the development, analysis and characterization of highly efficient, industrially feasible MWT solar cells with rear side passivation, so called HIP-MWT devices, and on new printing technologies for silicon solar cell processing.



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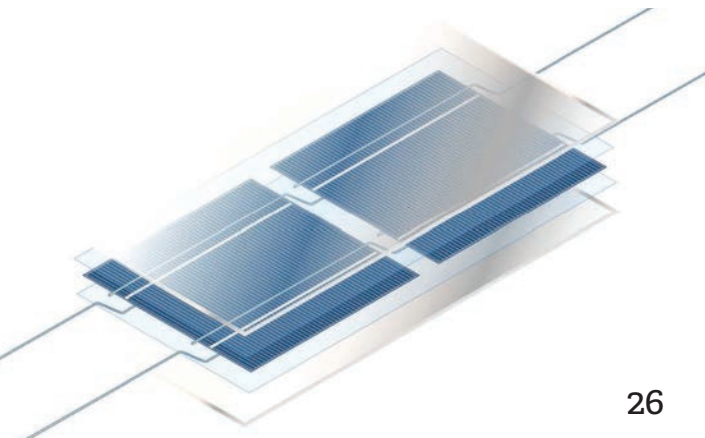
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*<sup>1</sup>Aurora Solar Technologies Inc., North Vancouver, Canada; <sup>2</sup>WAVELABS Solar Metrology Systems GmbH, Leipzig, Germany; <sup>3</sup>Sino-American Silicon (SAS) Products Ltd, Hsinchu, Taiwan; <sup>4</sup>Solar Energy Research Institute of Singapore (SERIS), Singapore*

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*<sup>1</sup>Helmholtz-Zentrum Berlin, PVcomB, Berlin, Germany; <sup>2</sup>VON ARDENNE GmbH, Dresden, Germany*
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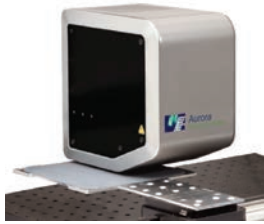




# Product reviews

## Cell Processing: **Aurora Solar Technologies**

**AST offers measurement of both emitter surface concentration and sheet resistance in the DM-110h**



**Product Outline:** Aurora Solar Technologies (AST) has introduced a new emitter surface concentration measurement feature in their 'DM-110h' product for diffusion furnace monitoring and process control.

**Problem:** Emitter surface concentration is the determining factor

in emitter bulk and surface recombination, and therefore the open-circuit voltage (VOC) of finished PV cells. It also plays a crucial role in the metal-semiconductor contact formation and therefore the fill factor (FF). This strong correlation to finished cell I-V parameters – much stronger than sheet resistance – makes it the best metric for quality control and yield in PV cell emitter fabrication, which is commonly achieved by use of a diffusion process. But until now, the only way to determine surface concentration has been through laborious destructive methods, such as electrochemical capacitance-voltage testing, on small areas of individual wafers. This has rendered it an impractical measure for monitoring and controlling diffusion furnace performance.

**Solution:** Aurora's patented infrared reflectometry (IRR) technology in the DM-110h measurement instrument is sensitive to the spatial distribution of dopant atoms within the emitter. This is in contrast to a four-point probe or SPV/JPV measurements, which are sensitive only to the emitter's total dopant concentration. Using this unique ability of the IRR technology, Aurora now offers measurement of both emitter surface concentration and sheet resistance in the DM-110h.

**Applications:** Both surface concentration and sheet resistance measurements.

**Platform:** The DM-110h measurement system consists of a compact measurement head, designed as a unit to fit within wafer cassette load-unload automation. Using Aurora's 'Visualize' quality control system for integration of measurements with process tools to provide real-time 3D visualization of intra-tool dynamics, both spatially and by batch.

**Availability:** Pre-ordering now and will be globally available early in the third quarter of 2020.

## Cell Processing: **Freiburg Instruments**

**Freiburg Instruments' new version of PIDcon offers bifacial PERC solar cell testing**

**Product Outline:** Freiberg Instruments has introduced a new version of its PIDcon tester, specifically designed for quality control of bifacial PERC (Passivated Emitter Rear Cell) and PERC+ solar cells and the ability to also measure AL-BSF, PERT, PERL and IBC solar cells.

**Problem:** In recent years bifacial solar modules have become increasingly widely used, offering many advantages over traditional solar modules: power can be produced from both sides, they are often more durable, because both sides are UV resistant, and potential-induced degradation (PID) was believed to be reduced, since the bifacial module is frameless. But recent investigations show that bifacial solar cells are sensitive to new types of PID at the rear side. One of them is the polarization PID (PID-p) and is caused by the depolarization of the AlOx passivation layer. Another PID mechanism was found to be caused by local corrosion of the silicon wafer beneath the AlOx and SiNy capping layer (PID-c).

## PV Modules: **Ecoprogetti**

**Ecoprogetti's automatic bussing machine offers greater speed and flexibility than manual cell interconnect**

**Product Outline:** Ecoprogetti's automatic bussing machine performs the induction soldering of the interconnections between the strings. Today, the machine is optimized to work on the head, middle (centralized panels) and lower part of the module,



providing a complete and high-quality bussing with high throughput.

**Problem:** Due to the growing trend to limit cell-to-module (CTM) losses in high-efficiency cells, the number of busbars (BB) per-cell is increasing from four to six and even 12. As a result, the manual operation of interconnections' soldering becomes slower due to the increase in interconnection points to solder, reducing throughput and increasing production costs.

**Solution:** The automatic bussing machine ensures high speed, quick and reliable interconnection soldering process (bussing without the need of operators), enclosed in a compact footprint ensuring a higher number of modules per hour with the possibility to work with a range of different panel. Ecoprogetti has upgraded the Automatic Bussing Machine, which now operates at high speed with improved efficiency, while also improving the module quality. The achieved speed is lower than 30 seconds, depending on the design of the module and with certain designs the cycle time can go down to 25 seconds/module. The automatic loading, centering and unloading systems are integrated in the machine. The whole ribbon preparation process is performed by the machine, from the ribbon cutting and bending (L bend) to the soldering.

**Applications:** Replace of manual bussing operations in PV module production lines.

**Platform:** With this high-speed cycle times (<30sec/panel) Ecoprogetti's automatic bussing can manage a production line of up to 300MW/year, increasing time and quality efficiency in a smaller footprint. The machine can work with 5,6 or 12 busbars, and with modules of 60 or 72 cells; half cut cells provision is available as an option.

**Availability:** Currently available.

**Solution:** In order to test cells for these kinds of PID, the PIDcon bifacial was developed. It is stressing the complete cell with temperature, illumination and high voltage, which can be polarized in both directions. By measuring the IV curve under illumination the PID sensitivity can be determined.



**Applications:** PID detection at cell level. Research, Production & Quality Control of PERC, AL-BSF, PERC+, bifacial PERC, PERT, PERL and IBC solar cells

**Platform:** PIDcon was developed in cooperation with Fraunhofer CSP. Undertakes Measurement of: Rparallel, leakage current, IV curve under illumination. Test duration: 4 hours (typical). Easy to use bench top device with no climate chamber necessary.

**Availability:** Currently available.

# PV manufacturing capacity expansion announcements hit new records

Mark Osborne, Senior News Editor, *Photovoltaics International*

## Abstract

PV manufacturing capacity expansion announcements in 2019 were a stark contrast to 2018, when major policy changes in China impacted the upstream supply chain. This paper looks in detail at not only a significant recovery in capacity expansions throughout the year but also new trends in the capacity scale of announcements and a marked shift in wafer sizes and cell technology. 2019 was also notable for the dominance of Chinese manufacturers announcing new expansions, specifically in China. This was made at the expense of further globalization and a collapse in new announcements in Europe, South East Asia and North America, despite strong downstream PV installation growth. Finally, the paper details an unprecedented level of solar industry capacity expansion plans that were announced in just the first quarter of 2020, easily surpassing any total annual plans in the history of the industry.

## 2019 analysis by quarter

### Q1 2019: solar cells dominate

With the collapse in capacity expansion announcements in the second half of 2018, primarily due to the lack of activity in China, which plummeted to a staggering 40MW, the first quarter of 2019 set a new course for much of the year. The first quarter was dominated by high-efficiency mono cell plans that totalled 10,200MW in January. This was in contrast to the lack of any new solar cell expansions announced in the third quarter of 2018, and only a global total of 590MW being announced in the fourth quarter of 2018 (Fig. 1).

Only one major solar cell expansion plan, however, was announced in January, while the other was for 200MW of mono passivated emitter rear cell (PERC) capacity, via Taiwan-based Tainergy Tech shifting reduced total capacity from China and Taiwan to a new plant in Vietnam with a nameplate capacity of 650MW.

The major announcement in the quarter came from Jolywood (Suzhou) Sunwatt Co. The company has an annual output of 2.1GW of n-type mono tunnel oxide passivated contact (TOPCon) technology, initially developed at Fraunhofer ISE. Jolywood has launched TOPCon modules with seven busbars and incorporating high-efficiency half-cut cells, with power outputs of 440Wp and above. TOPCon cell conversion efficiencies had reached 23.36% by mid-

2019. In January 2019, the company announced plans to establish a strategic partnership with Huajun Industrial, part of the Huajun Group, to expand cell capacity by a further 10GW in Quzhou, China.

In February 2019, total cell capacity expansions announced totalled 6,370MW, but from just three companies. The most significant announcement was plans by China-based PV manufacturer GS-Solar to break ground a 5GW manufacturing base in Jinjiang City. The first phase of the project is expected to be 2GW of heterojunction (HJ) solar cells with an RMB5bn (US\$732m) investment. GS-Solar is targeting 25% cell conversion efficiencies in the new production plant.

News soon followed that Panasonic was transferring a 90% stake in its heterojunction intrinsic layer (HIT) solar cell technology and its plant in Malaysia to GS-Solar as part of a wider collaboration on HIT production expansion and R&D. GS-Solar would become the principal owner and operator of Panasonic's Malaysia plant, while a new company will be formed in Japan with GS-Solar undertaking all HIT R&D activities, which will entail Panasonic's existing R&D activities being separated from the group.

Solar Module Super League (SMSL) member LONGi Solar, which appears strongly in new capacity expansions in 2019, kicked off the year with plans for a 1,259MW mono PERC expansion at its facility in Malaysia.

Rounding-up cell announcements in February was a joint venture between European companies SoliTek and Valoe to expand production of HJ cells by 60MW at a facility in Vilnius, Lithuania, with plans to double capacity to 120MW in the future.

In March 2019, a total of 5,550MW of new solar cell capacity expansions were announced. Again, only three companies accounted for the total. Major SMSLs JinkoSolar and Canadian Solar announced solar cell expansions of 3,000MW and 1,550MW, respectively, at the time of announcing fourth quarter 2018 and full-year financial results. However, the key news came from Turkish industrial and PV project developer EkoRE, which held a groundbreaking ceremony on 11 March 2019 for the world's first vertically integrated HJ technology cell/module factory in Turkey, with an expected nameplate capacity of 1,000MW.

The vertically integrated HJ technology plant will be the first in the world to integrate n-type

**“With the collapse in capacity expansion announcements in the second half of 2018, the first quarter of 2019 set a new course for much of the year.”**

monocrystalline ingot and wafer production through to assembled solar modules at one manufacturing site. EkoRE said that the n-type Czochralski crystal pulling factory would have an initial nameplate capacity of 2GW, while the cell and module capacity would initially be 1GW each. The company is collaborating with HJ equipment and technology specialist Meyer Burger.

Total solar cell capacity expansion plans in the first quarter of 2019 totalled 22,120MW (Fig. 2).

There were no new dedicated module assembly capacity expansion plans announced in January or February 2019. However, in March, Jiangsu Seraphim Solar System in partnership with Shanxi Lu'An Photovoltaics Technology Co. announced a 1,000MW advanced module assembly plant in Shanxi province, China, to produce half-cell, dual-glass half-cell and bifacial half-cell PV modules.

SMSL's JinkoSolar and Canadian Solar announced module assembly expansions of 5,000MW and 2,400MW, respectively at the same time as announcing solar cell expansions planned in 2019.

Total dedicated module assembly plans in the first quarter of 2019 totalled 7,500MW.

### Q2 2019: PERC cells dominate

The second quarter of 2019 was notable for a few major PERC cell capacity announcements, led by SMSL member LONGi Solar. In April 2019, the company announced plans for a 5,000MW high-efficiency mono PERC cell plant to be built in Ningxia, China. This was accompanied by a 3,000MW cell plant to be located in Yinchuan, China. Also in April, Zhangjiakou HuanOu International (a subsidiary of Tianjin Zhonghuan Semiconductor) announced plans for a 500MW p-type mono PERC cell plant in Zhangjiakou, China.

However, the most notable plans were announced by REC Group, which planned to expand HJ cell and module capacity by 500MW at its Singapore manufacturing hub. Although cited as a 600MW expansion, REC Group had already established 100MW of HJ production in 2018. Meyer Burger is a strategic partner with REC Group.

Only one solar cell expansion was announced in May, which related to China-based Sunport Power adding 1GW of metal wrap-through (MWT) cell capacity in Xuzhou, China. There were no further solar cell expansion plans announced in June.

Second quarter of 2019 solar cell capacity expansion announcements totalled around 11,000MW.

As with the halving of new cell announcements in the second quarter of 2019, compared with the first quarter, PV module assembly plans also subdued.

In April, along with Zhangjiakou HuanOu International's planned 500MW cell plant, a module assembly plant of the same capacity was also announced. Also notable in April, was the 500MW fully automated module assembly plant planned by AE Solar in Kutaisi, Georgia.

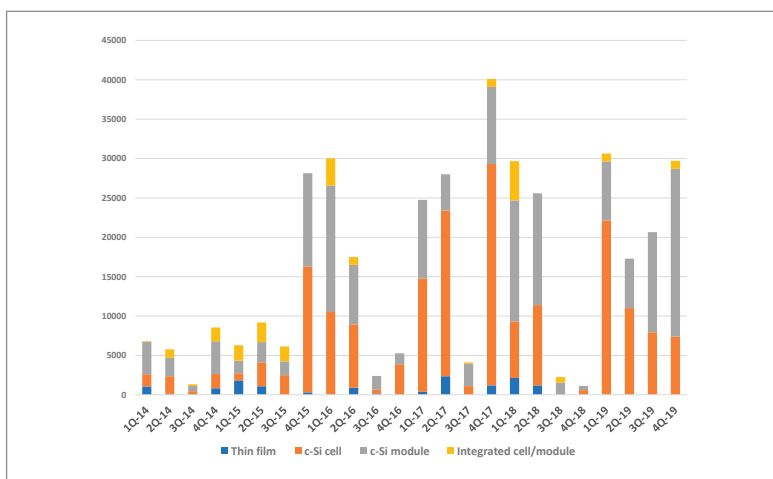


Figure 1. Total quarterly capacity expansion announcements by product type 2014–2019 (MW).

May followed a similar trend with Sunport Power's matching 1,000MW MWT module assembly expansion and Philadelphia Solar planning to add 280MW of module assembly in the Al Qastal Industrial Area, Amman, Jordan. The only announcement in June 2019 was LONGi Solar's plans for a 5,000MW module assembly plant in Taizhou New Energy Industrial Park, Taizhou City, Zhejiang Province, China.

Total module assembly capacity expansion plans in the second quarter of 2019 reached 6,285MW.

### Q3 2019: heterojunction dominates

Total capacity expansions in Q3 2019 were higher than in the second quarter, with major plans being announced for new HJ cell and module assembly plants, primarily in China, in the third quarter.

A total of over 7,500MW of new HJ solar cell plants were announced in July 2019 by three companies: Jiangsu Akcome Science & Technology Co, Risen Energy and an unidentified customer of Meyer Burger in North America. Akcome plans a 5,000MW HJ plant in Changxing, Zhejiang province, China, while Risen Energy is planning a 2,500MW HJ plant in Ninghai, Hejiang province, China. Few details have been reported by Meyer Burger, other than the signing of a US\$100m heterojunction equipment order.

In August, Oxford PV confirmed its 250MW perovskite-on-silicon solar cell manufacturing line being added to its facility in Brandenburg an der Havel, Germany. No solar cell capacity expansions were announced in September.

Total solar cell capacity expansions announced in the third quarter of 2019 reached almost 8,000MW.

Along with Akcome's and Risen Energy's HJ cell announcements, equivalent capacity is planned for module assembly. Also of note in July was a further 5,000MW assembly plant announced by LONGi Solar, which would be located in the Xianyang High-tech Industrial Development Zone of Xianyang City, China.

There were no module assembly expansion plans announced in August and only one in September – a 500MW expansion confirmed by Waaree Energies





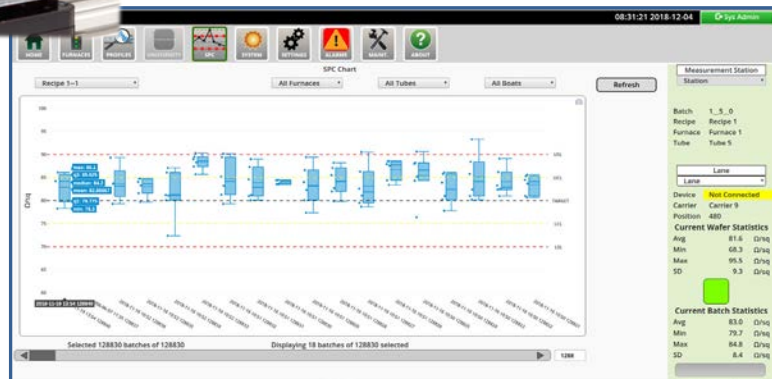
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at its facility in Vapi, Gujarat, India bringing its total capacity to 2,000MW.

New module assembly capacity announced in the third quarter of 2019 reached a total of over 13,200MW.

#### Q4 2019: module assembly dominates

With module assembly capacity plans exceeding cell expansion plans in the third quarter of 2019, that trend continued in the fourth quarter, which witnessed an overall increase in module assembly capacity expansion figures above those in the second and third quarters.

October 2019 was dominated by one company. LONGi announced a 5,000MW mono PERC solar cell plant in Xi'an Xincheng City, China. No other solar cell expansions were announced in this month.

As in the previous month, November had only one company announcing solar cell expansions. Jinneng Clean Energy Technology (Jinergy) announced a 2,300MW mono PERC cell expansion, as well as a doubling of capacity of an existing HJ line to 200MW. The PERC expansion takes nameplate capacity to 4.5GW.

In December, no expansions were announced for solar cell expansions. However, Jiangsu Akcome Science & Technology Co announced a 1,000MW integrated HJT cell and module project.

In the fourth quarter of 2019, total solar cell expansion announcements topped 7,400MW.

LONGi Solar was also the only company to announce a further 10,000MW of new module assembly plants in October. The company is planning a 5,000MW assembly plant, dubbed Luzhou Phase II, in Zhangzhou, China. The second 5,000MW assembly plant is to be built in Xianyang High-tech Industrial Development Zone, Xianyang, China.

Module assembly also dominated new capacity announcements in November, as over 6,000MW was announced from four companies. Because of stronger demand than expected, SMSL members JinkoSolar and Canadian Solar announced module assembly expansion plans of 1,000MW and 2,000MW, respectively. Included in the November figures was Jinergy's 2,300MW assembly expansion to go along with the mono PERC cell expansion. Finally, India-based Vikram Solar proposed increasing module assembly by 1,000MW should Indian government policies support the expansion. The expansion would almost double module capacity.

Wuxi Suntech, on the last day of the year, announced a new 5GW high-efficiency, large-area wafer, fully automated module assembly plant in the Yangzhou Economic and Technological Development Zone, Jiangsu province, that would be operational in 2020.

In the fourth quarter of 2019, announced module assembly expansion plans totalled 26,300MW.

#### 2019 geographical review

With a major pick-up in capacity expansion plans

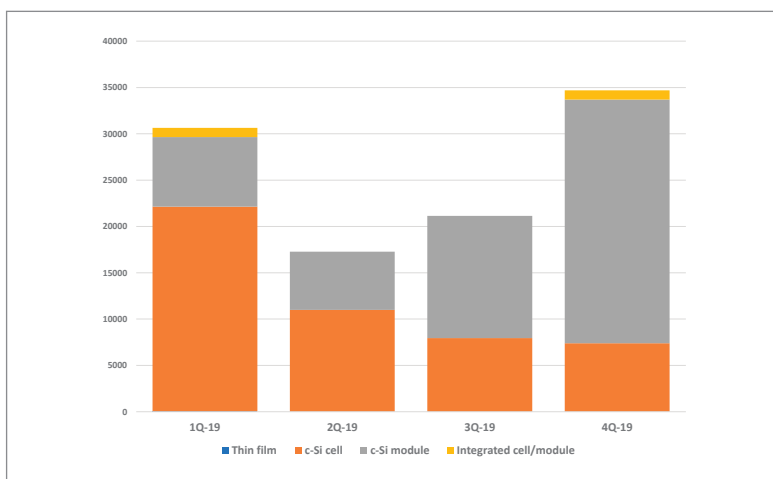


Figure 2. Quarterly capacity expansion announcements by product type in 2019 (MW).

“With module assembly capacity plans exceeding cell expansion plans in the third quarter of 2019, that trend continued in the fourth quarter.”

in 2019, compared with 2018, driven by almost complete shutdown in future planning from Chinese manufacturers, the geographical capacity expansion map looks completely different to that seen in 2018 (Fig. 3).

In 2018, China accounted for only around 20,000MW of total combined cell, module and thin-film capacity expansions, or 37% of the total; India accounted for 28% of the total, while Egypt, the USA and Turkey accounted for 18%, 7% and 5%, respectively. A total of 15 countries announced capacity expansion plans in 2018.

In 2019, however, China accounted for over 90,000MW of combined cell, module and thin-film capacity expansions, or 94% of the total; India, Malaysia and Turkey accounted for 2%, 1% and 1%, respectively. A total of only 13 countries made announcements of capacity expansion plans in 2019.

The highly speculative 16GW of combined expansion plans in India in 2018 dwindled to just 1,000MW of the 1,500MW total in 2019. Clearly there has been major shift back to China in 2019. Expansions in South East Asia (Malaysia, Indonesia and Vietnam) have been minimal, and the small flurry of module assembly activity in the USA in 2018 did not continue into 2019.

Small, sporadic announcements, typically module assembly related, occurred in Jordan and Saudi Arabia.

#### 2019 manufacturing trends

A trend noticeable in the last three years has been the scale of company announcements, particularly in China. Typically, the 500MW expansion or new plant announcements have given way to nameplate capacities of 5,000MW and above in 2018 and 2019. Indeed, 10,000MW expansion plans have been noted in 2019.

However, many plans announced that are in the 5,000 to 10,000MW range tend to include

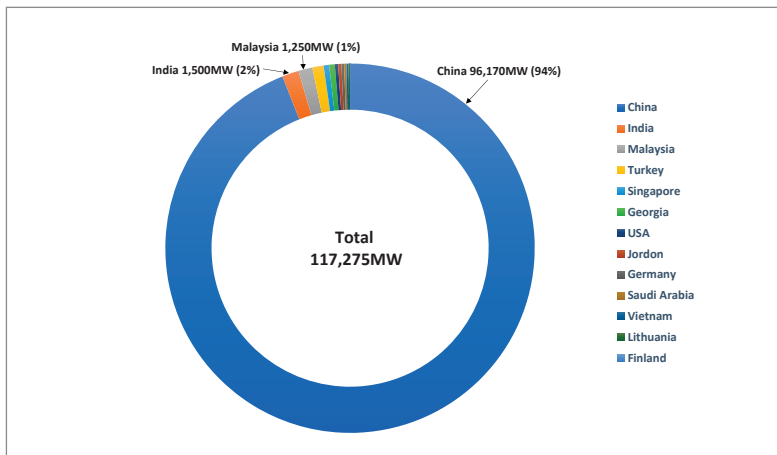


Figure 3. Total capacity expansion announcements by country in 2019 (MW).

multiple phases that can span several years at a given location(s). The scale of many greenfield site announcements means that timelines for construction through to tool install and ramp lends itself to an initial multi-gigawatt phase, especially with new solar cell capacity, taking longer than 12 months. The following tool install and ramp phases can be done significantly faster.

A consequence of multiphase build-outs is that some companies that made major expansion announcements in 2017, for example, have not announced new capacity expansions since, as they execute on multiphase, multi-year plans previously initiated. This has led to a drop in the number of companies announcing plans on an annual basis. However, it also provides insight into when these

sorts of company might announce new multi-gigawatt, multiphase and multi-year plans.

Another trend gaining momentum has been the need to dedicate capacity within a 2,000 to 5,000MW solar cell plant to different large-area wafer sizes. Though clearly a strategy seen with major merchant cell producers, such as Tongwei Solar and Aiko Solar, rapid migration to several large-area wafer sizes at SMSLs, in order to benefit from lower cost per watt at large plants, has also meant dedicated cell lines for different wafer sizes. That trend should be short-lived, as within the next few years the industry is more likely to end up adopting the largest wafer size (210mm × 210mm), which was just entering volume production at the end of 2019. However, it should also mean a forthcoming phase of tool upgrading at the multi-gigawatt level, which would also boost nameplate capacity at existing cell plants.

### 2019 summary

Total solar cell capacity expansion announcements in 2019 topped 48,000MW, compared with almost 18,000MW in 2018. With cell expansions, primarily for high-efficiency p-type mono PERC, dominant in 2018, heterojunction cell technology announcements have significantly increased in 2019, reaching at least 14,000MW, compared with just over 1,000MW in 2018. It should be noted, however, that with many HJ announcements being multi-gigawatt plans, these should be treated as multi-year projects, not least because many could initially only deploy pilot manufacturing lines.

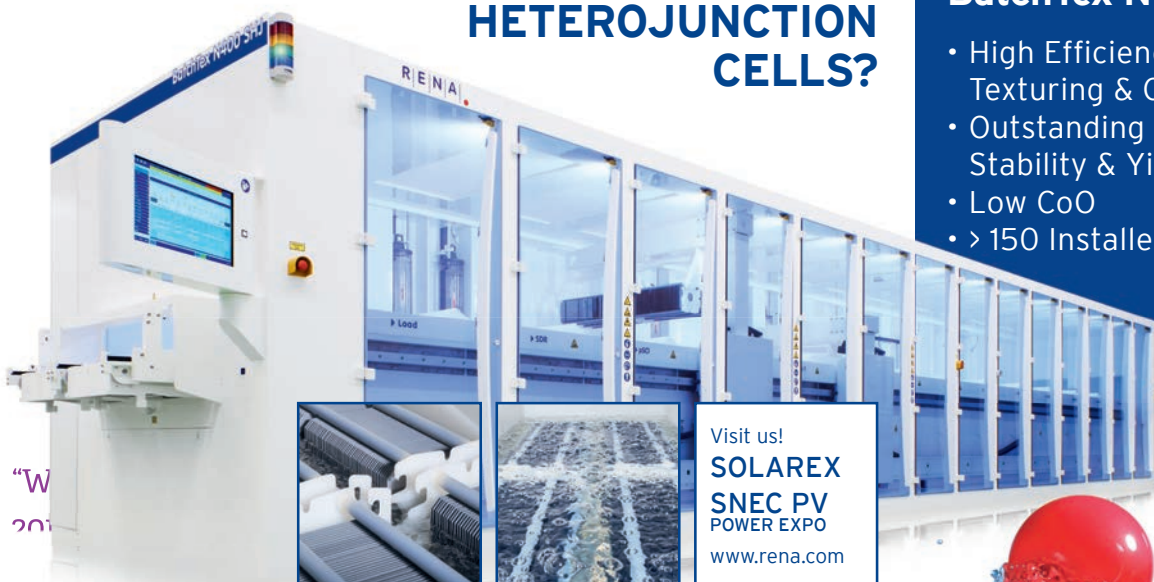
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Dedicated module assembly capacity expansion announcements in 2019 also increased, topping 53,000MW, compared with 31,600MW in 2018.

Integrated cell and module capacity (where stated) was around 2,000MW in 2019, compared with 5,700MW in 2018.

Solar cell capacity expansions and module assembly expansions were overall well balanced in 2019, despite greater module assembly activity in the second half of the year.

Thin-film expansion announcements in 2019 were almost non-existent and well below 100MW. However, as noted in the manufacturing trends section of this paper, since 2017 there have been announcements of multi-gigawatt multiphase projects, which included thin-film companies. As these project expansions reach completion, new announcements could happen in 2020.

Combined total capacity expansions in 2019 sailed past 117,000MW, compared with over 58,000MW in 2018. As a result, 2019 was a record year for nameplate capacity expansion announcements, surpassing 2017, when announcements topped 97,000MW.

### A record setting Q1 2020

Preliminary data compiled by PV Tech highlights an unprecedented level of announcements of solar industry capacity expansion plans in just the first quarter of 2020, easily surpassing any total annual plans in the history of the industry (Fig. 4).

PV Tech’s preliminary analysis of upstream manufacturing capacity expansion announcements in Q1 2020, across ingot/wafer, solar cell and module assembly segments combined, exceeded a staggering 500GW (Fig. 5). To put this in perspective, this is more than double PV Tech’s preliminary analysis of capacity expansion plans announced in 2019 (a combined total of just over 228GW). The vast majority of announcements in Q1 2020 were driven by China-based PV manufacturers revealing plans for facilities in China.

### Ingot/wafer expansions

Capacity expansion announcements in Q1 2020 related to the combined ingot and wafer segment exceeded 123GW, compared with approximately 118GW of expansion plans announced in all of 2019, according to preliminary PV Tech data.

### Solar cell expansions

Solar cell (c-Si) capacity expansion announcements in Q1 easily topped 212GW. This contrasts with PV Tech’s preliminary 2019 figures of planned expansions topping 53GW.

### PV module assembly expansions

With regard to total module assembly capacity expansion announcements in just Q1 2020, preliminary figures suggest almost 164GW has been reached. In comparison, total module assembly capacity expansion plans in 2019 reached nearly 57GW.

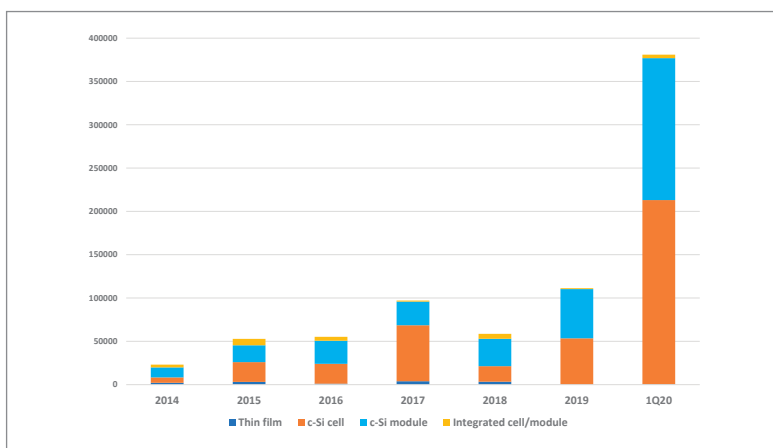


Figure 4. Annual capacity expansion plans by product type in 2019 vs. Q1 2020 (MW).

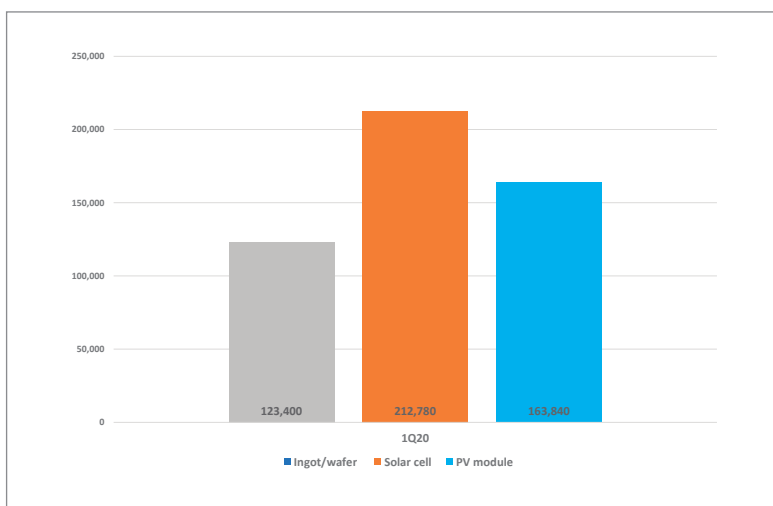


Figure 5. Capacity expansion announcements in Q1 2020 by product type (MW).

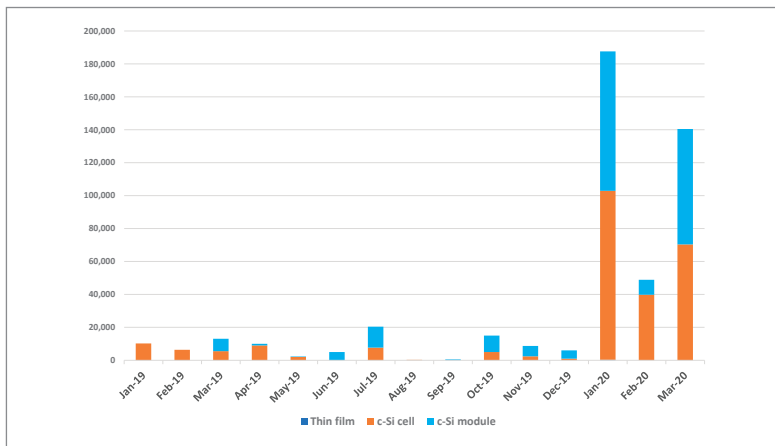
## Q1 2020 by month

### January 2020

The most active month for capacity expansion announcements in the first quarter of 2020 was January, leading up to Chinese New Year celebrations. A preliminary total of 22 companies announced expansion plans in this month, which was dominated by over 102GW of solar cell expansion announcements, followed by module assembly plans totalling almost 85GW (Fig. 6). Preliminary ingot/wafer expansions exceeded 52GW in January.

Key announcements kicked off in early January, when JA Solar announced plans to expand mono solar cell and module assembly capacity by 10GW each. Major merchant cell producer Aiko Solar announced expected capacity ramps over a three-year period totalling 12.8GW in 2020 alone, and totalling almost 36GW through 2022.

**“PV Tech’s preliminary analysis of upstream manufacturing capacity expansion announcements in Q1 2020 exceeded a staggering 500GW.”**



**Figure 6. Monthly capacity expansion plans by product type Q1 2020 (MW).**

### February 2020

Not surprisingly, the extended Chinese New Year, travel restrictions and escalating impact of COVID-19 led to only eight companies announcing further capacity expansion plans in February. The month was again dominated by solar cell expansion plans that totalled almost 40GW, with only 9GW of module assembly expansion plans and zero plans to add ingot/wafer capacity, according to PV Tech's preliminary analysis.

Highlights included an announcement by major merchant solar cell producer Tongwei Group of further expansions plans which entailed a new 30GW manufacturing hub. JA Solar's second wave of plans totalling 8.6GW is also of note, including cell technology upgrades that would boost nameplate capacity in 2020.

### March 2020

Despite COVID-19 challenges escalating through early to mid-March, well over 70GW of new ingot/wafer capacity expansion plans were announced in China, followed by just over 70GW of solar cell and 70GW of module assembly plans. Despite the very strong figures, however, only five companies contributed to the preliminary total in March, which was dominated by GCL System Integration Technology (GCL-SI) and LONGi Group.

In late March, GCL-SI announced a new 60GW megacomplex to house the complete manufacturing supply chain to feed 60GW of annual PV module production in a multiphase, multi-year plan. LONGi also announced another wave of future expansions that included a 10GW mono ingot project, a 7.5GW mono solar cell project, a 5GW module assembly project and an advanced integrated cell and module project totalling 680MW.

### Key trends in Q1 2020

With manufacturing equipment costs significantly lower than five years ago, having module assembly plants with lower utilization rates has little impact on production costs when companies are already at significant scale. This also applies to solar cell production plants but to a lesser degree.

The large-scale announcements are being fuelled by near-term end-market growth projections, coupled with a major technological race to achieve higher conversion efficiencies and lower production costs. That will also displace more than 100GW of legacy manufacturing from multicrystalline ingot/wafer capacity to p-type and n-type monocrystalline with large-area wafers, to next-generation cell technologies, such as HJT, after the mainstream PERC era.

However, there was a relatively large number (seven) of announcements in Q1 2020 related specifically to integrated high-efficiency (HJT) cell and module projects, totalling around 4,400MW, which could be highly speculative through 2020. The number of HJT announcements in the last 15 months, regardless of some being speculative rather than becoming effective capacity, indicates that HJT is the clear next-generation (post-PERC) choice for PV manufacturers.

It should also be noted that the analysis does not include HJT activity from major mid-term expansions from the likes of GCL-SI, Aiko Solar and Tongwei, which is understood will include HJT production lines in future expansion phases recently announced that span several years.

### Technical notes

#### Preliminary data

The data for the capacity expansion plans for 2019 and Q1 2020 remain 'preliminary' because a number of public-listed companies are still due to report full-year 2019 financial results through to the end of April 2020. Companies will often have added capacity in a financial year that was outside specific announcements or an expansions-only feature, or that can be analysed in annual reports. Therefore, there is a level of backdating necessary as well as time required to obtain confirmations of expansion plans when very little or no data existed.

#### Effective capacity

Historically, capacity expansion announcements are no guarantee that such plans will go ahead. Should plans be executed, the capacity becomes 'effective capacity'. The process can typically take between 12 and 18 months from when plans are announced to when capacity is converted to effective capacity.

Since 2014, PV Tech's analysis has shown that the conversion rate of plans/announcements becoming effective capacity can be as little as 50%. Many factors are at play, including low conversion rates for start-ups or new industry entrants to next-generation technology adopters. Certain countries and regions have also proved to have a history of perennially low conversion rates, some being as high as 90%. The inability to raise necessary funds, changes in market dynamics, and the lack of inward investment incentives are also factors contributing to low conversion rates, after expansion announcements are made.

# Statistical insights from inline solar cell metrology data in a PERC production environment

Johnson Wong<sup>1</sup>, Bernhard Mitchell<sup>2</sup>, Sascha Esefelder<sup>2</sup>, Britta Mette<sup>2</sup>, Budi Tjahjono<sup>3</sup>, Kwan Bum Choi<sup>4</sup>, Jian Wei Ho<sup>4</sup> & Gordon Deans<sup>1</sup>

<sup>1</sup>Aurora Solar Technologies Inc., North Vancouver, Canada; <sup>2</sup>WAVELABS Solar Metrology Systems GmbH, Leipzig, Germany; <sup>3</sup>Sino-American Silicon (SAS) Products Ltd, Hsinchu, Taiwan; <sup>4</sup>Solar Energy Research Institute of Singapore (SERIS), Singapore

## Abstract

The adaptation of solar cell physics models and advanced laboratory-based measurement techniques to enable their use in high-volume, inline solar cell production settings is an exciting development towards implementing Industry 4.0 compliant smart solar cell factories. This paper outlines how a blend of physics-based analysis and statistical data science methods can aid continuous improvement and yield optimization in high-volume solar cell fabrication. A specific example is provided for a passivated emitter, rear locally contacted (PERC) solar cell production environment, where four batches of 500 commercial solar cells are evaluated using  $I-V$  at one-Sun as well as both contacted and contactless spectral response techniques. The spectral response techniques revealed prominent periodic patterns in the cell measurement sequence, which could be traced to the anti-reflection coating deposition process. This process inhomogeneity led to bimodal distributions in each batch with an efficiency difference as large as 0.07% between the modes. Thus, its identification by the spectral response technique is an important first step towards improving the efficiency distribution via deposition uniformity improvement. A yield-oriented cell physics model is used to interpret the various data in the context of underlying cell parameters, forming the basis for previously impractical root cause analysis in complex adverse events, and for process optimization in order to obtain sustained yield improvement in high-volume production.

## Introduction

While the solar industry is undergoing unprecedented levels of capacity expansion – exceeding 500GW across ingot/wafer, solar cell and module assembly segments combined in the first quarter of 2020 [1], the rate at which world electricity sources are transitioning from fossil fuel to renewal energy must further *increase* for the world to ward off disastrous levels of global warming [2]. For PV to do its part, terawatt levels of production will soon be required, and advanced manufacturing concepts must therefore be successfully implemented to support these new volumes of production.

**“Terawatt levels of production will soon be required, and advanced manufacturing concepts must therefore be successfully implemented to support these new volumes of production.”**

The Industry 4.0 framework, which originated in 2011, outlines a number of timely and important concepts that address the need for greater levels of digitization and data analytics as manufacturing continues to scale up. One of these important concepts is the *digital twin*, a near-real-time digital image of a physical object or process that helps optimize business performance [3]. When applied to solar cell manufacturing, a digital twin can be considered to be akin to solar cell device models and fabrication process simulations [4–5]. This opens up the field for analytical modelling, simulation and optimizations that converge to derive value from massive volumes of data, leading to significant improvements in cost and process efficiencies [5].

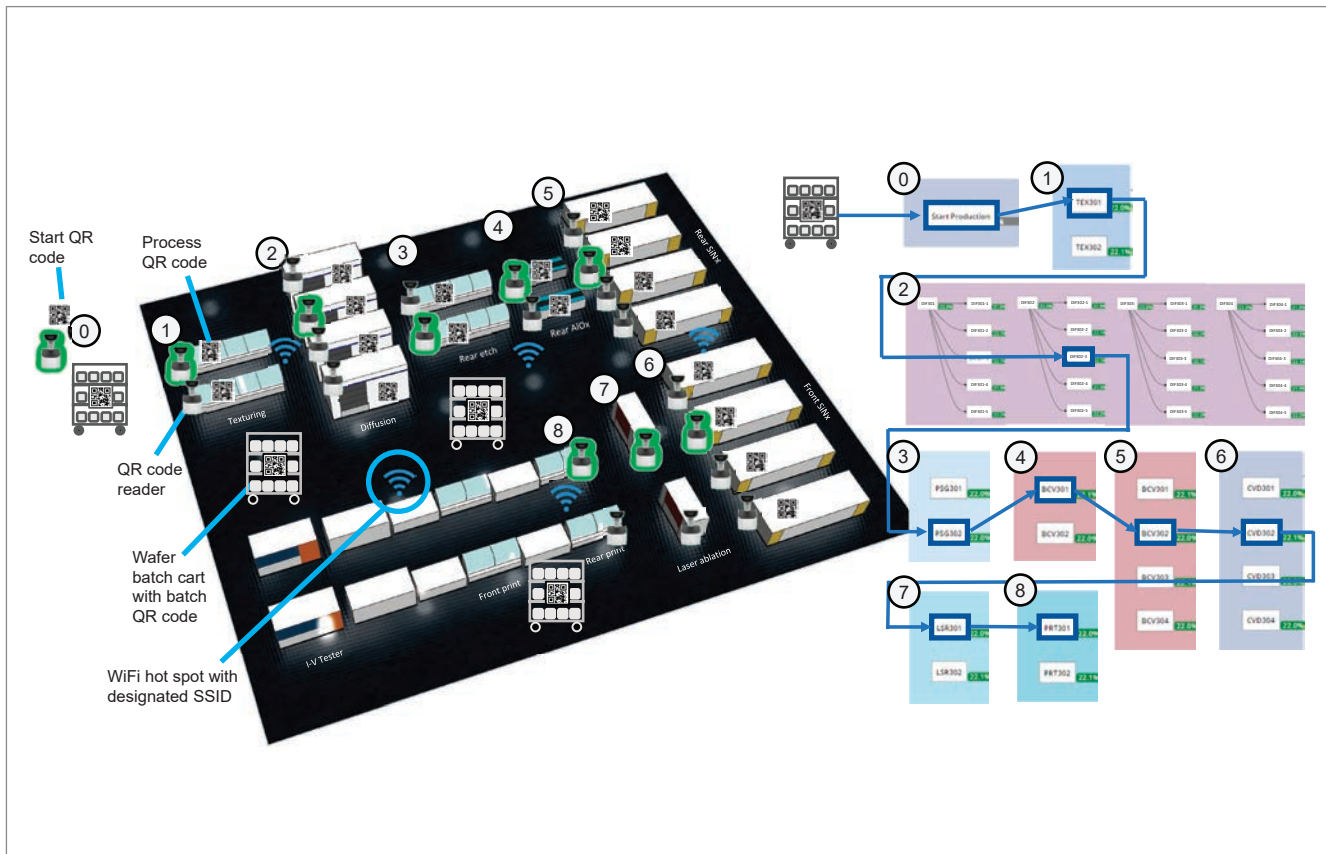
Just as the brain applies a cognitive model of the world on sensory data, a digital twin is effective only if it is fed a continuous, rich set of measurement data derived from the operation of manufacturing processes. In this context, recent trends in solar cell factories point towards an increasing richness of end-of-line measurement data on the finished device, with electroluminescence (EL) and infrared (IR) imaging becoming standard, while the  $I-V$  tester has also gone through innovations that enable it to measure more than just the current–voltage characteristics [6–7]. One of the most exciting developments is the advent of  $I-V$  testers with monochromatic LED illumination that have tuneable spectra and therefore the capability of measuring a solar cell’s relative spectral response [7]. In the laboratory, current–voltage tracing and spectral response are standard and complementary solar cell measurement techniques [8], so their recent incorporation in production line measurement allows lab analysis methods to be adapted to high-volume data in the production line for the purposes of pin-pointing areas of manufacturing improvements.

This paper explores the multivariate statistical information offered when both volume one-Sun  $I-V$  and spectral response data are available for large batches of passivated emitter, rear locally



Batch	Description
1	Baseline
2	Identical processing to batch 1, except for the type of furnace used for phosphorus diffusion
3	Identical processing to batch 1, except for the quartz tube used for phosphorus diffusion
4	Identical processing to batch 1, except for the tool used for rear passivation

**Table 1. Description of the four solar cell batches.**



**Figure 1. Batch path-tracking system using QR code pairing to record the check-in time and process tool/chamber at each step.**

contacted (PERC) solar cells that have undergone different variations in manufacturing processes. For added value, two spectral response techniques are compared: 1) the traditional contacted method, which is based on short-circuit current measurement; and 2) a contactless quantum efficiency (QE) method, which is based on open-circuit luminescence emission measurement [9–10]. The two techniques are performed when the solar cell is exposed to monochromatic illumination. Both kinds of spectral response data are used in conjunction with one-Sun  $I-V$  data to perform intra-batch and inter-batch analysis.

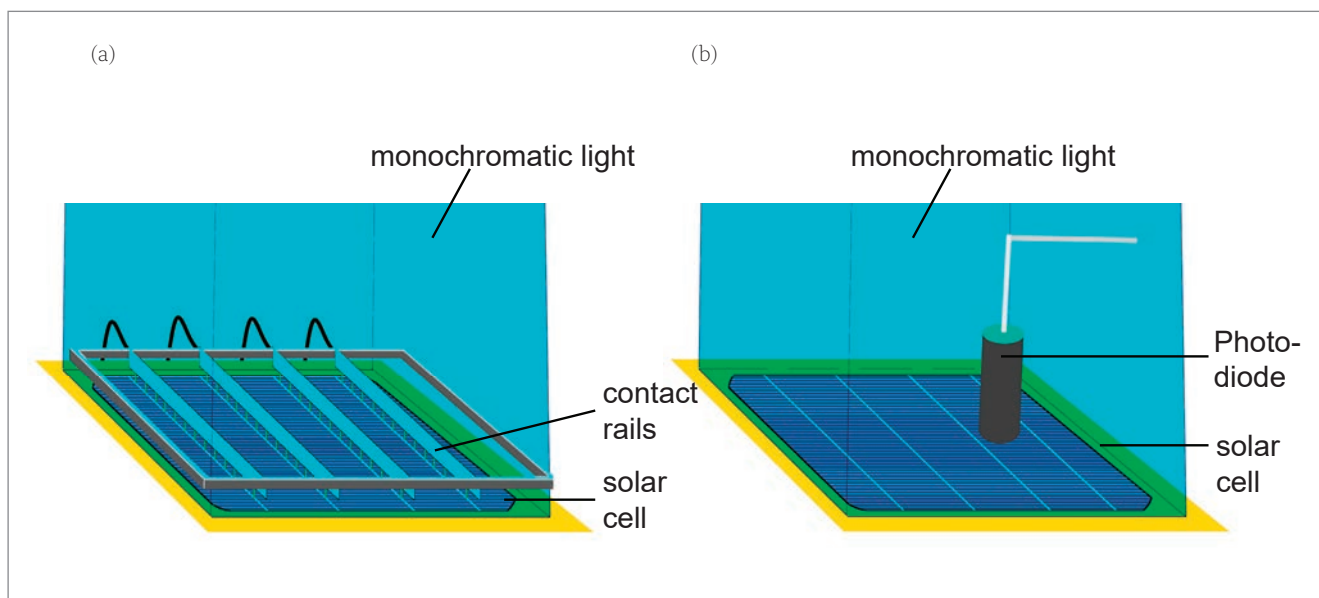
### Cell fabrication and tracking

Four batches of PERC solar cells were fabricated in a volume manufacturing environment. Each batch took a different route through the path of process tools/chambers to create four experimental splits. Table 1 summarizes the differences in the process paths taken by the four batches.

In order to verify that the batches did follow

the intended paths, a batch path-tracking system using QR code scans was implemented to record the check-in times, and specific process tool/chambers used as the cassettes containing each batch were loaded for processing at each process step. The production facility operators were trained and instructed to perform the QR code scans using a handheld reader, which sent the batch QR code and process QR code scan pair to a server in real time. The server timestamped and logged these events in a path-tracking database. Other than logging the check-in events of the four batches, the server computer also consolidated the path data of all batches to give either a plant-wide view, or a tool-comparison view, in which the  $I-V$  parameters of batches moving through different tools could be compared.

The schematic of this path-tracking method is given in Fig. 1, which shows the mapping of the physical factory and tool space to the server database space, as presented on the manufacturing facility view screen. The corresponding process



**Figure 2. (a) Contacted spectral response measurement, with current being measured under short-circuit conditions. (b) Contactless spectral response measurement, with luminescence intensity being measured under open-circuit conditions. Both are performed using monochromatic illumination.**

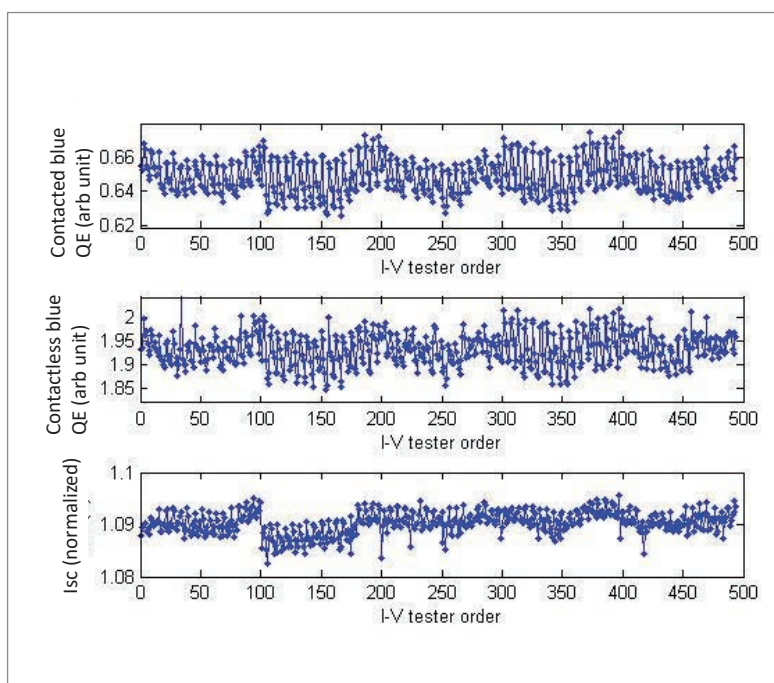
steps in the two spaces are numbered. For illustrative purposes, Fig. 1 also shows an example case where the path information of a batch is recorded. The highlighted QR code readers denote QR code scans, and in the plant-wide view screen, the blue boxes denote the recorded process tool/chambers that were used to process the batch.

### I–V and spectral response measurement

All four batches of solar cells were metallized in the same print line and flashed by the same xenon-lamp-equipped *I–V* tester sorter. For each batch, about 500 contiguous cells were extracted for offline testing. The test sequence consisted of standard one-Sun *I–V* testing using an LED-based illumination, as well as the contacted and contactless implementations of spectral response measurements as described above and in Fig. 2. The contacted technique is based on short-circuit current measurement, and the contactless technique is based on open-circuit luminescence emission measurement. The contacted measurements are taken under monochromatic illumination at 395nm, 686nm, 799nm, 975nm and 1,060nm, while the contactless measurements are taken under monochromatic illumination at 390nm and 660nm.

Because the wavelengths of 686nm and 660nm are very near constant spectral response per unit cell active area, the measurements at these wavelengths can be used to normalize the measurements at other wavelengths. This procedure, while optional for the contacted measurement, is necessary for contactless measurement in order to generate meaningful results [10].

The normalized spectral response at 395nm

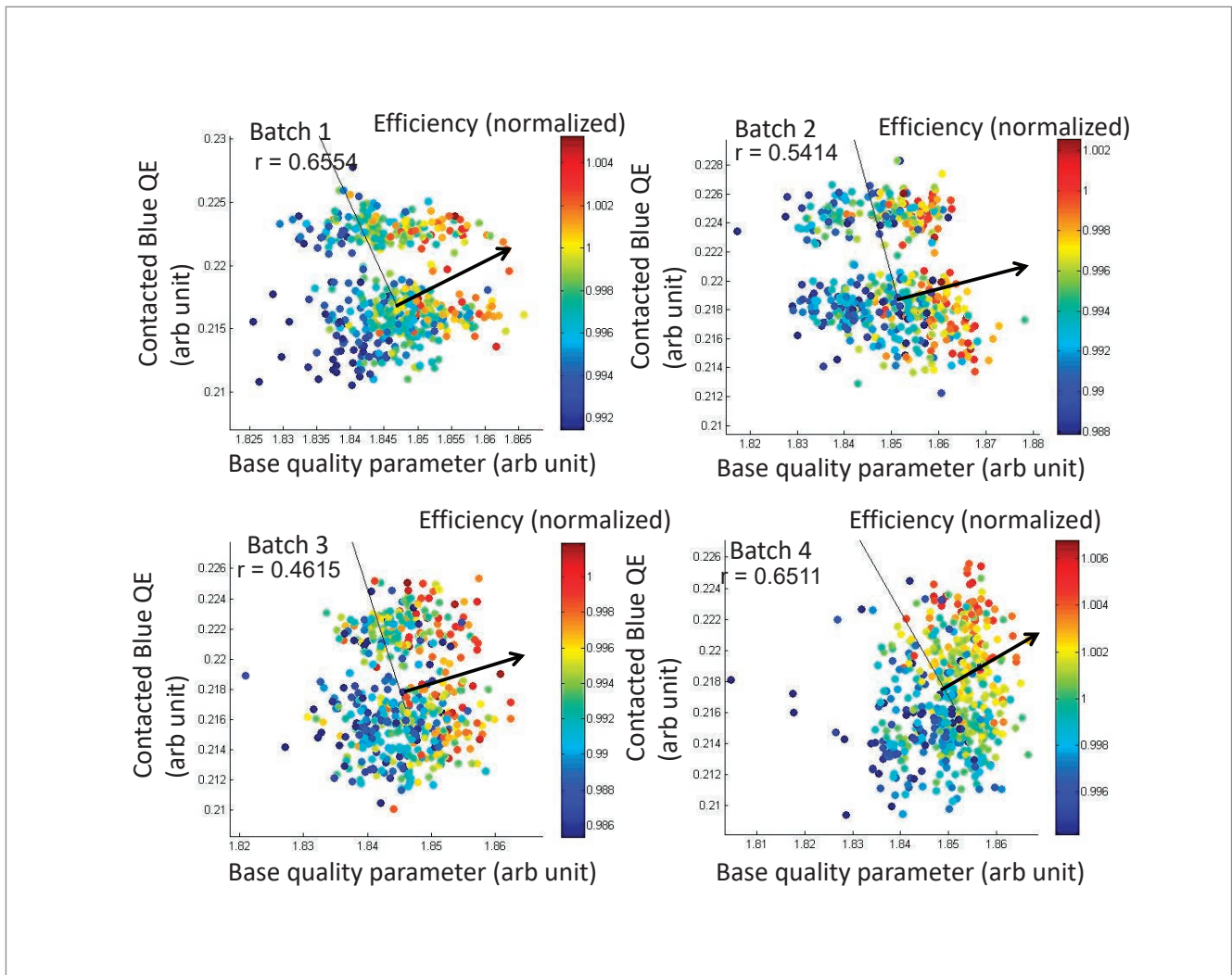


**Figure 3. Blue response in contacted spectral response and contactless response, and the one-Sun short-circuit current ( $I_{sc}$ ) for batch 4 measurement sequence.**

or 390nm is called the *blue response*. It is highly sensitive to the anti-reflection coating thickness and refractive index, and slightly so to emitter passivation quality and emitter bulk recombination. For the contacted spectral response measurement, the response at 975nm or 1,060nm is called the *red response*. It is also highly sensitive to the anti-reflection coating thickness, and slightly sensitive to the base diffusion length.

### Measurement results and discussion

Fig. 3 shows the blue response in contacted spectral measurement and contactless spectral



**Figure 4. Intra-batch scatter plots of efficiency versus the contacted blue response and base quality parameter (derived from the IR response), each shown with the gradient direction.**

measurement, and the one-Sun short-circuit current ( $I_{sc}$ ) for batch 4, with the spatial cell ordering in the batch preserved. Clearly, in all three types of measurement, there is a periodic structure in the batch spatial sequence. In fact, this periodic structure is evident in all four cell batches, but for brevity only that of batch 4 is presented here. By using a correlation technique, it is found that the periodicity in the blue response is eight solar cells. Because this periodicity is observed only in  $I_{sc}$  in the blue spectral response, one can conclude that the periodicity is related to a process tool that influences the anti-reflection coating refractive index, which is most likely the silicon nitride ( $\text{SiN}_x$ ) vacuum deposition tool.

Fig. 3 also shows that the contacted and contactless spectral response techniques produce similar results in the blue response. In fact, the correlation coefficients between the blue responses

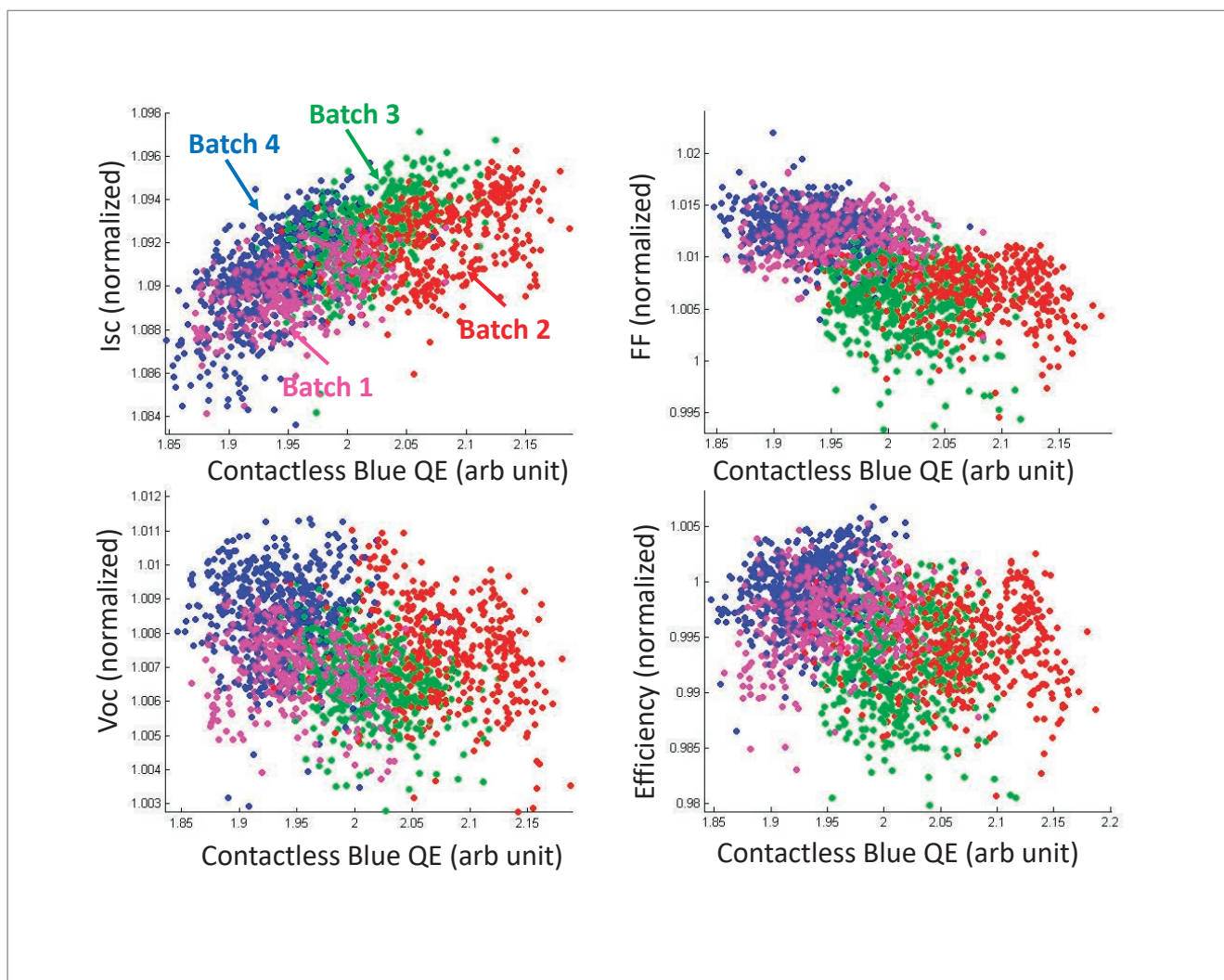
of the two techniques are  $r = 0.957, 0.832, 0.945$  and  $0.963$ , for the four batches, respectively, which is excellent. This shows that, in practice, the cells' blue response can be reliably obtained either by using the contacted spectral response method, preferably integrated in the  $I-V$  tester [8], or by using a contactless device situated at the end-of-line position, close to the  $I-V$  tester.

Having identified and briefly discussed this periodicity in the blue spectral response, it is now desirable to investigate how it and other spectral response results relate to cell efficiency. Fig. 4 shows, within each batch, the scatter plots of efficiency versus the contacted blue spectral response and a base quality parameter (which is derived from the red response), each shown with the gradient direction. As expected, in each case the efficiency trends positively with both the blue response and the base quality parameter.

Examination and use of the blue response can be a significant factor in improving finished cell efficiency and therefore production line yield. Observe from Fig. 4 that each batch has a bimodal distribution: a high blue response mode and a low blue response mode. The differences in median

**“Examination and use of the blue response can be a significant factor in improving finished cell efficiency and therefore production line yield.”**





**Figure 5. Inter-batch trends of contactless blue response versus short-circuit current ( $I_{sc}$ ), fill factor ( $FF$ ), open-circuit voltage ( $V_{oc}$ ) and efficiency.**

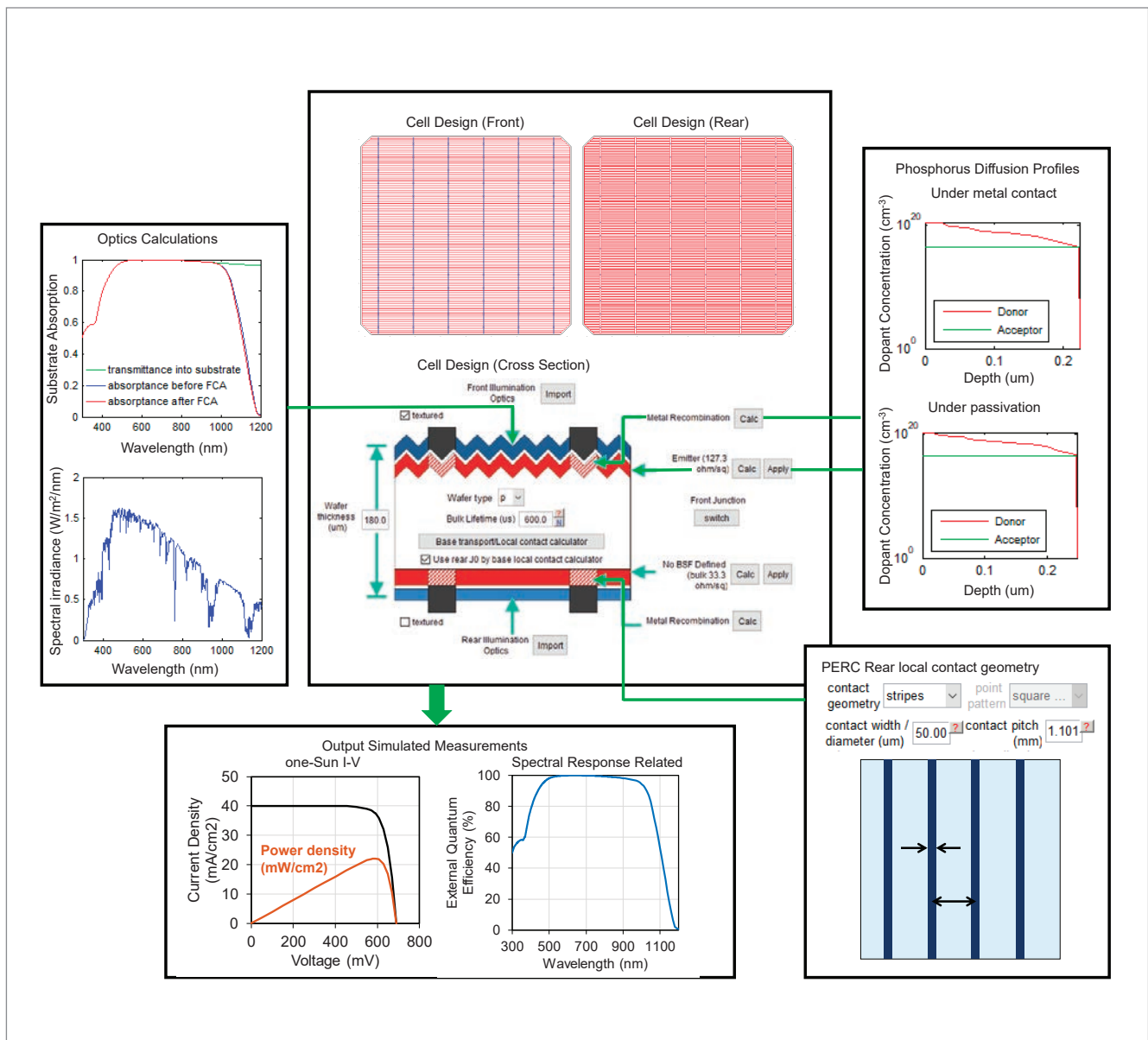
efficiencies between these two modes are 0.02%, 0.02%, 0.04%, 0.07% absolute efficiency points for batches 1 to 4 respectively. These differences are sufficiently significant to make it worthwhile to investigate, and, if possible, reduce or eliminate the  $\text{SiN}_x$  vacuum deposition tool inhomogeneity as a way to reduce the variance and possibly increase the mean of the finished cell efficiency distribution.

Additionally, it turns out that the base quality parameter explains an even more significant part of the total variance in efficiency. There is evidently an improvement in the base quality parameter for batch 4, which was subjected to a different rear-passivation recipe to that of batch 1. This improvement in base quality parameter largely explains the difference in the two batches' efficiencies. Thus, using the base quality parameter to interpret experimental splits – where the intended change is in the rear passivation – can lead to clearer conclusions, more accurate attribution of efficiency changes to the control variable, and potentially more efficient experiments that require fewer samples.

More inter-batch analysis can be carried out by plotting all four batches together in a set

of two-variable plots. Fig. 5 shows four inter-batch trends of contactless blue response versus, respectively, short-circuit current ( $I_{sc}$ ), fill factor ( $FF$ ), open-circuit voltage ( $V_{oc}$ ) and efficiency. Batches 1 and 4 (which differ only by their rear-passivation processing) have a nearly identical blue response and  $I_{sc}$  while batches 2 and 3 (which were processed in a different type of diffusion furnace and in a different diffusion tube compared with batch 1, respectively) have distinctly different blue responses and slightly different short-circuit currents. Thus, the contactless blue response could be a parameter that is more sensitive to changes in emitter profile compared with  $I-V$  parameters, as evident in its ability to differentiate batches that have different emitter processing.

There is also a negative trend between the blue response and the fill factor among the batches. This trend makes sense if it is posited that emitters with higher surface concentration have higher Auger and surface recombination, and therefore lower blue response, while at the same time forming lower-resistance contacts with the screen-print metal lines, thus leading to a higher fill factor. A long-term inter-batch study of this trend



**Figure 6. Physics-based device model for the PERC cell, which accepts as inputs various detailed cell parameters – such as emitter phosphorus diffusion profile, anti-reflection coating thickness and refractive index, and rear-passivation quality – and calculates both the one-Sun  $I-V$  and spectral response characteristics.**

could aid emitter profile optimization by diffusion furnace process tuning.

### Digital twin

As mentioned in the introduction, a digital twin for the solar cell manufacturing process can be considered to be akin to solar cell device models and fabrication process simulations. Indeed, in this work, as the starting point for the device model part of a digital twin, a detailed solar cell physics model created in Griddler was used, which is a finite-element model and simulation program for solar cells [11–12]. Griddler accepts as inputs various detailed cell parameters, such as emitter dopant profile, anti-reflection coating thickness and its refractive index, and rear-passivation quality (defined by the surface recombination velocity), and calculates both the one-Sun  $I-V$  and spectral response. As shown in Fig. 6, a physics-based

device model was constructed in Griddler, using cell parameters typical of a PERC cell that would yield similar  $I-V$  parameters to those of the median solar cell in the production line batches described earlier.

While the Griddler model is useful for device design work – metallization pattern optimization, modelling the influence of material quality, evaluation of new diffusion recipes, and so on – it cannot interpret production line measurements in real time. Such real-time interpretation is necessary for continuous manufacturing-yield optimization and troubleshooting, unlike during device design. Indeed, as mentioned in Zimmer et al. [4], one of the most important points in modelling is to find the right balance between pragmatism and scientific rigour, as the latter may consume unnecessary computing power and render real-time processing infeasible.

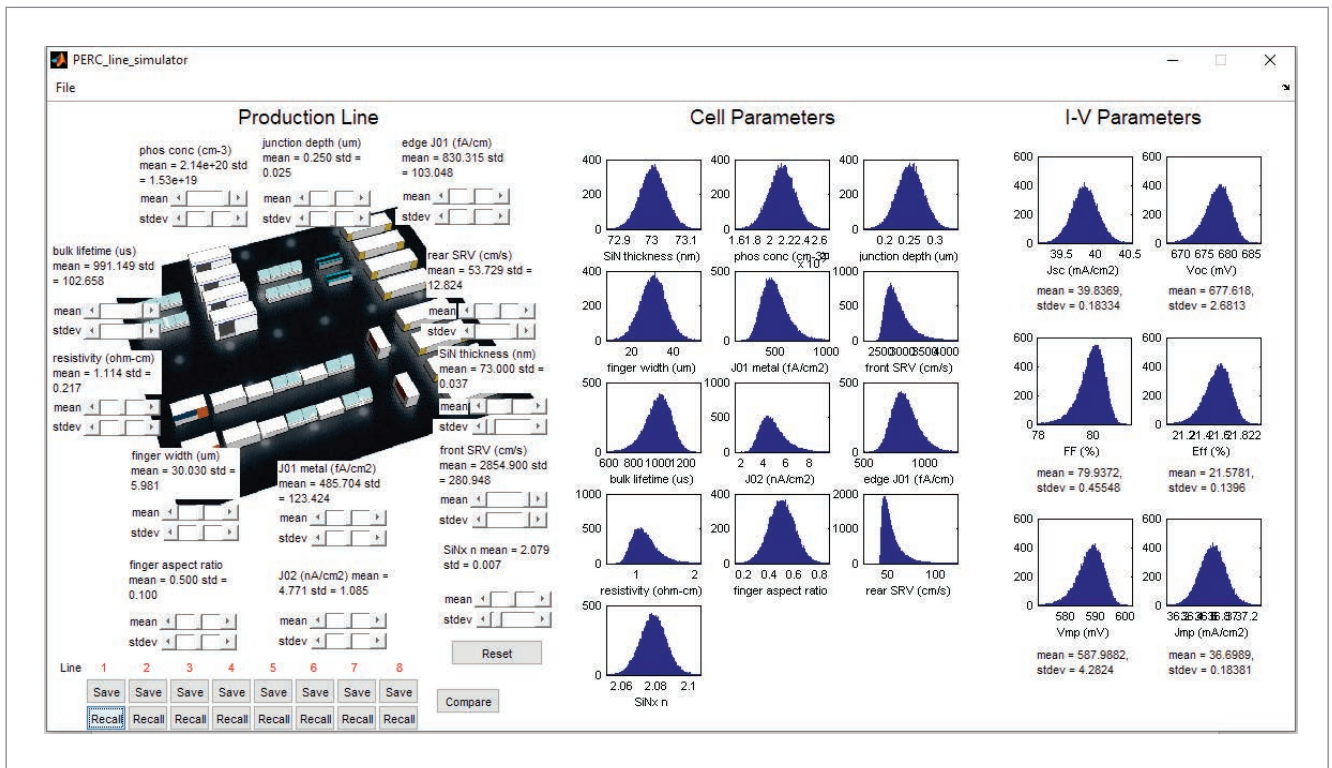


Figure 7. Yield-oriented model for variations in PERC cell fabrication. The model accepts as inputs the statistical distributions of the cell properties, and outputs the statistical distributions of the I–V and spectral response parameters (the latter is not shown in this figure).

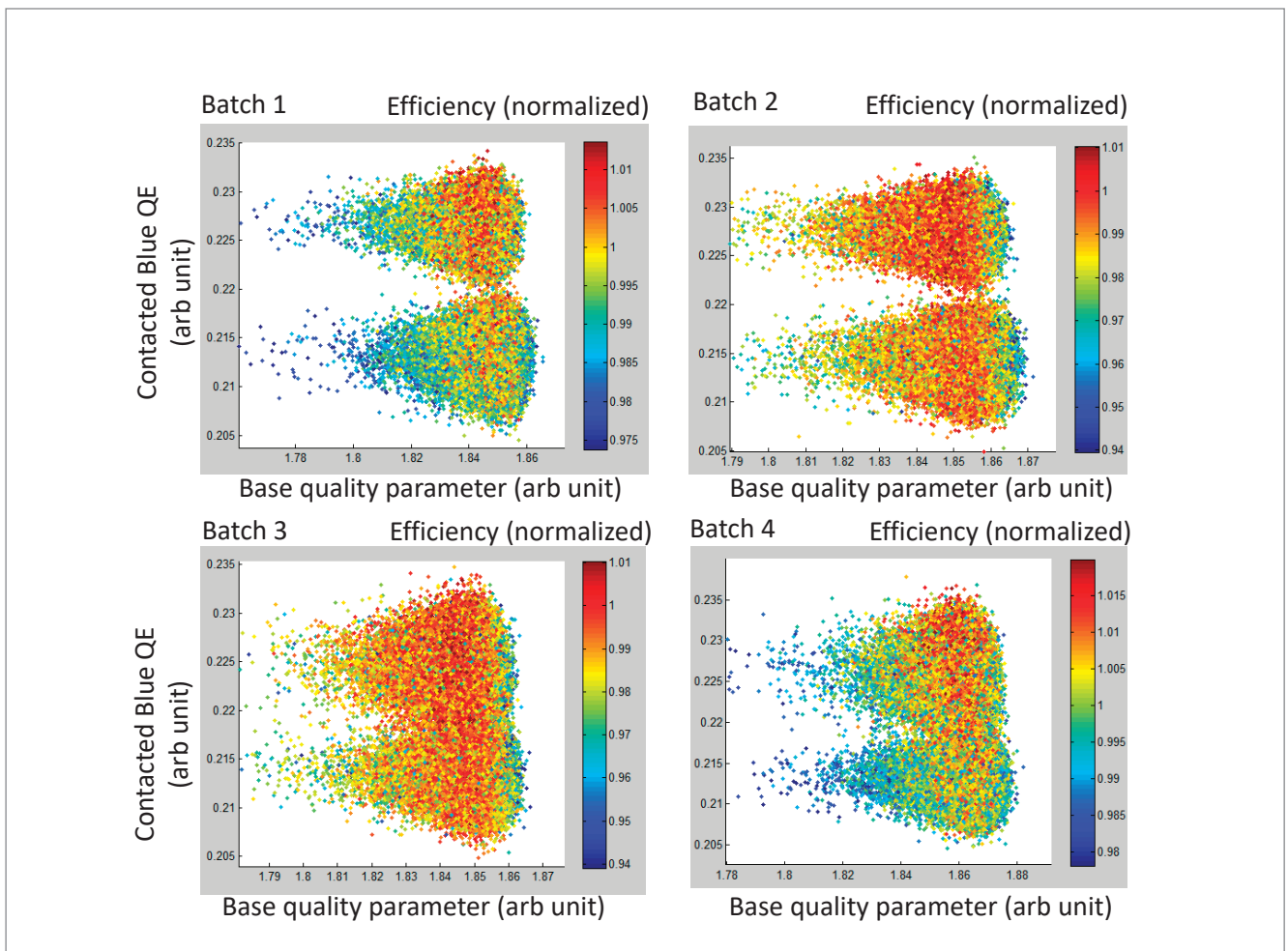


Figure 8. Interpretation of the spectral response data plots in Fig. 4, using the yield-oriented cell model, showing a bimodal distribution for each batch.



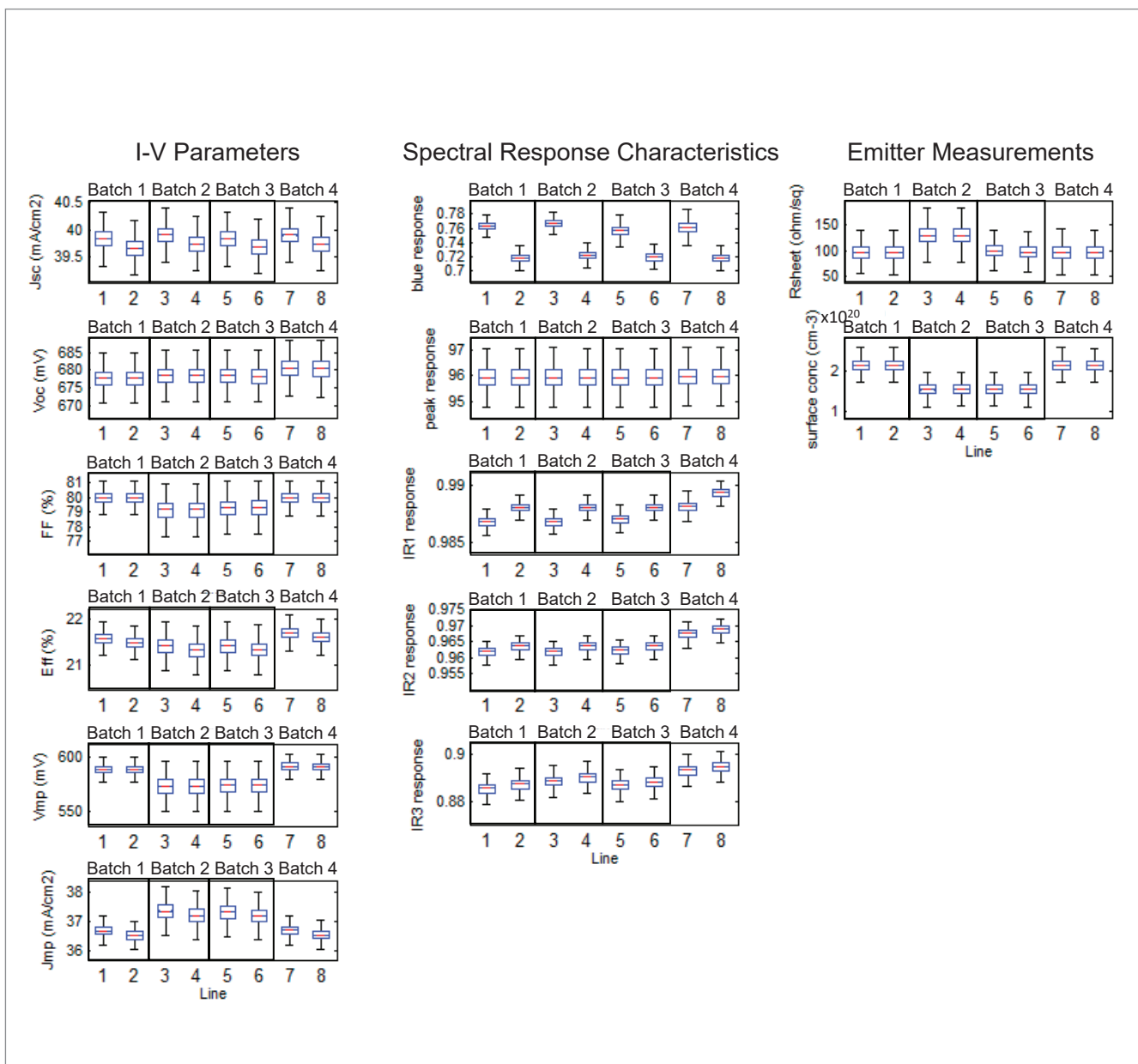
In order to render the Griddler device model suitable for employment as a digital twin, good use is made of the fact that the digital twin is intended for the interpretation of statistical distributions in which the underlying material properties and finished cell parameters are not drastically different from the median for most of the time. Therefore, the focus will be on a simple statistical model that yields the same results as the Griddler model when all input properties are at median

**“The resulting model for the PERC cell accepts as inputs the statistical distributions of the cell properties, and outputs the statistical distributions of the  $I-V$  and spectral response parameters.”**

values, and which performs well at predicting the rates of change in measurement values that are caused by variations in those properties that are relevant to manufacturing yield.

The resulting model for the PERC cell accepts as inputs the statistical distributions of the cell properties, and outputs the statistical distributions of the  $I-V$  and spectral response parameters, as shown in Fig. 7. This model is characterized as *yield oriented*, because it includes the variances (distributions) of input properties and shows the resulting finished cell parameter variances (distributions).

While it is a straightforward matter to model  $I-V$  and spectral response results on the basis of a given set of cell properties and their variations, the



**Figure 9.** Box plots of the various modelled measurement characteristics for the four cell batches, using the yield-oriented model. In addition to  $I-V$  and spectral response parameters, the emitter sheet resistance and surface concentration are also modelled. The ability of the model to predict these latter properties offers increased depth of analysis and enhanced diffusion process control options for production lines that have inline doped layer measurement tools.

accuracy of the inverse approach – finding a set of cell properties that give rise to specific observed finished cell parameters – is prone to severe degradations by measurement noise, confounding factors and model inaccuracies. The model for deriving these properties must be designed to seek solutions within a plausible range of possibilities by setting certain rules, bounds and constraints, the details of which are beyond the scope of this paper. This allows a digital twin to be used to interpret  $I-V$  and spectral response data in a practical manner. As an example, referring to the spectral response data plots in Fig. 4, the model interprets the bimodal nature of the blue response in each batch as arising from corresponding bimodal variations in the anti-reflection coating refractive index. Fig. 8 shows the resulting plots of the spectral responses for the four batches.

Fig. 9 shows box plots of the various modelled  $I-V$  and spectral response parameters for the four cell batches, using the inverse yield-oriented model. Notice that each batch has two distributions of cell parameters, each with a different median for the anti-reflection coating refractive index, in order to reproduce the bimodal nature in the blue response. In addition to  $I-V$  and spectral response parameters, the emitter sheet resistance and surface concentration are also modelled. These latter modelled properties are to illustrate – for production lines equipped with inline emitter layer measurement capabilities [13] – that certain doped layer measurements be interpreted together with end-of-line cell parameters to form a more conclusive picture of the underlying causes of variations seen on the production floor.

### Summary and outlook

This study of volume manufacturing data using four solar cell batches demonstrates the usefulness of inline spectral response measurements in the production line. First, by attributing patterns seen in the  $I-V$  parameters to the blue response or the base quality properties (derived from the red response), one can quickly identify the fabrication processes and their variations that give rise to these patterns, and also assess the impact of the process variations on finished cell efficiency. The spectral response data is often more sensitive than  $I-V$  parameters to variations in fabrication processes, thus potentially aiding pre-emptive maintenance actions or diagnosis of issues in the production line.

A suitably designed digital twin which combines the rigour of a physics model with the practicality of statistical models proves to be useful in performing real-time batch statistics interpretation. With a physics basis, the digital twin is sophisticated enough to consider a multitude of data, such as  $I-V$  and spectral response parameters, and possibly doped layer

measurements in the future. With a statistical basis, it is built to handle high-volume, high-throughput data typically encountered in a solar cell factory. One can envisage the digital twin being used for yield-improving purposes, such as:

1. What-if analysis, e.g. predicting the benefits of employing engineering process control to reduce a certain process-induced cell property variance.
2. Root cause analysis to remedy and prevent out-of-control events.
3. An aide in experimental data interpretation in evolutionary operations to reduce the number of cells required in processing experimental batches.

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**“A suitably designed digital twin which combines the rigour of a physics model with the practicality of statistical models proves to be useful in performing real-time batch statistics interpretation.”**

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### About the Authors



Johnson Wong is the senior physicist at Aurora Solar Technologies. He previously headed the PV characterization group at SERIS, where he created various analytical tools to delineate the factors that contributed to solar cell power loss. He is also the inventor of Griddler, computer programs that apply full-area, two-dimensional finite-element analysis (FEA) to solar cells with arbitrary metallization geometries, and the inventor of Module, a finite-element simulation program for solar panels.



Bernhard Mitchell is a physicist and product engineer with WAVE LABS Solar Metrology Systems GmbH, Germany. He has more than 15 years’ experience in photovoltaics in both academic and business sectors. His work focuses on automated optical inspection systems for silicon and solar cells. He received his Ph.D. from the University of New South Wales, Sydney, Australia in 2013.



Sascha Esefelder is the head of product development at WAVE LABS. He previously worked at Hanwha Q CELLS, where he was responsible for the company-wide calibration chain of cell and module  $I-V$  measurement, as well as the senior expert on  $I-V$  testing. He was engaged in volume data analysis and developed tools for CTM ratio determination and prediction.



Britta Mette has more than 15 years of experience in cell and module  $I-V$  measurement, calibration and characterization. She supervised calibration measurements at Fraunhofer ISE CaLab, after which she developed and implemented calibration

methods at Q CELLS. She then led the electrical characterization team at Calyxo, before joining WAVE LABS as a service and development engineer in 2019.



Budi Tjahjono received his Ph.D. in photovoltaic engineering from UNSW, Australia. He worked as a consultant for PV companies worldwide, before joining Sunrise Global Solar Energy Co. Ltd as their chief technology officer. He is now the group CTO for Sino-American Silicon (SAS) Products Ltd. He has authored/co-authored more than 100 technical papers and is a co-inventor on over 30 international patents.



Dr. Choi Kwan Bum is a research fellow at SERIS. As team leader of the solar cell testing team, he manages the solar cell  $I-V$  measurement activities. His main research interests lie in the use and development of different techniques to perform solar cell characterization, such as improved  $I-V$  measurement methods and luminescence-based lifetime measurement techniques.



Dr. Ho Jian Wei is the head of photovoltaic characterization at SERIS, where he manages the institute’s comprehensive characterization capabilities for solar cells and materials. His research interests include accurate solar cell measurement, quantification of performance losses, and metrology in solar cell manufacturing. He has a B.Eng. from the National University of Singapore (NUS) and received his Ph.D. from the NUS Graduate School of Integrative Sciences and Engineering.



Gordon Deans is the CEO at Aurora Solar Technologies. He has over 35 years of business, engineering and scientific experience in photovoltaics, industrial automation (Omron Adept Technology) and telecommunications (Bell-Northern Research and Nortel Networks). He is a co-designer of Aurora’s measurement technology and holds a number of patents in industrial metrology, process control and telecommunications.

### Enquiries

Johnson Wong  
Aurora Solar Technologies Inc.  
Tel: +1 (778) 241-5000  
Email: [jwong@aurorasolartech.com](mailto:jwong@aurorasolartech.com)



# Bifacial solar cell interconnection technology: A bird's-eye view

Tom Borgers & Jonathan Govaerts, imec – EnergyVille, Genk, Belgium

## Abstract

The recent trends in crystalline Si-based bifacial cell development are having a major impact on interconnection technology. This paper presents an overview of various bifacial interconnection technologies. Starting from traditional tabbing and stringing, the discussion elaborates on developments in multi-wire interconnection technology, and subsequently examines the concept of shingling bifacial cells. The overview concludes with the latest developments in bifacial back-contact cell interconnection technology.

## Introduction

Although bifacial cells implement a few changes at the solar cell level compared with their monofacial counterparts, this is not necessarily the case for the method used to interconnect the cells. Indeed, the most widely adopted way of interconnecting bifacial cells and creating modules is still based on the very traditional approach involving double-sided interconnection of the cells by soldering metal ribbons between the front of one cell and the rear of the neighbouring cell, to create cell strings.

An increase in power resulting from new trends in cell development, however, reveals the limitations of this technology in terms of optical–electrical trade-off for the finger grid. In addition to this evolution, the trends towards thinner cells and heterojunction technology (HJT) severely compromise the temperature budget for the interconnection technology [1]. Addressing this issue, a lower-temperature interconnection technology reduces thermal stress caused by differences in thermal expansion of interconnection materials.

Several technologies are being developed to fulfil these requirements. Apart from drop-in replacements of the soldering compounds in the traditional approach with low-temperature versions or electrically conductive adhesives (ECAs), some very promising options are based on multi-wire interconnection technology, besides

other developments in the area of shingling. A bit further afield, but no less interesting, are some interconnection technologies related to back-contact bifacial cell development.

## Traditional tabbing and stringing of solar cells

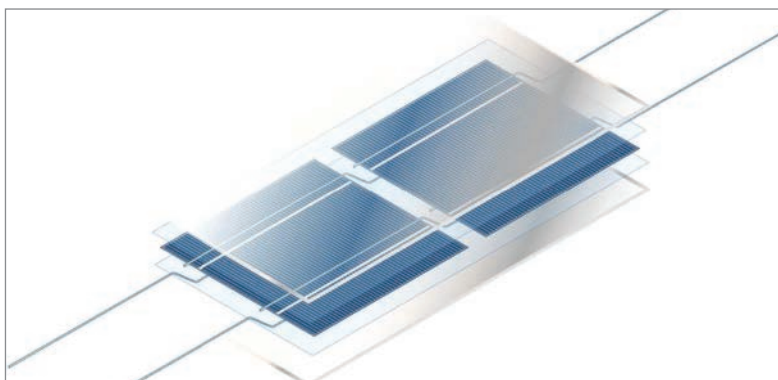
The most traditional technology that is compatible with bifacial cells is based on tabbing and stringing of cells with solder-coated copper ribbons. The generated electrical current is collected through distributed metal fingers across the cell into typically nowadays three to five printed busbars (BBs). By soldering tinned copper ribbons to these busbars between opposite polarities of the cells, the cells are electrically connected in series to form cell strings. The size of these ribbons is a compromise between shadowing on the illuminated surface of the cells and resistive losses.

After the lay-up of the strings – and string interconnection using thick bussing ribbons – between encapsulant sheets and a front and back transparent protective layer, a vacuum lamination step is performed. This method of cell interconnection and module fabrication is very well documented and described by Wohlgemuth and Narayanan [2], among others, and is in many cases applicable to bifacial cells. Fig. 1 shows an exploded schematic view of a cell string in a glass–glass laminate stack.

Currently, 3BB cell designs are widely used, but the share of 4BB designs is on the increase, together with 5BB designs (as also predicted by the ITRPV roadmap [1]). Increasing the number of busbars will reduce the current build-up in the printed fingers of the cell metal grid, as more conductors are distributed over the cell surface crossing the fingers. This leads to lower resistive losses in the fingers, enabling smaller finger cross-sections, and better optical yields and lower metallization costs at the cell level.

High-efficiency grooved interconnection ribbons have been developed to compensate for the shading effect of the ribbons; by adding grooves in the ribbons, more light is scattered and reflected on the glass–air interface of the module, improving internal light capturing (Fig. 2).

Although PV modules are currently excluded from the restrictions imposed by WEEE and RoHS guidelines, the motivation to look at interconnections free of lead and harmful substances is becoming more and more important and is partly driven by the emerging changes in environmental



Source: imec

Figure 1. Exploded view of a standard cell string.

Source: Ulbrich

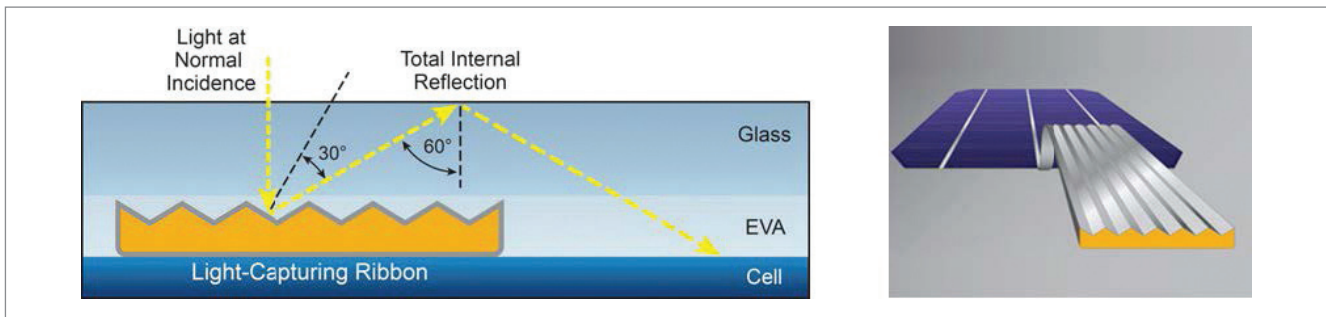


Figure 2. Ulbrich LCR-XP™ light-capturing ribbon.

Source: LG

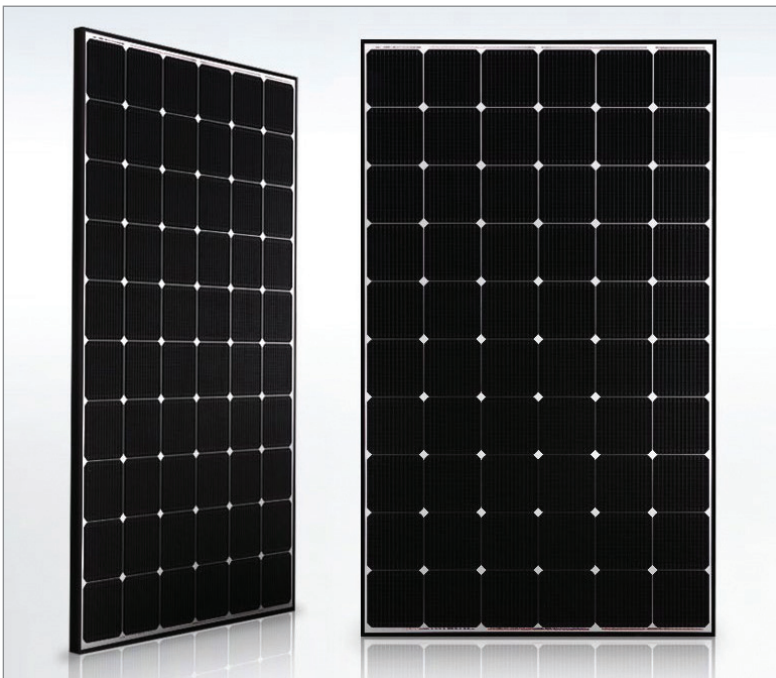


Figure 3. LG NeON module with Schmid multi-busbar (MBB) technology.

**“The motivation to look at interconnections free of lead and harmful substances is becoming more and more important.”**

legislation that could potentially limit the use of lead; after all, in addition to regular updates on substance restrictions, the European Commission will be reviewing the RoHS Directive and is expected to prepare a new proposal by 2021 [3,4].

It is difficult to find an equivalent alternative to this widely used solder; the use of tin- and tin-copper-based solder is limited to applications that are not affected by its higher melting temperature [5]. Low-melting-point solders are often characterized by higher brittleness or poor cell contact wetting characteristics, although Bi-based alloys are also under development [6].

To achieve both objectives – low-temperature and lead-free interconnection – ECAs are also being considered, despite their higher cost. The ECA can be applied as a tape between the ribbon and the cell, or printed on the cell. This technique allows the interconnection of cells with thicknesses below 160µm as a result of better thermal stress management during the interconnection process and thermal cycling [7], and because of the lower bonding temperatures than those encountered with standard solder processes based on tin, tin-lead and tin-copper.

In addition, there have been growing efforts to reduce the lead (and silver) content in the metal

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paste material for the solar cell. Secondly, to meet the temperature-budget restrictions during cell production, low-temperature firing pastes have been developed. However, both these developments also have an impact on the cell interconnection technology.

### Multi-wire technology

#### Multi-wire based on tabbing and stringing

To reduce the resistive losses in the cell fingers, as well as the costs associated with the cell metallization grid, a further evolution of the tabbing-ribbon approach has been developed and implemented by Schmid, making use of stringing busbar-free cells with multiple round wires (Schmid multi-busbar technology; see Fig. 3). This multi-wire interconnection technology has been introduced for double-side contacted cells [8,9]. Since the peel forces achieved on soldered wires are limited for wires directly soldered onto fingers, small solder pads are predicted to increase the soldered area. Nevertheless, as no full busbars are used, a significant reduction in shadowing and/or inactive area is achieved.

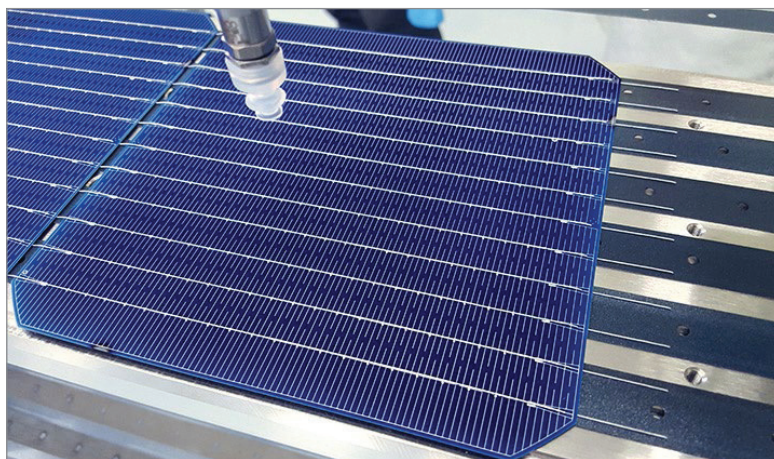
A distributed network of typically 15 round metal wires replace the three to five metal busbars. This eliminates the need for cell busbars, and finger length is drastically reduced, allowing a saving on the finger metallization without increasing ohmic losses. Resulting in reduced shading losses, the round metallic wires can attract a considerable performance advantage, as the round shape of the wires promotes internal light scattering, leading to more internal reflection and thereby improving light harvesting. A 0.33%<sub>abs</sub> higher performance of MBB versus the established H-pattern solar cell has been demonstrated [4].

Schmid's MBB technology for cell tabbing and stringing is similar to traditional tabbing and stringing. To assemble MBB modules, existing module lines can simply be upgraded by replacing the tabber and stringer machine by a dedicated stringer machine (Fig. 4) (provided the cell metallization grid is adjusted accordingly).

#### Multi-wire based on pre-laminated contact sheets

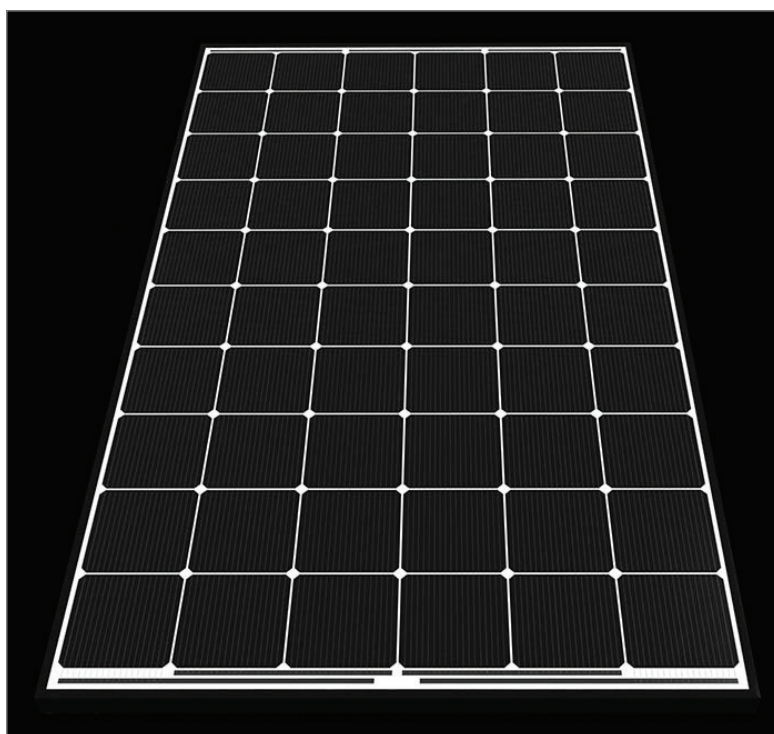
Not too long ago, Meyer Burger introduced its SmartWire Connection Technology (SWCT™), a technology that was first put forward by Day4Energy [10], and further industrialized by Meyer Burger. SWCT combines multiple wires with a polymer foil to create an interconnection foil; the copper wires are coated with a low-melting-point solder (Fig. 5).

The interconnection foils are pre-laminated on busbarless cells to form strings (Fig. 6). After the lay-up between outer protective glass sheets and encapsulant sheets (similarly to the two previously described methods), the stack is laminated in a vacuum laminator. During this lamination process, a low-temperature solder interconnection with the cell



Source: Schmid

Figure 4. Schmid MBB connector machine.



Source: SolarTech

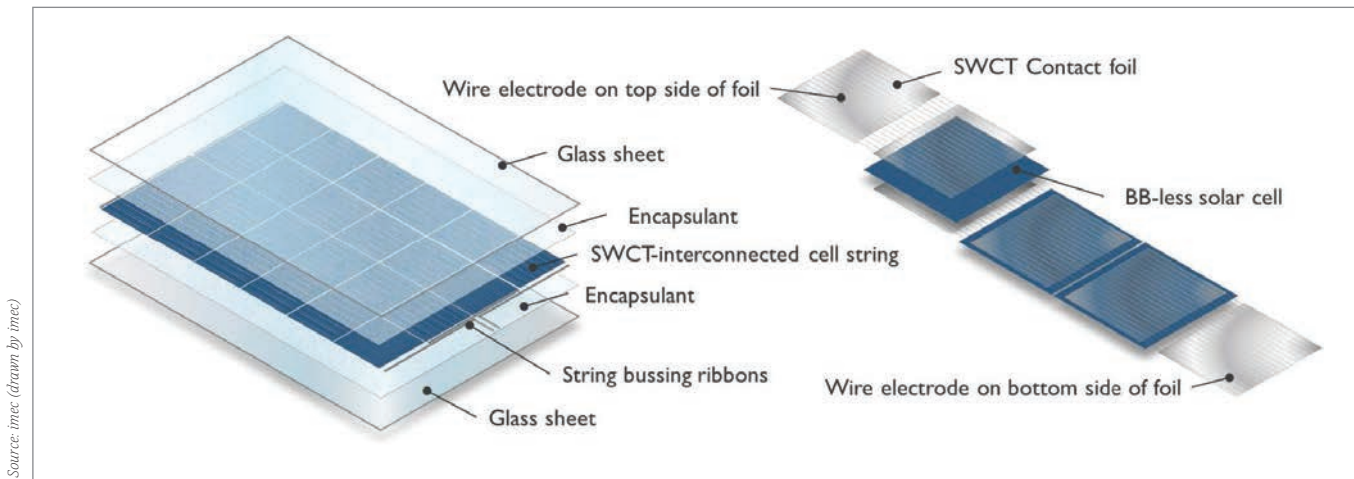
Figure 5. SolarTech Universal EPIQ module based on SWCT technology.

metallization fingers is established: the temperature of the lamination process is sufficient to melt the low-melting-point solder on the copper wires and form an intermetallic connection between the wires and the cell fingers. This temperature budget is also compatible with the process window of the encapsulant material [11].

SWCT technology also benefits from improved light recycling, resulting in better optical and electrical performance, similar to that of the Schmid approach. Additionally, even more wires can be used more easily (typically 18, but up to 24), as the specific (albeit small) contact pads used for the Schmid approach can be avoided. In consequence, more

**“A major advantage of SWCT technology is its compatibility with applications that demand low-temperature interconnection.”**





Source: imec (drawn by imec)

**Figure 6. SWCT cell string build-up.**

redundancy is created in case of cracks or occasional defective solder joints.

A major advantage of SWCT technology is its compatibility with applications that demand low-temperature interconnection – a particularly important factor for heterojunction solar cells.

Moreover, the technology is compatible with cell thicknesses as low as 120µm [12]. As the solder is lead-free, this technology also addresses future RoHS guidelines concerning hazardous substances.

Although Meyer Burger's SWCT deviates significantly from Schmid MBB technology, the required changes to the process flow are in principle confined to an adaptation of the cell stringing process (Fig. 7). Instead of pre-soldering wires on the cell, the stringer in this case pre-laminates the SWCT foils on the cells to create strings. The actual solder interconnection of the wires and fingers is established during the subsequent lamination step, after the lay-up of the pre-laminated strings in the module stack on a lay-up station.

#### Multi-wire based on encapsulant-integrated contact sheets [13,14]

Building further on the evolution towards a low-temperature interconnection technology consisting of multiple wires, imec is developing a system whereby the contact foil is replaced by a woven interconnection sheet combining interconnection wires and encapsulation material (Fig. 8). The idea behind this method is to provide enough encapsulation material in the contact sheet to allow a single lamination step for both lamination and interconnection, without introducing additional materials.

The contact sheet can be made by combining low-temperature solder-coated copper wires, interwoven perpendicularly with encapsulant ribbons (Fig. 9). The metal wires extend over both sides of the woven fabric, and can therefore also be contacted electrically on both sides. Finger contact is enhanced by means of a diagonal progression of an intertwining of the wires along the weave (twill lines).

Because of the weaving process, out-of-plane thermal-stress-relief features are integrated into the sheet, created by the undulating shape of the woven wires (alternately contacting the cell metallization and floating above the cell), which reduces thermomechanical stress generated after soldering or during thermal cycling.



Source: Meyer Burger

**Figure 7. Meyer Burger IBEX SWCT stringer.**



Source: imec

**Figure 8. Example of a 4x4-cell module incorporating imec multi-wire interconnection technology.**

An alternative method for weaving is also in development: here, the wires are directly introduced into an encapsulant sheet through locally implemented cuts according to an optimized cutting pattern for contact and stress relief (Fig. 10).

Because no prior stringing or tabbing of solar cells is required, the lay-up of the module layers can be started immediately by placing the front or back glass in the lay-up station. A contact sheet is placed on the glass, with the contact side facing up (i.e. the side where the wires mostly protrude from the weave). The first (bifacial) cell is laid on this side. A second sheet is laid on the cell, with the first contact-side half facing down. The next cell is laid on the second half of this contact sheet (i.e. the half where the contact side is facing up). This procedure is continued to create cell strings.

Any orientation of the contact sheet relative to the fingers of the cell would be possible, providing that a diagonal orientation of the finger metallization grid on (at least one side of) the cell is foreseen. Strings can therefore be connected by turning contact sheets perpendicularly to a cell string, thereby avoiding the use of end-bussing ribbons between two cell strings. This would considerably reduce the amount of Cu consumption in module manufacturing and avoid time-consuming and production-yield-restricting process steps. The lay-up is schematically illustrated in Fig. 11.

As a final step, a second protective glass sheet is positioned. Depending on the outer borders of the module, no additional encapsulation material is needed. The lay-up can be done in an automated lay-up station, as shown in Fig. 12.

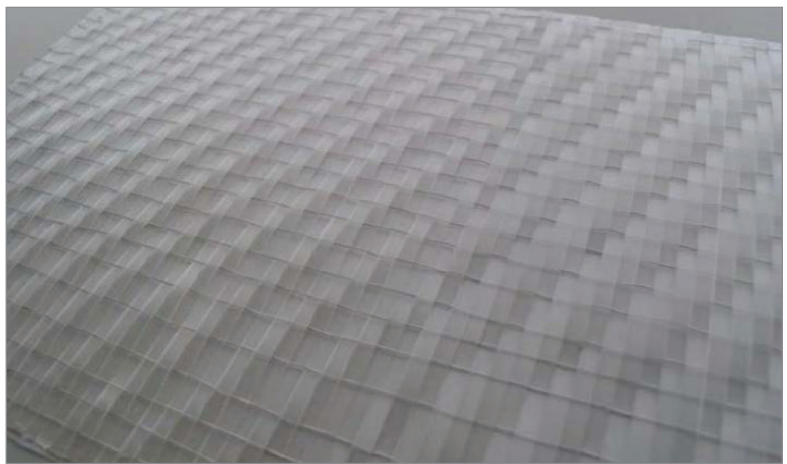
During the subsequent vacuum lamination step, the copper wires are soldered to the metal fingers of the cells. The wires are coated with a lead-free tin-bismuth-based low-melting-point solder.

Initially, the polymer material is not fully liquefied in order to avoid the penetration of encapsulant material between the cell fingers and the wires, which might lead to poor electrical solder contacts. A further increase in temperature causes the thermoplastic encapsulant ribbons to melt, transforming them into a uniform encapsulation layer (Fig. 13).

### Shingling technology

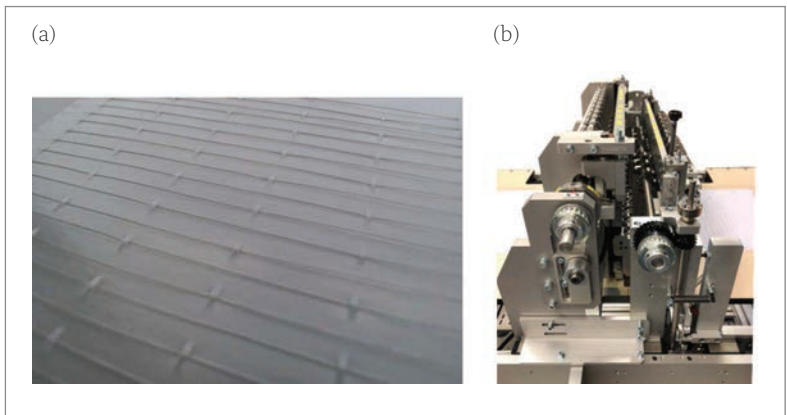
Another, very different, approach for two-side contacted cells that is gaining popularity is based on shingling (Fig. 14). Although an old concept in PV interconnection, it is now rapidly attracting interest in the industry because of some very interesting features. The significant erosion of cell prices has assisted the progress of shingling, the main drivers being an increased active area, a decrease in electrical losses, and a straightforward string assembly.

While current commercial modules typically target monofacial applications and superior aesthetics (rooftop BAPV), there is no reason why shingling could not be employed in a bifacial application with



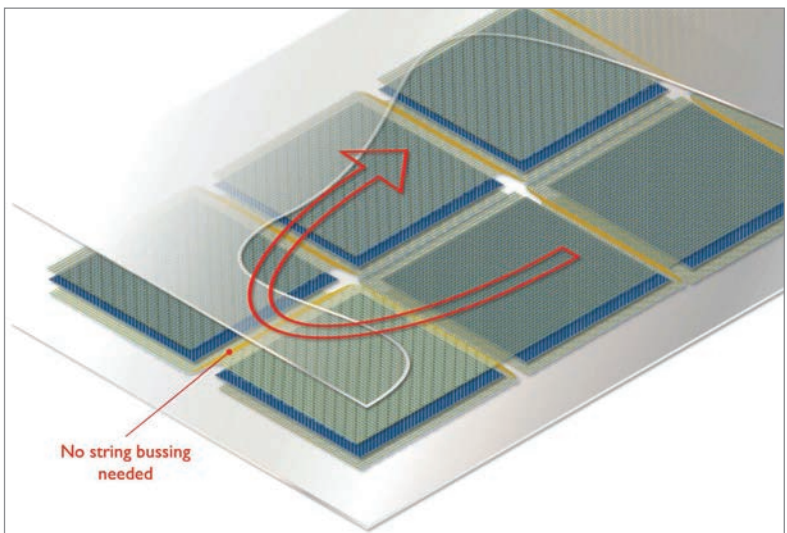
Source: VdS Weaving

Figure 9. Example of a woven interconnection sheet.



Source: IPTE

Figure 10. (a) Finished sheet with locally 'stitched' wires. (b) Process unit of an IPTE proof-of-concept contact sheet processing machine.



Source: imec

Figure 11. Exploded view of multi-wire technology module lay-up, based on encapsulant-integrated contact sheets.

a suitable metal grid design on both sides of the bifacial cells. As cells are cut (typically into five or six strips) to reduce cell metallization grid resistive losses, the current in the cell string is reduced, leading to lower resistive losses. No additional wires or ribbons are needed, thus avoiding shading on the cells, and allowing a very straightforward assembly process. The overlapping method in the shingling approach allows an increased active area of the

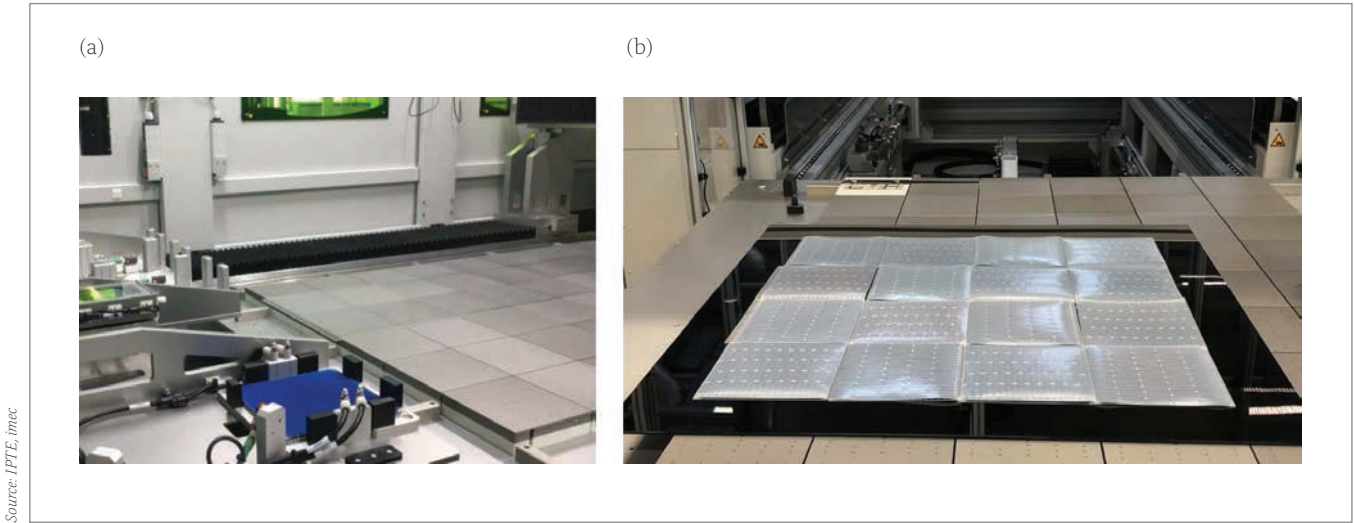


Figure 12. (a) IPTe automated lay-up station. (b) 4x4-cell module after lay-up.

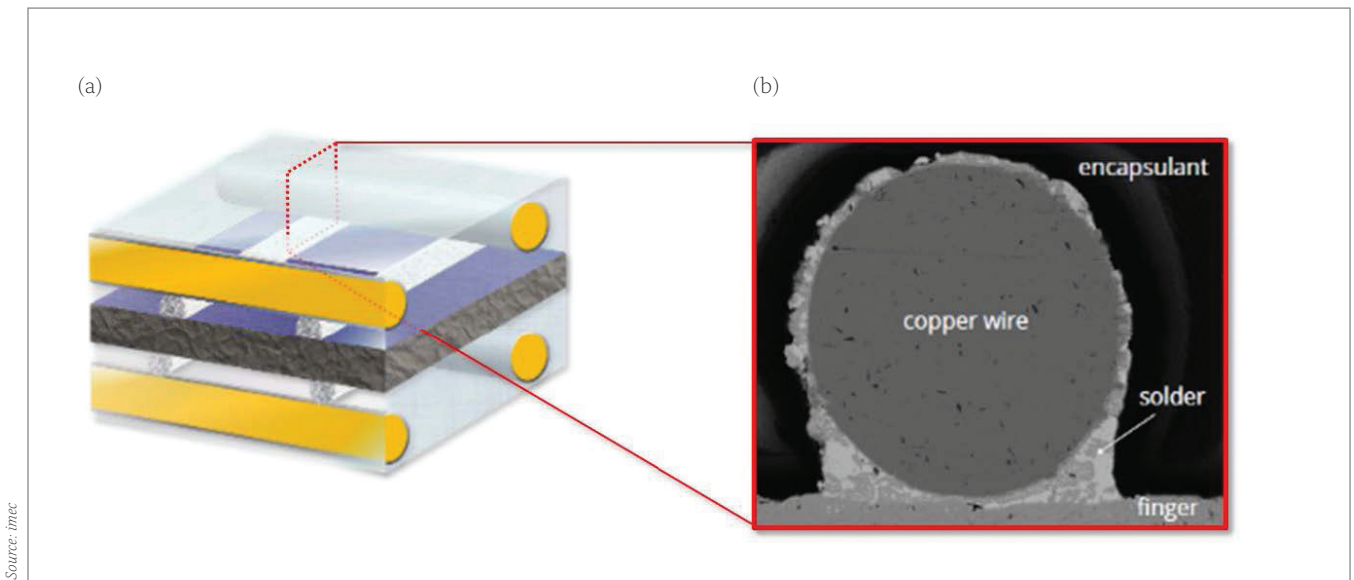


Figure 13. Schematic view (a) and cross-sectional SEM image (b) of a solder joint, created after lamination.

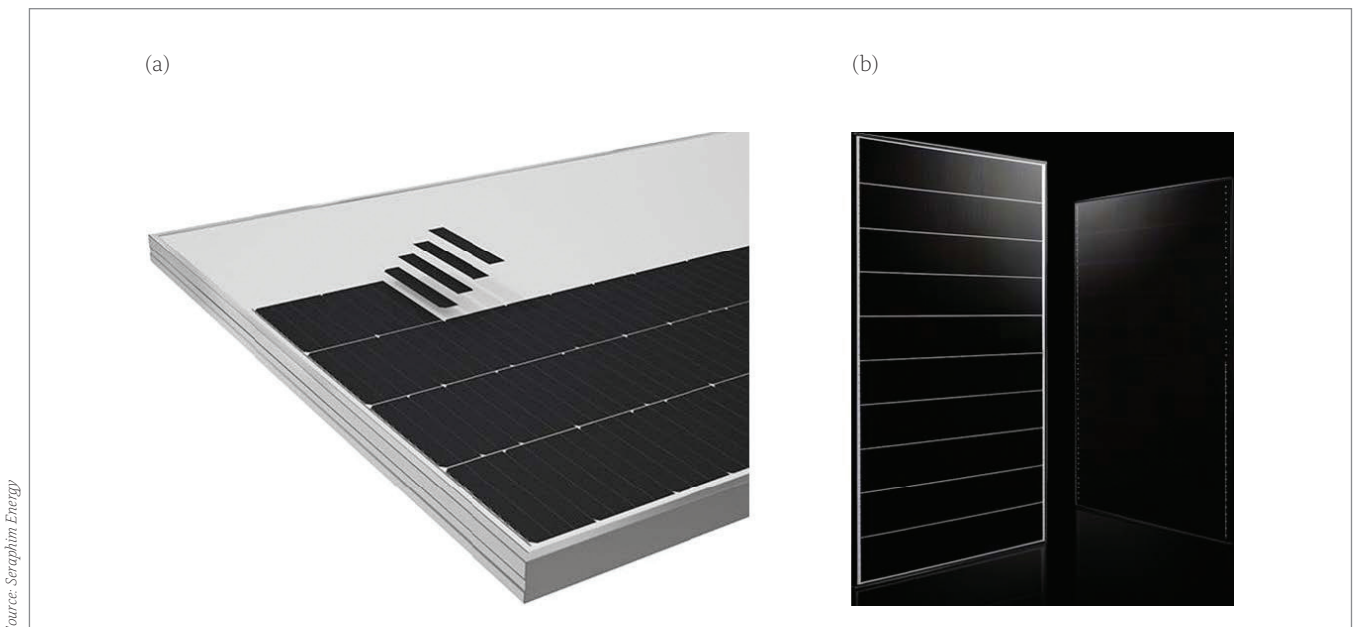


Figure 14. (a) Shingling concept (SunPower). (b) Example of a (monofacial) shingled module (Seraphim Energy).



module, but at the cost of the overlapping Si area that is lost on the bottom cell stripe.

Current shingling technologies use ECA on the collection points of the cell metallization for front-to-back cell interconnection. Although solder paste is also judged to be a possible joint material, additional measures are necessary to limit the shear forces on the solder joint because of the brittle nature of the joint.

The shingling approach leads to lower interconnection losses. As a result of the overlapping of the cells in a string, the only spaces existing between the cells is foreseen to be those between cell rows. A cell-to-module analysis comparison between a standard 6BB module and a shingled-cell module using cells cut into six strips reveals a cell-to-module (CTM) efficiency gain of 1.5–2% for the shingled-cell approach [15].

**Back-contact bifacial interconnection technology?**

Somewhat less obvious is the fact that back-contact cells may also be designed to benefit from bifaciality. Of course, the interconnection and module technology should then also be designed to allow the highest potential. While some technologies, for example the conductive backsheet approach [16], are less suitable in this respect, the more traditional tabbing–stringing-style interconnection, combined with an interdigitated back-side metallization, may still show potential [17], while an edge-stringing approach would require narrower stripes, more along the lines of shingling, to allow narrower fingers (and thus reduced shading). Two concepts in development that are distinctly different from such approaches, but showing significant promise, are discussed below.

**Multi-ribbon**

In an effort to further elaborate its multi-wire and bifacial two-side contacted technology mentioned earlier, imec has also proposed a back-contact version, using a 3D-woven fabric with added functionalities

**“There is no reason why shingling could not be employed in a bifacial application with a suitable metal grid design on both sides of the bifacial cells.”**

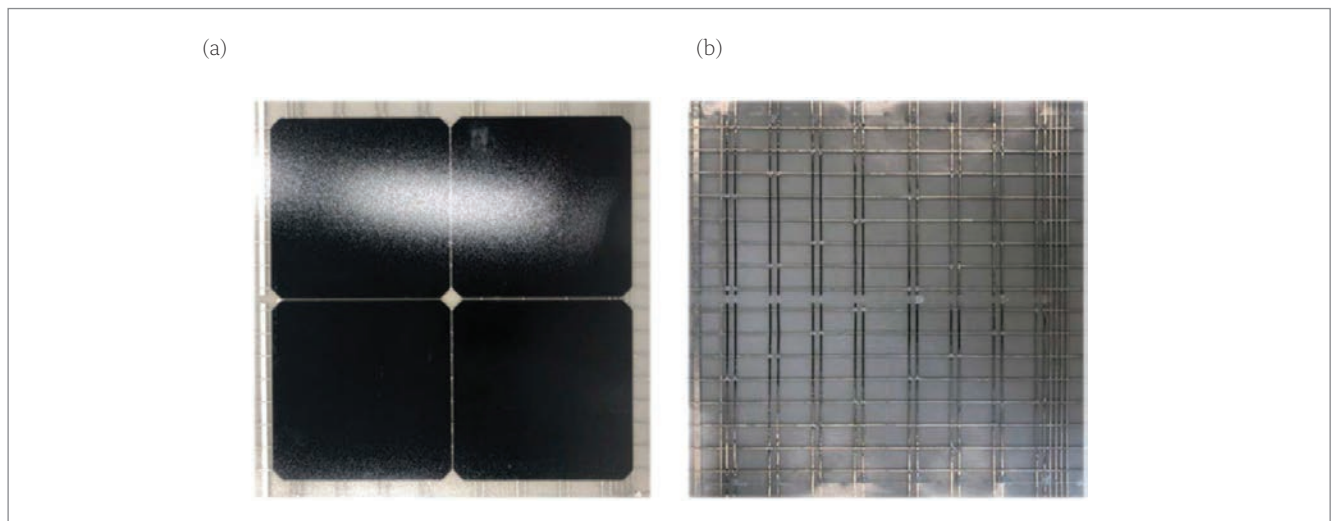
[14,18]. The resulting sheet is an advanced monolithic contact sheet, combining a transparent back-side encapsulant sheet and two layers of metallic ribbons, perpendicularly oriented to each other, and interwoven with the encapsulant sheet (Fig 15).

In addition to its function as a filling encapsulant material during vacuum lamination, the encapsulation material is used as an electrical insulator material between opposing polarities on cells and conductive ribbons, where needed, to avoid shunting. The result after lamination resembles a multi-layer PCB.

The concept itself is based on a hybrid twill-weave-style fabric, a variant of a simple plain weave, and consists of interwoven metal and polymer ribbons. The polymer ribbons are multi-functional: they act as encapsulation material and simultaneously ensure electrical insulation where necessary. The two layers of metal ribbons cross each other according to a specific scheme, determined by the weaving style.

Depending on the location in the 3D fabric, the crossing metal ribbons are either separated by the encapsulant ribbon to allow electrical insulation, or electrically making contact at the locations where the ribbons cross each other on the same side of the encapsulant ribbon to create a floating interweaving interconnection. The metal ribbon layer on the cell contact (bottom) side of the 3D-contact sheet locally protrudes to allow an interconnection with the individual cell fingers of the same polarity on the cell. As such, these ribbons replace the busbar metallization on the cell. The second layer of busbars in the fabric is used to create an electrical connection between subsequent cells in the module for connection in series. The principle is schematically illustrated in Fig. 16.

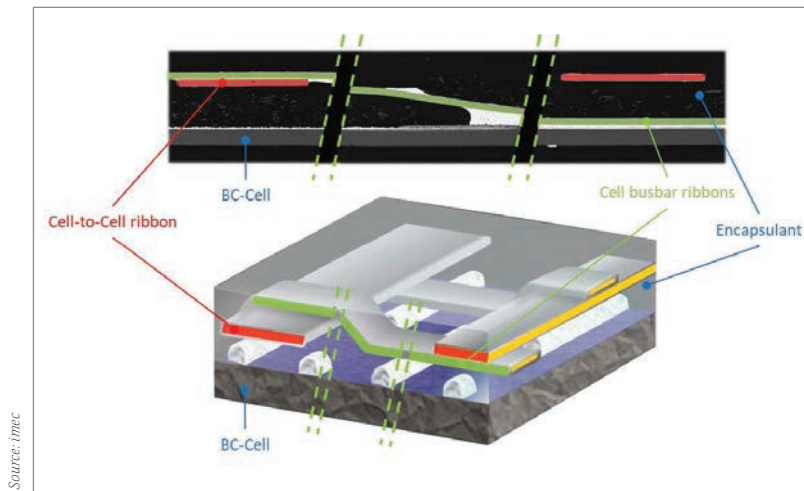
Using only encapsulation material and metal



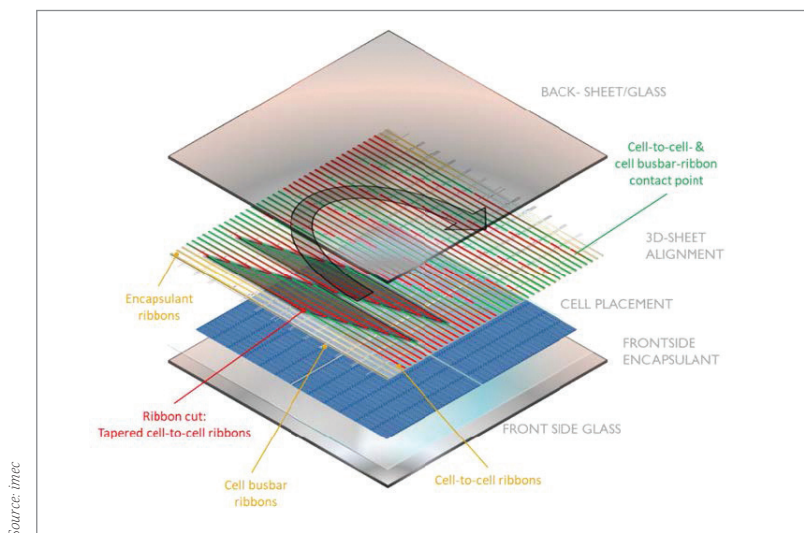
**Figure 15. (a) 3D-sheet-contacted module incorporating four IBC cells. (b) 3D interconnection sheet.**

Source: imec





**Figure 16. 3D drawing of an interconnected cell (bottom), and cross-sectional images of different contact configurations (top).**



**Figure 17. Exploded view of a 3D-fabric-interconnected module incorporating four bifacial IBC cells.**

ribbons, both of which ensure structural integrity, the interconnecting foil also provides enough encapsulation material for good lamination of the cells and backsheet without compromising the electrical separation of the different conductors (Fig. 17).

The double function of the encapsulant, combined with the creative tapered ribbon structure, results in an interesting cost perspective. With the use of a tapered cutting structure of the cell-to-cell busbars, a copper reduction of 37% is achieved for a 60-cell-module with 3D interconnection (with six sub-cell metallization design), compared with standard 5BB modules, while still maintaining a total cell-to-cell interconnection conductor cross section similar to that of a non-tapered ribbon interconnection approach. Eliminating the solder coating on the cell-to-cell busbars results in a total solder-to-copper

**“With the use of a tapered cutting structure of the cell-to-cell busbars, a copper reduction of 37% is achieved for a 60-cell-module with 3D interconnection, compared with standard 5BB modules.”**

ratio equal to that of a 5BB module. Potentially, the cell cost can be reduced, since no additional insulating material on the cell is required because this function is accomplished by the rear-side-integrated encapsulant.

### SWCT approach for back-contact HJT cells

Building further on the SWCT multi-wire technology for bifacial interconnection, Meyer Burger together with CSEM have demonstrated a further development of SWCT technology, adapting it for back-contact interconnection of bifacial heterojunction solar cells (Fig. 18).

By using dedicated wires for both terminals of the back-contact cells, on a single contact foil, along with interruptions of the wires in dedicated locations, a series interconnection can be created between the solar cells in a cell string. As described previously, electrical solder interconnection of the fingers of each polarity with the dedicated wires is created during the subsequent vacuum cycle. This interconnection principle was demonstrated and presented by CSEM at the 2019 EU PVSEC conference [19]. In this case, the insulation between cell fingers and wires of opposing polarities above the cell is realized by printing an additional insulating layer on the cell.

### Conclusion

This overview has highlighted the fact that several bifacial technologies for two-side contacted cells are beginning to win a share of the PV market and that suitable interconnection technologies are being deployed to this end, while offering a glimpse of the possibilities for back-contact cells.

Starting from the transformation of solar cells into bifacial cells, and providing this transformation with suitable interconnection technologies, an important takeaway is that the subsequent implementation must not negate these efforts. In practical and chronological terms, this means that the positioning and dimensioning of bussing ribbons, junction boxes and frames, as well as any support structures or other obstacles that are deployed at the installation site, should be very carefully considered in order to minimize potential shading of the rear side.

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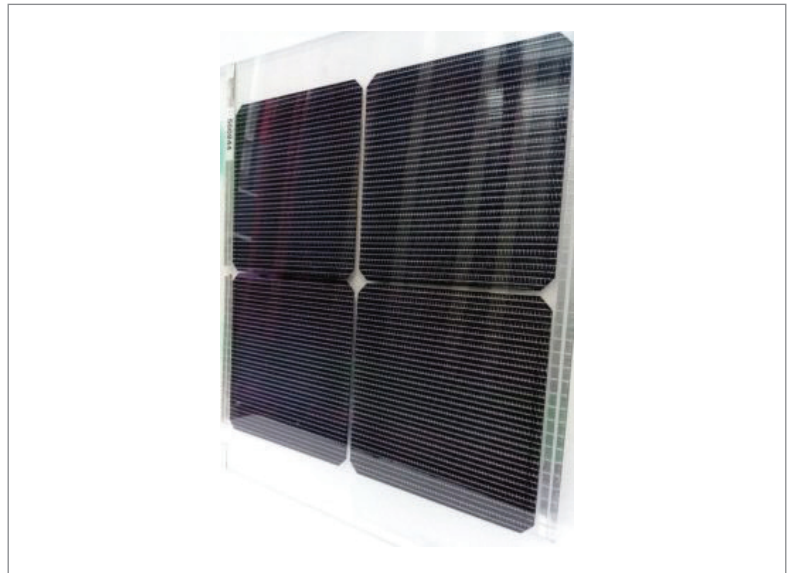
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Source: NextBase

**Figure 18. Module interconnected with dedicated SWCT foils for BC-HJT cells.**

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**About the Authors**



Tom Borgers joined imec in 2000, working on III-V IR detector technologies, flip-chip development for megapixel arrays, and microsystems 3D integration and packaging. Switching to the field of PV in 2008, he became involved in back-contact solar cell interconnection concepts. In 2012 he joined imec's Reliability and Modelling group and is currently working on module interconnection technology with the PV Module Technology team.



Jonathan Govaerts received his Ph.D. from Ghent University, Belgium, in 2009 on packaging and interconnection technology for (flexible) electronics. Since then he has been working with the Solar Cell Technology group at imec, focusing on cell-module integration of silicon solar cells.

**Enquiries**

imec – EnergyVille  
Thor Park 8320  
3600 Genk, Belgium

Email: Tom.Borgers@imec.be  
Website: www.imec-int.com/www.energyville.be

# Potential-induced degradation (PID) of bifacial PV modules incorporating PERC+ technology

Kai Sporleder, Volker Naumann, Stephan Großer, Marko Turek & Christian Hagendorf, Fraunhofer Center for Silicon Photovoltaics CSP, Halle, Germany

## Abstract

The market share of bifacial solar modules is rising, because of the additional power yields of up to 20% per year, which reduce the levelized cost of electricity (LCOE). Many manufacturers have bifacial PV modules in their portfolios, with a majority of them employing bifacial passivated emitter and rear cell (PERC+) technology. In this paper, it is shown from the results of studies that rear-side-related potential-induced degradation (PID) effects can occur in addition to the conventional front-side shunting type (PID-s). Two types of rear-side PID are described – polarization-type degradation (PID-p) and corrosion-type degradation (PID-c) – which can both lead to severe power losses: up to 50% from the rear-side contribution, and around a 10% loss in overall front-side performance. To assess and distinguish these PID effects at an early stage in PV module production, a novel test scheme at the cell level, which combines illumination with high-voltage stress, is proposed. Additionally, a new method is presented for a quantitative evaluation of the rear-side PID on the basis of spectral measurements using LED solar simulators, which is also applicable to outdoor assessment of PV power plants. These new findings on rear-side PID for bifacial PERC+ solar cells thus also require the establishment of a new standardized test routine for solar cells and modules in order to ensure equal test conditions for the quantification of expected power losses in the field.

## Introduction: bifacial PERC technology and new types of degradation

The idea of bifacial solar cells dates back to the 1960s [1] and describes the ability of solar cells or modules to convert light from both the front and the rear side into electrical energy. About 10 years ago, technological concepts were introduced to manufacture and mass produce the passivated emitter and rear cell (PERC) in a bifacial design – the so-called *bifacial PERC*, or *PERC+*. For PERC+ cells, bifaciality is achieved in an adapted cell process, whereby a full-area rear-side metallization is replaced with screen-printed metallization; thus, the rear side becomes translucent [2].

In 2020 bifacial solar cells are predicted to reach a market share of around 20%, and it is envisaged that the market share will grow steadily to around 60% within the next ten years [3]. Bifacial PERC is expected to play a key role, because it can conveniently be produced on existing PERC production lines, since production capacity is

available and is anticipated to grow further [3,4]. With the introduction of PERC+ technology, new degradation mechanisms have come under the spotlight during the last few years. In this paper, the origin and importance of potential-induced degradation (PID) of bifacial PERC solar cells will be explained.

For PERC+ cells, bifaciality is achieved by omitting the full-area metallization at the rear side of the solar cell in favour of local contacts. However, without this metallization there is no electromagnetic shielding of the rear side, making it vulnerable to rear-side PID. This phenomenon has been confirmed by reports in a number of scientific publications in the last two years, on laboratory tests with commercially available bifacial PERC solar cells. Two different rear-side PID mechanisms have so far been distinguished. The first – *PID-p* – is due to a polarization effect at the rear interfaces; this effect results in a non-permanent reduction in the field-effect passivation and is mostly reversible. The second mechanism – *PID-c* – is due to corrosion of the silicon; to a large extent, this is irreversible and results in permanent and localized structural damage to the passivation layers.

## PID: a short history

Depending on the polarity of the voltage and on the type of solar module, potential-induced leakage currents through encapsulating module layers can cause various degradation phenomena. For thin-film modules, it has been known since 2003 that transparent conductive oxides (TCOs) based on tin oxide can corrode under conditions of increased humidity and temperature, if the active layer is at negative potential compared with the grounded module frame [5].

In 2005 a ‘polarization effect’ was reported for solar modules with back-contacted n-type crystalline silicon solar cells [6]. These modules showed a degradation in performance when they were at a positive potential relative to the module frame. It was assumed that the degradation was based on a field effect that causes deterioration of the electrical surface passivation of the solar cells. This is what is referred to as *polarization-type degradation*, or commonly *PID-p*.

Other degradation phenomena relate to corrosion of anti-reflective layers, cell metallization and cell

**“With the introduction of PERC+ technology, new degradation mechanisms have come under the spotlight during the last few years.”**

connectors, which were also found to be associated with leakage currents through electrical potentials in 2010 [7]. Finally, in the same year a substantial reduction in the power output of solar modules with p-type solar cells was reported [8,9]. This significant degradation of solar modules, referred to as *potential-induced degradation*, occurs in PV systems where the solar cells are at a negative potential compared with the module frame. In this case, a strong reduction in the shunt resistance, well below  $1\Omega$ , in the affected solar cells has been observed.

Through microstructural investigations, the degraded performance was able to be attributed to a large number of nanoscopic shunts in the affected solar cells, which was then called *PID-s* [10]. An accelerated, yet realistic, test for PID-s on solar cells was developed at Fraunhofer CSP, and test set-ups for the approach became commercially available, e.g. the PIDcon testing tool by Freiberg Instruments [11].

The drop in the parallel resistance due to the PID-s shunts is, however, reversible. After reducing the potential difference, the solar cells heal slowly; this regeneration can be accelerated by increasing the temperature and applying a reverse voltage [8,12].

In subsequent years, a number of countermeasures against PID-s were developed and implemented in state-of-the-art modules and PV systems. Because of the high relevance to reliability and the increasing number of bifacial crystalline silicon solar modules, current PID research activities are now focusing on the investigation of PID effects on the rear side.

### PID – a new threat for the rear side?

For standard PERC solar cells, there is no risk of PID affecting the rear side. The passivating layers and the silicon are shielded by the fully metallized rear side. However, for PERC+ cells, the electrostatic shielding due to this metallization is missing, and cells are exposed to the same high-voltage conditions on the rear side that are known to cause PID on the front side. Thus, the rear side can also suffer from PID.

The fact that the rear side can be affected by PID was reported in various publications in 2018 and 2019 [13–15]. In these works, p-type mono PERC+ cells were investigated, with the result that similar high-voltage stress conditions on the rear side also led to performance losses because of PID. The performance losses described in these publications ranged from 12% after 40h [13], 10% to 13% [16], and up to 50% [15].

From all these published results, it is clear that PID stress can severely damage the back side of bifacial solar cells, thus reducing the overall cell performance. However, the results are difficult to compare quantitatively, and conclusions regarding yield losses cannot directly be drawn, as the test conditions were not identical: test times between 24h and 136h, temperatures of 50°C, 60° and 85°, and voltages of 1,000V and 1,500V were used in the studies. It is therefore important to identify and specify unique test conditions, i.e. by means of a standardized test procedure for rear-side PID, similar

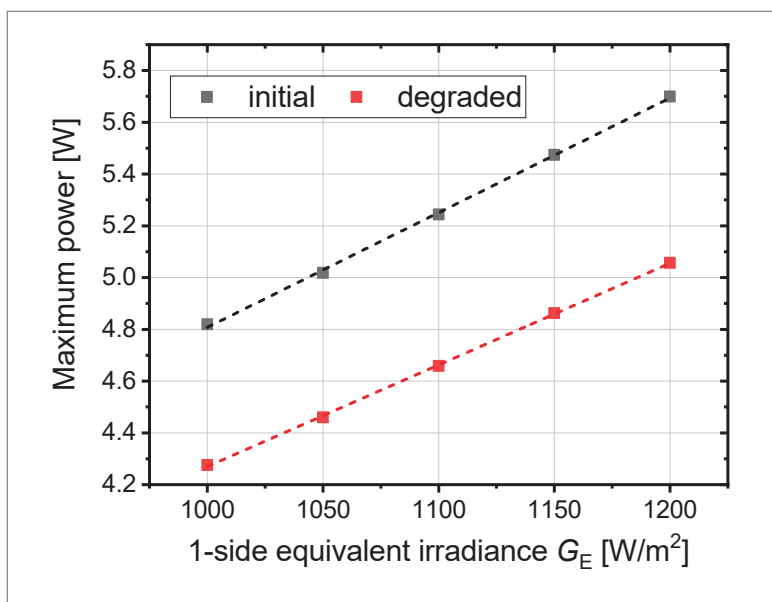


Figure 1. Power ( $P_{max}$ ) of a mini-module as a function of the one-side equivalent irradiance  $G_E$ .

to the existing test norms for front-side PID.

Two different degradation mechanisms are currently known in the scientific literature for PID at the rear side: 1) a degradation due to depolarization of the passivation layers, abbreviated *PID-p*; and 2) a corrosive PID type, referred to as *PID-c*.

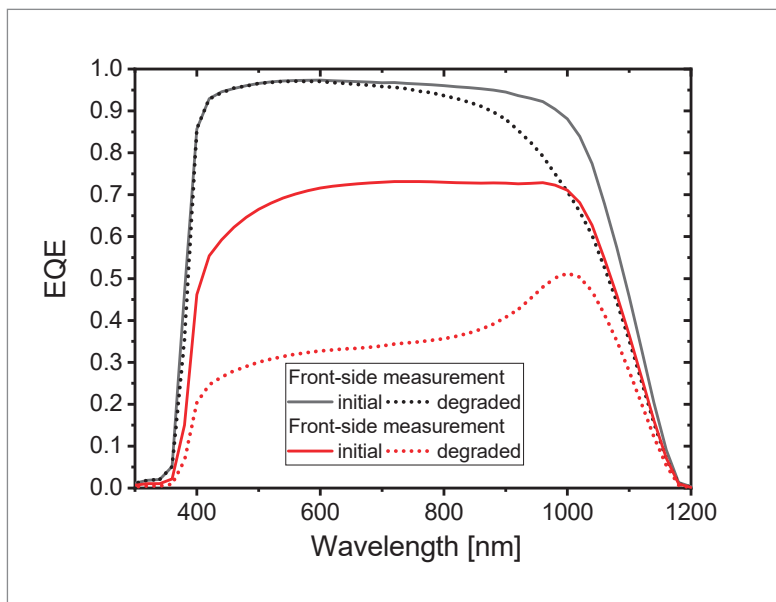
PID-p of the polarization type assumes that the field-effect passivation of the  $AlO_x$  layer is depolarized by charge compensation because of an accumulation of positively charged ions in the rear-side  $AlO_x$  passivation layer [13]. This interpretation was developed according to the findings of Swanson et al. [6].

The second currently known PID effect is due to corrosion of the Si below the passivating  $AlO_x$  and  $SiN_y$  layers. By analysing just the  $I-V$  curves, it is not possible to distinguish whether the high potential causes just a depolarization or an irreversible corrosion. This differentiation can be accomplished by using spatially resolved methods: microscopic regions of up to  $2\mu m$  in size showing corrosion can be detected by means of laser beam induced current (LBIC) or electron beam induced current (EBIC) methods [14].

Another fundamental difference between PID-p and PID-c can be related to the recovery behaviour of degraded cells or modules under light exposure. Alternatively, the high-voltage stress test can be performed under simultaneous illumination. If the degradation is caused by corrosion (PID-c), the performance of the stressed sample cannot be recovered by illumination. However, in the case of PID-p a complete healing can be achieved [17,18]. More importantly, if the PID test is performed

**“PERC+ cells are exposed to the same high-voltage conditions on the rear side that are known to cause PID on the front side.”**





**Figure 2. External quantum efficiency (EQE) of a bifacial PERC one-cell module. Compared with the initial state (solid lines), the measurements in the degraded state (dotted lines) have reduced EQE signals in certain wavelength ranges as a result of PID.**

### “Spectral features serve as a criterion for distinguishing rear-side PID from front-side PID.”

under simultaneous illumination, PID-p can even be suppressed. This implies that for a PV park, polarization-type degradation (PID-p) is probably

not critical, assuming that a rear-side light intensity exceeding  $10\text{W/m}^2$  is sufficient to suppress PID-p [17]. This is not the case, however, for corrosion-type degradation (PID-c), which causes damage to the cells in field conditions.

In the light of these findings, an accelerated PID test is proposed for the rear side, whereby illumination together with the high-voltage stress is simultaneously applied in the test set-up. Furthermore, to test for PID at the rear side a new standard ought to be developed which includes these combined test conditions. On the basis of the results obtained at Fraunhofer CSP, the authors propose that the standard should feature a high-voltage stress of 1,500V at elevated temperatures around  $85^\circ\text{C}$ , combined with an illumination of 1–5% of normal test intensity.

As an example, Fig. 1 shows the power of a mini-module as a function of the one-side equivalent irradiance  $G_E$ . The measurements were carried out before and after a PID test. In the test configuration, a voltage of 1kV was applied across the full-area metallic electrode on the back of the module opposite the grounded solar cell. The front of the module was also connected to the ground. In this special configuration, a single-side PID assessment is possible in such a way that shunting-type PID (PID-s) of the front side is avoided. Power losses of around 11% under standard test conditions are thus caused by rear-side PID as a result of the degradation of the rear side only.



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- Voltage:  $\pm 1.5\text{ kV}$
- No climate chamber necessary
- Easy to use bench top device

#### Applications

- PID detection at cell level
- Research, Production & Quality Control of PERC, AL-BSF, PERC+, bifacial PERC, PERT, PERL and IBC solar cells



Developed in cooperation with:  **Fraunhofer**  
CSP

### Classification and quantification of different types of PID

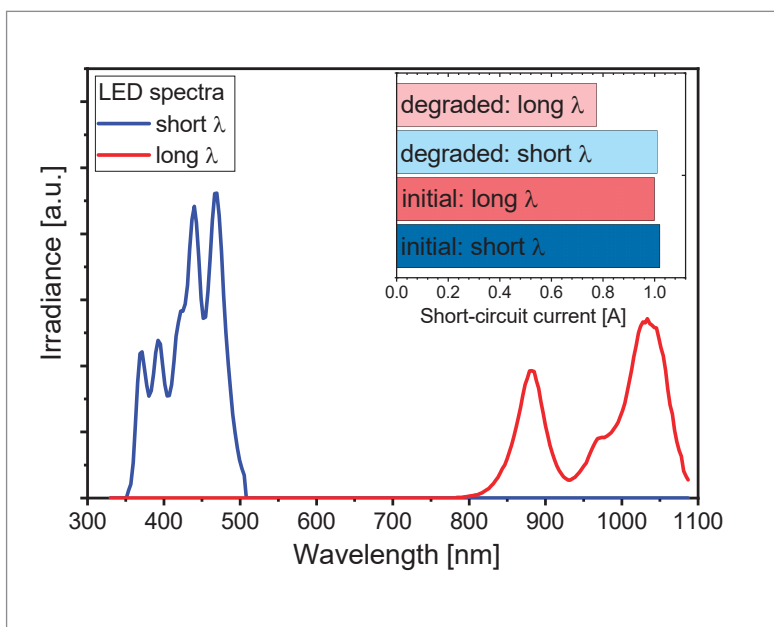
The major impact of all types of PID in an advanced stage is the reduced power of the solar cells and modules. During quality assurance tests or product development, the power under standard test conditions is typically determined using solar simulators. As the cells within a single module are usually not affected equally by PID – visible, for example, as a checkerboard pattern in luminescence imaging – it is essential that the light field from the solar simulators used is of high lateral uniformity for a reliable power analysis. Reliability can be ensured, for example, by the use of the Fraunhofer CSP uniformity test sensor, which is made of identical materials to those of the modules under consideration, but with all cells individually connected to an integrated measurement electronics. This allows a simple, fast and accurate assessment of the lateral properties of the solar simulator light field.

Nevertheless, while conventional measurement systems reliably yield the power losses after a stress test, it is not possible to identify the specific type of PID. In particular, for a failure identification and optimization of the production process, it is of critical importance whether the front side or the rear side of the solar cell is affected.

It has been shown that the two types of PID, PID-p and PID-c, exhibit a distinct characteristic change in the spectral response of the cell (see Fig. 2). A spectrally resolved external quantum efficiency (EQE) analysis was carried out for the one-cell module, both in the initial state and after the PID stress test. In the degraded state, an increase in carrier recombination is observed for wavelengths above 700nm when measured with the sunny side up. This is reflected in a reduced EQE signal at larger wavelengths. While the absorption of the incident light depends on the wavelength, electron hole pairs are still created throughout the entire depth of the cell, including the degraded rear surface of the cell.

With the module flipped over, i.e. the rear side is now the sunny side during the EQE measurement, PID-related carrier recombination dominates the near-surface regions and thus leads to a characteristic and severe drop at wavelengths below 900nm. A peak in the rear-side EQE in the 900 to 1,100nm wavelength range indicates that an increase in bulk recombination due to rear-side PID is negligible. These spectral features are characteristic for rear-side degradation and thus serve as a criterion for distinguishing rear-side PID from front-side PID.

Using a recently developed rapid quantum efficiency test based on LED solar simulators [19], this classification and distinction of the PID type can easily be combined with the power test under standard test conditions. Furthermore, the spectral information provided by a more advanced test set-up using LED solar simulators results in far more reliable estimation of yield than a single



**Figure 3. Two spectra of an LED solar simulator for rapid rear-side PID testing, representing the short-wavelength range (blue line) and the long-wavelength range (red line). The inlay shows the resulting short-circuit current of a bifacial one-cell module for the two indicated spectra in the initial and degraded states. While there is almost no change in the current for the short-wavelength spectrum, the long-wavelength spectrum clearly shows the rear-side degradation.**



**Figure 4. LED-based solar simulator at the Fraunhofer CSP PV park. Using different coloured LEDs, an initial diagnosis of the type of PID can be made.**

**“The new types of PID associated with PERC+ solar cells need to be tested using an adapted new test standard which includes the simultaneous application of illumination and high-voltage stress.”**

measurement as described in the test norm for measurements under standard test conditions.

In a simplified version, the usage of LED solar simulators allows the illumination to be controlled using either short or long wavelengths only. As can be seen from the inlay in Fig. 3, the short-circuit current  $I_{sc}$  of a module is significantly reduced by about 20% for long-wavelength illumination; on

the other hand, the  $I_{sc}$  is not reduced when using short wavelengths. Thus, this simplified version of a spectral measurement can clearly reflect the increase in carrier recombination at the rear surface of the solar cell due to rear-side PID.

The indoor-testing schemes applicable to quality assurance or to R&D can also be transferred to a quick outdoor assessment. As the first outdoor LED solar simulators are now commercially available, similar measurement approaches can be implemented in a field inspection of PV modules, resulting in a more defined failure classification and in the ability to distinguish between rear-side PID and front-side PID (see Fig. 4).

### Conclusions

With bifacial PERC, or PERC+, technologies, new degradation mechanisms related to high-voltage stress of the cell rear side can occur. There are two PID effects which can affect the rear side of a bifacial solar cell and reduce a PV module's power in a significant way. The first of these, polarization-type PID (PID-p), is reversible and can be suppressed by illuminating the solar cells; thus, the implications for field operation are less significant. The second, corrosive-type PID (PID-c), leads to permanent structural damage of the passivation layer of the solar cell; it is not reversible and also occurs under illumination. The new types of PID associated with PERC+ solar cells need to be tested using an adapted

new test standard which includes the simultaneous application of illumination and high-voltage stress.

All three PID types – PID-s, PID-p and PID-c – result in a power loss of the cell. In order to distinguish between the various types, spectral measurements are necessary, which – in a simplified version – can even be performed using LED solar simulators. As PERC+ technology becomes more widespread, it is essential that new test schemes are established, i.e. high voltage combined with illumination, new test devices, and adapted characterization tools and procedures, in order to classify and quantify the PID effects.

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**About the Authors**



Kai Sporleder studied medical physics at Martin Luther University Halle-Wittenberg, Germany. In 2015 he joined Fraunhofer CSP, focusing on defect diagnostics and electrical characterization of silicon solar cells.

Since 2017 he has been carrying out research work for his Ph.D. on potential-induced degradation at the rear side of bifacial solar cells.



Dr. Volker Naumann studied physics in Halle, Germany. He began working at Fraunhofer CSP in 2008, and has been involved in research on diagnostics and microstructure analysis since 2010. He received his Ph.D. in physics, with a thesis on PID root cause analyses, from Martin Luther University Halle-Wittenberg in 2014. He is currently a researcher in the Diagnostics and Metrology group at Fraunhofer CSP, where he leads the Surface and Layer Characterization team.



Dr. Stephan Großer studied physics and received his Ph.D. in the field of surface science from the Martin Luther University Halle-Wittenberg in 2008. He joined the Fraunhofer CSP in 2011, where he leads a team that focuses on microstructure characterization of materials and devices. His research interests lie, in particular, in the localization, target preparation and root cause analysis of defects and contaminations.



Dr. Marko Turek studied physics at Dresden University, and received his Ph.D. in the field of condensed matter theory from the University of Regensburg. At Fraunhofer CSP he leads the team involved in the electrical characterization of solar cells and modules. His research focuses on the loss analysis of solar cells, advanced characterization methods, and the development of new test methods and devices.



Dr. Christian Hagendorf is the head of the Diagnostics and Metrology research group at Fraunhofer CSP. He obtained his Ph.D. at Martin Luther University Halle-Wittenberg in the field of surface and interface analysis of semiconductor materials. Joining Fraunhofer CSP in 2007, he established a research group which focuses on defect diagnostics and metrology in crystalline and thin-film PV.

**Enquiries**

Kai Sporleder  
Diagnostics and Metrology  
Fraunhofer Center for Silicon Photovoltaics CSP  
Otto-Eissfeldt-Strasse 12  
06120 Halle, Germany

Tel: +49 345 5589-5070  
Email: kai.sporleder@csp.fraunhofer.de



# Thermal laser separation technology for optimized half-cell module performance

Michael Grimm, 3D-Micromac AG, Chemnitz, Germany

## Abstract

Half-cell modules are gaining an increasing market share because of their potential for increasing module power without requiring any changes to cell technology. However, it has emerged that different cell separation technologies can produce similar electrical performances of the half cells, yet lead to an entirely different mechanical behaviour of the cells. An electrical evaluation showed minor electrical power losses for the half cells, leading to an efficiency reduction of less than 1%<sub>rel.</sub> As regards mechanical behaviour, the mechanical strength at the solar cell and module laminate levels was evaluated for thermal laser separation (TLS) and laser scribing with cleaving (LSC) cutting technologies on multicrystalline silicon Al-BSF solar cells. It was possible to systematically show that mechanical defects found at the cell level could also be seen at the module level. More precisely, the mechanical strength in the case of the LSC batch decreased by 35% at the cell level and 23% at the module level. The TLS process, in contrast, did not have an effect on strength at the cell level or the module laminate level. Additionally, the origin of fracture was found to be at the edge for the laser batch and on the rear-side pads for the full cells and TLS-cut cells.

## Introduction

The key characteristics of solar cells for half-cell modules are their electrical performance parameters and their mechanical strength. In recent years, there has been significant progress in limiting the electrical losses due to the cell separation process, so that a significant power gain of around 5% can be achieved for half-cell modules [1–3]. On the other hand, the mechanical strength of solar cells is a key parameter with regard to ensuring high yield during the manufacturing of solar cells and modules [4]. Each critical incident of mechanical damage during solar cell production will affect any subsequent process and application, because it will always be the most critical defect that will lead to failure. Furthermore, a reduction in mechanical cell strength leads to increased breakage rates of cells during operation in the field.

In this paper, a systematic study is presented where damage within the solar cell was investigated through fracture tests of single solar cells and of the module or module laminate

(without frame) incorporating the same cells. Thus, the approach allows the mechanical damage at any stage of the production to be quantified. The mechanical tests were accompanied by the determination of the electrical performance of the half cells in order to ensure that either process yields minimal electrical losses due to cell separation. As a result, it was found that different cell separation processes can lead to similar electrical performance parameters of the half cells, while yielding very different levels of mechanical strength.

## Material and methods

In the work reported here, commercially available multicrystalline silicon Al-BSF solar cells with four busbars were investigated. The cells were cut into half, either by thermal laser separation (TLS) [5] or by laser scribing with cleaving (LSC). The TLS process was used on the sunny side of the cells, whereas for the LSC process a laser scribe was used on the back side of the cells and cleaved by applying tensile stress, also to the back side of the cells, because of bending. The module laminates were produced using typical standard materials (full-tempered 4mm glass front; Sky S88 EVA encapsulant; Akalight ECS 675 PPE backsheets; Bruker-Spaleck 1.2mm × 0.2mm Solar Tab interconnector). The cell interconnection was performed using a fully automatic tabber–stringer, and lamination was carried out on industrial equipment with process parameters similar to those for industrial processes.

## Electrical characterization

In order to quantify the electrical losses induced by the half-cell processes, 30 full cells from each batch were electrically characterized by measuring their illuminated current–voltage curves. Each batch was then split into five reference cells and 25 cells, which were further separated into half cells. In a second measurement sequence, the five reference cells and the 50 half cells were measured once more. The electrical measurements were taken using the LOANA loss analysis tool by pv-tools GmbH. The current–voltage characterization was performed under standard test conditions, and the most relevant electrical performance parameters were obtained by

**“The key characteristics of solar cells for half-cell modules are their electrical performance parameters and their mechanical strength.”**

applying a two-diode model to the measured data. As a cross check for measurement uncertainty, the data for the five reference cells from each batch was compared for the two measurement runs.

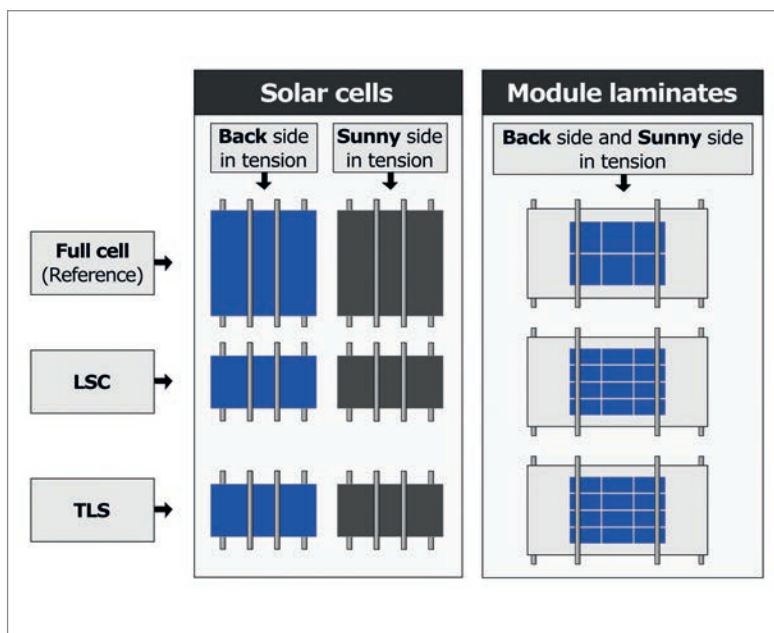
### Mechanical characterization

The mechanical strength was determined by means of four-point bending fracture tests in cell and module laminate configurations (see Fig. 1). In four-point bending tests, the samples are supported by two rolls at the bottom and loaded by two rolls at the top, thus creating a fairly constant stress field between the inner rolls. The solar cell tests were performed on a universal testing machine (ZWICK 005), using a load cell of 500N in accordance with DIN SPEC 91351 [6]. For each test, 50 samples were loaded with the rollers parallel to the busbars in the four-point bending set-up until cell breakage occurred for all three batches: 1) full cell without separation; 2) half cell after LSC; and 3) half cell after TLS. Each batch was divided into two tests, with the sunny side or the back side in tension.

The four-point bending configurations used in this work had an outer span (outer rollers) of 80mm and inner load span (inner rollers) of 40mm; the rollers are made of steel with a diameter of 10mm. For better contact behaviour and reduced friction, PTFE foils were placed between the rollers and the cells. A finite-element model was used to calculate the fracture stresses in the four-point bending experiment, taking account of nonlinearities during the bending test [7]. Fracture stresses were evaluated using the Weibull distribution [8,9]. Furthermore, a reduced mechanical cell model was used to capture just the behaviour of the silicon layer, because the metallization does not have a major influence on the stiffness or bending stresses in the four-point bending test for silicon [10]. The metallization, however, governs the defect structure within the silicon layer. For the evaluation of all cells, considering the effect that size has on strength, the effective area was set to  $A_{eff} = 9,116\text{mm}^2$ ; this has also been used in previous publications [11] and allows meaningful comparisons to be made.

The method for in-laminate strength testing is described in detail in Sander et al. [12]. The experimental set-up represents a four-point bending load. With the use of an electroluminescence (EL) camera (Sensovation coolSamBa HR-830), all the cells between the two load rolls can be inspected during the test. The set-up is mounted on a universal testing machine (Zwick Z400). Deflection of the middle of the test sample is measured by a displacement sensor, and load is measured by a 10kN load cell.

All tests were performed at room temperature. The load was increased in steps of 10N and remained constant for 60 sec while the EL image was taken. The test was continued until all cells



**Figure 1. Overview of all the mechanical tests for all the batches (full cell, LSC and TLS), and both configurations (solar cells and module laminates).**

were broken or a specified maximum load was reached. As a result of the procedure, load time data and EL images for every load step were available. Crack occurrences can be identified from the load displacement curve when the load decreases abruptly because of a reduction in stiffness of the sample due to a cracked cell. The cracked cell and the fracture origin are identified from the EL images.

In the case of full cells, six module laminates were produced, each incorporating six cells. For the half cells, three module laminates with 12 half cells each were produced for the LSC and TLS batches. In total, it was possible to obtain 36 fracture occurrences for each batch. With regard to the testing of the module laminates, the back and front sides of the cells are in tension. The fracture stresses were calculated by finite-element models and evaluated by means of the Weibull distribution. Some cracks were induced during the lamination process, but these were excluded from the evaluation.

## Results

### Electrical

The results of the electrical tests reveal minor electrical losses caused by the half-cell processes (see Fig. 2). The power of the half cells is decreased by about 0.5 to 0.8%, which is mainly because of a reduction in the fill factor (see Fig. 2(b)). However, this fill factor reduction cannot be attributed to

**“Both cell separation processes lead to fairly high-quality half cells with regard to electrical performance.”**

**"In the case of the TLS batch, no significant change in mechanical strength could be observed for the sunny side or the back side."**

increased recombination, as the pseudo-fill factor (see Fig. 2(c)) remains fairly unaffected by the half-cell process. The reduction in the fill factor can instead be attributed to an increased series resistance during the cell measurements, which can be caused by the different respective contacting schemes used for full and half cells. This contacting-related issue is not expected to occur in a module. Furthermore, it was found that each of the half-cell processes yields similar, moderately loss-less, half cells. Hence, both cell separation processes lead similarly to fairly high-quality half cells with regard to electrical performance.

#### **Mechanical strength of the solar cells**

The mechanical strength data of the solar cells are shown in the 90% confidence intervals of the Weibull parameters in Table 1 and Fig. 3. Compared with the full cells, there is a significant 35% reduction in the characteristic fracture stress of the LSC batch on the back side in tension. The scattering of this batch is also significantly decreased. In contrast, on the sunny side in tension, the characteristic fracture stress of the LSC batch is decreased by 10%, compared with the full cells. In the case of the TLS batch, no significant change in mechanical strength could be observed for the sunny side or the back side. It can be assumed, therefore, that no mechanical damage occurs as a result of the TLS process.

#### **Mechanical strength of the module laminates**

For the module laminates, the characteristic fracture stress of the LSC batch is decreased by 23%, compared with the full-cell laminate, and the Weibull modulus is increased (Table 2 and Fig. 4). In contrast, the characteristic fracture stress for the TLS batch is increased by 9%, compared with the full-cell laminate, while the Weibull modulus shows no significant difference for all batches.

#### **Cell vs. module: fracture stresses and fracture origin**

The fracture stresses of all three batches (full, LSC and TLS) for the solar cell and module laminate configurations are shown in Fig. 5. In general, the fracture stresses of the cell batches are higher than those of the module laminate batches, because of additional soldering and lamination effects and the effect of size on strength due to different evaluated areas. The damage caused by the LSC process can be seen at the cell and module laminate levels, while the fracture stresses dominate in the weaker back side at the module level because of the similar loads on the sunny and back sides in the laminate.

The scattering of fracture stresses for the full-cell batch and the TLS batch are very similar at the solar cell and module laminate levels, which means that in both cases the same defect distributions are addressed. For the LSC batch, however, the scattering is much smaller than that for the other batches at the module laminate level and the cell level. As can be seen from the Weibull parameters (see Fig. 3 and Table 1), the lowest scattering occurs for the LSC cells on the back side, where the laser induces very strong but constant defects.

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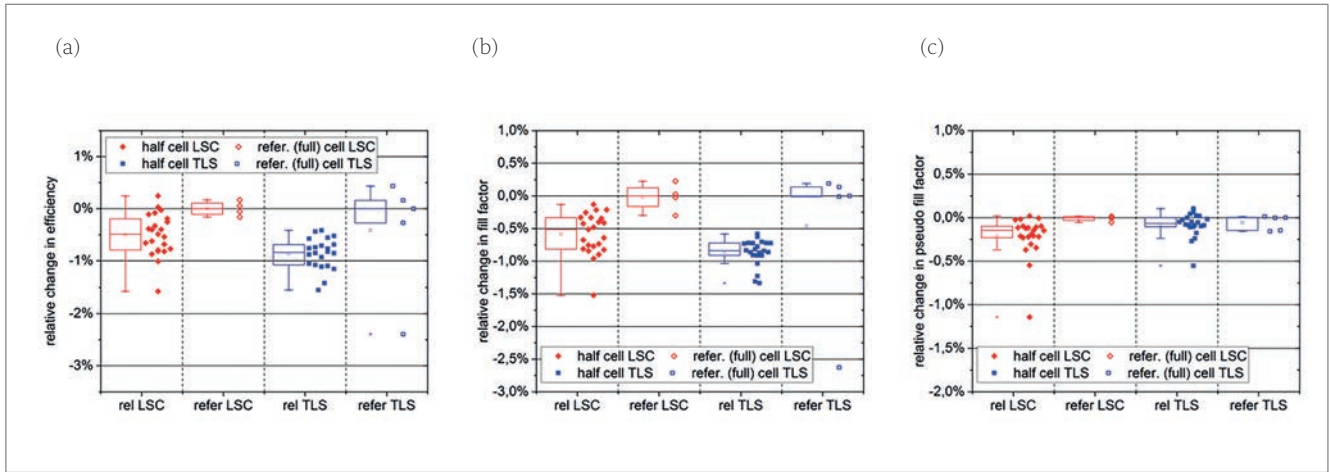


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**Figure 2. (a) Efficiency losses of half cells compared with full cells. (b) Reduced fill factors of half cells compared with full cells. (c) Pseudo-fill factors of half cells, indicating minor losses compared with full cells.**

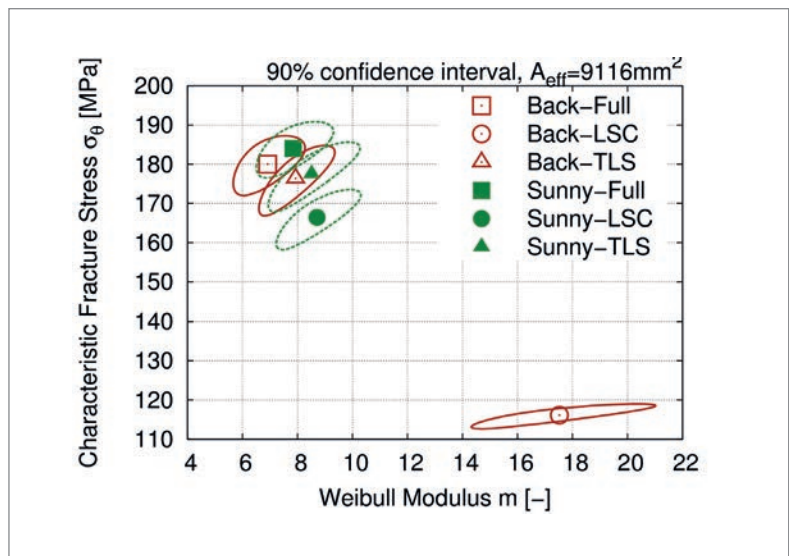
Batch	Characteristic fracture stress $\sigma_0$ [MPa]	Weibull modulus m [-]
Back-full	180.0 (173.8 ... 186.4)	6.9 (5.7 ... 8.3)
Back-LSC	116.1 (114.4 ... 117.8)	17.5 (14.3 ... 21.0)
Back-TLS	176.4 (170.8 ... 182.1)	7.9 (6.6 ... 9.4)
Sunny-full	184.0 (178.3 ... 189.8)	7.8 (6.5 ... 9.3)
Sunny-LSC	166.4 (161.8 ... 171.1)	8.7 (7.2 ... 10.3)
Sunny-TLS	177.5 (172.1 ... 182.7)	8.5 (6.9 ... 10.3)

**Table 1. Strength data for the solar cells with 90% confidence intervals (effective area  $A_{eff} = 9,116\text{mm}^2$ ).**

Examples of the fracture origins found in the laminate fracture tests are shown in Fig. 6. In the case of the full-cell and TLS batches, the fracture origins were mostly found at the back-side pads, whereas for the LSC batch the fracture origins were mostly found at the cutting edge. This result is in good agreement with the strength data, because the TLS batch does not show any damage; thus, the fracture origin is the same as that for the full-cell batch. On the other hand, the LSC batch suffers significant mechanical damage, confirmed by the fracture origins at the laser cutting edges.

**Discussion**

The two half-cell separation processes examined in this work yield half cells with comparable minor electrical losses due to the cell cutting. However, major differences between the two types of half cell have been observed in terms of their mechanical strength. The damage of the LSC batch on the back side can be explained, because the laser scribe was performed on the back side. Front-side damage, however, can also occur if the laser scribe penetrates to a depth of more than half of the silicon cell thickness. The results at the cell level are in good agreement with the literature [3,13]. Because the half-cell batches are evaluated by taking into account the effect of size on strength, through using the same effective area as the full-cell batches, a quantitative comparison of strength can be made.

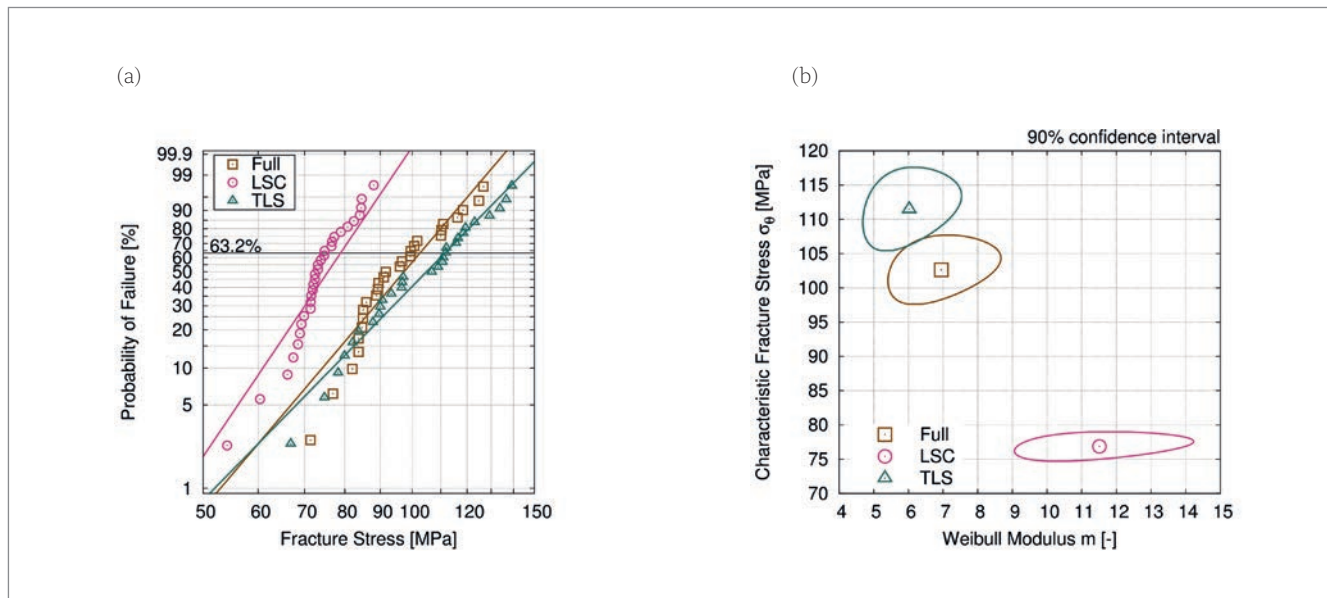


**Figure 3. Weibull parameters of the solar cells with 90% confidence intervals.**

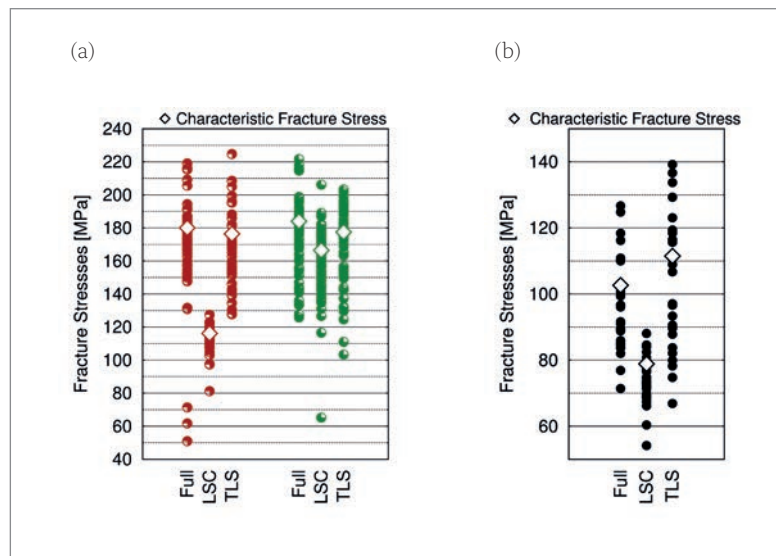
The strength results for the module laminates are quantitatively lower than the results where only the solar cells were tested; this is because of the effect of size on strength and the additional residual stresses from the soldering and lamination processes. The effect of size on strength means that the probability of finding a critical defect is greater for a larger area than for a smaller one; this is why the strength of a single solar cell has to be less than the strength of six full cells (or twelve half cells) within one module laminate. To evaluate

Batch	Characteristic fracture stress $\sigma_0$ [MPa]	Weibull modulus $m$ [-]
Full	102.6 (97.6 ... 107.7)	6.9 (5.4 ... 8.7)
LSC	78.9 (76.0 ... 81.8)	8.7 (7.0 ... 10.6)
TLS	111.5 (105.4 ... 117.6)	6.0 (4.7 ... 7.5)

**Table 2. Strength data of the module laminates with 90% confidence interval.**



**Figure 4. Mechanical strengths of the module laminates: (a) Weibull diagram; (b) Weibull parameters with 90% confidence intervals.**



**Figure 5. Fracture stresses of full cells and half cells cut by LSC and TLS and tested in a four-point bending set-up: (a) solar cells with  $A_{eff} = 9,116 \text{ mm}^2$ ; (b) module laminates.**

this effect, the strength results for the solar cells were applied to the full number and size of the cells in the module laminate configuration ( $A_{eff} = 156 \text{ mm} \times 156 \text{ mm} \times 6 = 146,016 \text{ mm}^2$ ).

Compared with the initial results (see Fig. 7(a)), the transformed cell results (see Fig. 7(b)) differ by approximately 5–30MPa from the module laminate results, which represents the remaining residual stresses arising from the soldering and lamination processes. The largest deviation

occurs for the LSC batch, where the module laminate results still exhibit lower strength, in the range of up to 30MPa, compared with the transformed cell results. This could be explained by the additional loading from the ribbons on the damaged cutting edges; the other two batches, which do not have additional damage at the edges, will not be affected. Note that the effective area of a single cell within the laminate can be much smaller than the full area of the cell as a result of inhomogeneous stress fields of the lamination and soldering processes.

## Conclusions

In the work reported in this paper, two solar cell separation processes – namely LSC and TLS – were investigated, with a particular focus on the mechanical defects. The cut solar cells were evaluated at both the cell level and the module laminate level. The first result was that both processes lead to similar half cells from an electrical point of view, while the mechanical properties of the half cells are very different. Second, it was shown that the defects responsible for breakage at the cell level are the same as those at the module laminate level. In particular, it was found that the LSC cut edge of half cells is predominant in the breakage at the cell and module laminate levels. In contrast to this, the TLS process did not show any significant mechanical damage to the cells.

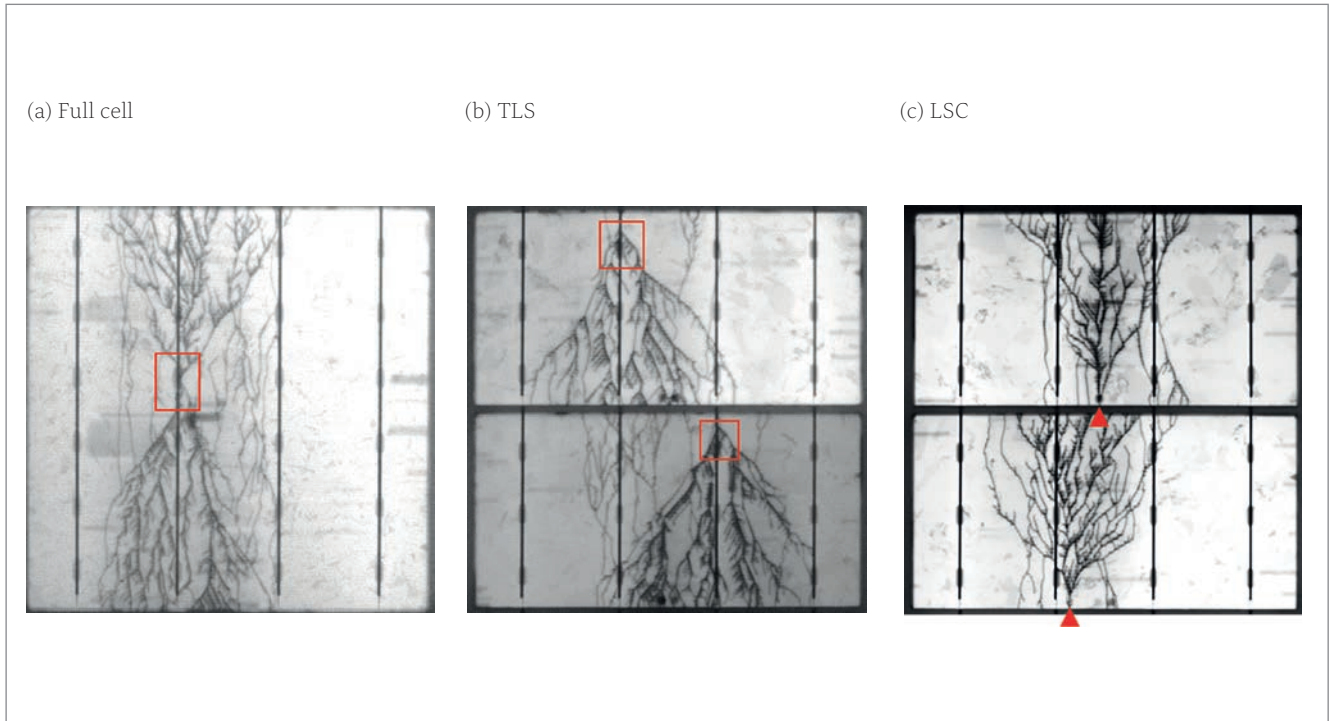


Figure 6. EL images (contrast and brightness adjusted) of broken cells from the module laminate fracture tests with fracture origin at the busbars (red squares) for (a) full cells and (b) TLS, and at the cutting edge (red triangles) for (c) LSC.

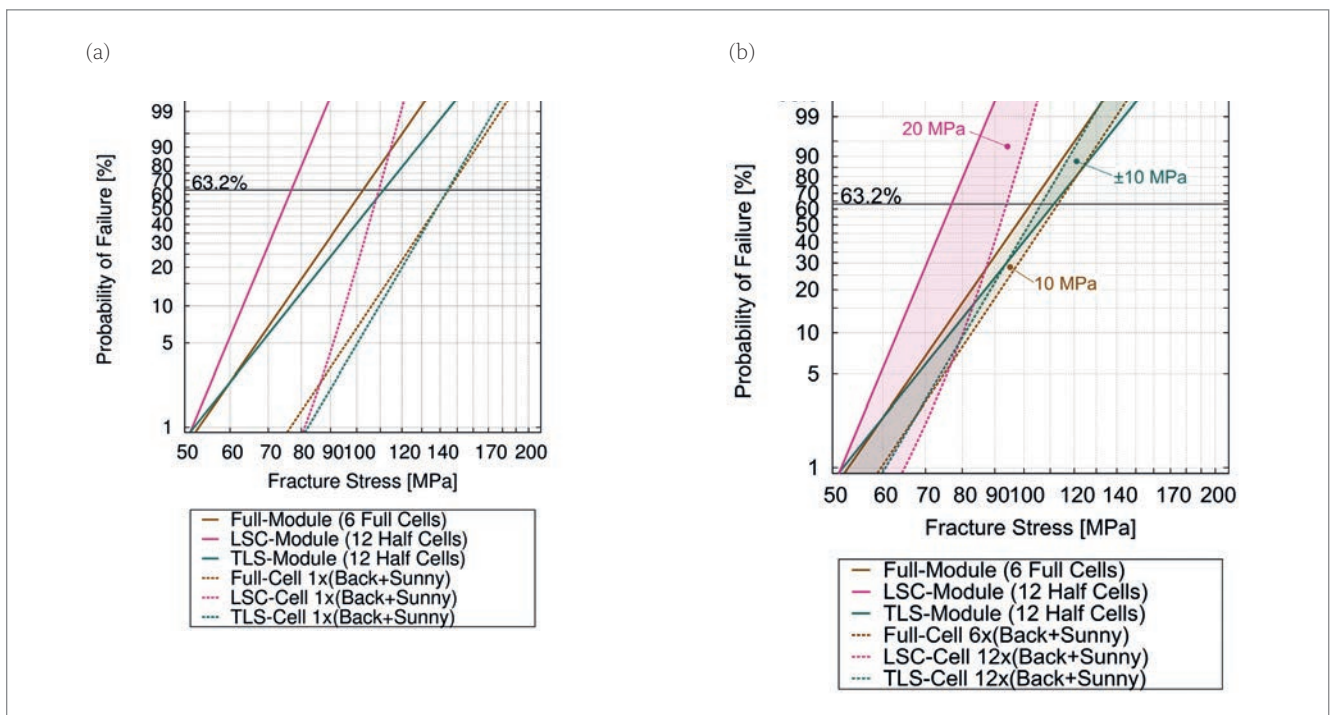


Figure 7. Application of the mechanical cell results to the module laminate configuration: (a) initial data at the module laminate and cell levels (1 full cell/1 half cell); (b) initial data at the module laminate and cell levels evaluated in terms of the size of the module laminate (6 full cells/12 half cells)

In conclusion, the mechanical testing of solar cells gives a fairly good quantitative estimate of the mechanical cell properties in the module laminate. Hence, the testing of solar cells with regard to their mechanical strength does not just characterize the cell and module production in terms of damage and yield; indeed, the testing provides more insights into the reliability of the modules in field conditions. The separation

processes strongly influence cell and module reliability and must be optimized for modules with small breakage rates.

**“The LSC batch suffers significant mechanical damage, confirmed by the fracture origins at the laser cutting edges.”**



**“The mechanical testing of solar cells gives a fairly good quantitative estimate of the mechanical cell properties in the module laminate.”**

### Outlook

Next-generation modules with further improved performance beyond the half-cell approach are already in development. The process of cutting solar cells into small strips and assembling them by shingling leads to a further reduction in electrical losses and to an enhanced active module area.

For cell cutting, the industrial approach of TLS dicing will be implemented and further optimized. The possibility of achieving excellent edge re-passivation for almost-perfect edges using TLS will be evaluated by means of various techniques, such as H<sub>2</sub> passivation carried out by plasma immersion deposition methods using organic layers. The main efforts will centre on the optimization of laser cutting in order to minimize recombination losses, as well as on demonstrating improved performance and reliability of shingled modules.

Shingling equipment based on electrically conductive adhesive (ECA) printing is in development and will target the assembly of thin (100–160µm) silicon heterojunction (SHJ) cells at a nominal throughput of 4,000 wph in a dual-lane configuration. This will be realized with a new TLS-dicing module with a bidirectional cutting head to cut cells into quarter-size strips, or smaller, and stack them into cassette bins. Integration kits of TLS dicing heads in third-party equipment will be also available.

### Acknowledgements

This work was supported by the German Federal Ministry of Economic Affairs and Energy (BMWi) within the framework of the Solar-TLS research project (Contract No. 032583C). The author would like to thank F. Kaule, M. Pander, M. Turek and S. Schoenfelder from Fraunhofer Center for Silicon Photovoltaics CSP in Halle (Saale), Germany, and E. Hofmueller from Cell Engineering GmbH in Kabelsketal, Germany, for their constant support and encouragement on this research project. He would also like to thank K. Bühler for the fruitful discussions. Work and activities regarding solar cell strips for shingled modules are financially supported through the HighLite project, funded by the EU.

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### About the Author

Michael Grimm received his Diploma in physics from Chemnitz University of Technology, and his Ph.D. in physical chemistry from the University of Wuerzburg in Germany. After a postdoctoral position at University College Dublin, he worked for several years for an equipment supplier in the solar industry, before joining 3D-Micromac in 2013. He has held various positions in the company and currently leads the Department of Technology Management, where he is responsible for technology and IP management, public-funded research projects, and national and international research cooperation.

### Enquiries

Mandy Gebhardt  
3D-Micromac AG  
Technologie-Campus 8  
09126 Chemnitz, Germany

Email: Gebhardt@3d-micromac.com

# Influences of different backsheets on PV module durability in high-humidity environments

Haidan Gong, Yiwei Guo, Minge Gao, SUNTECH

## Abstract

Different types of PV backsheets provide modules with varying levels of protection in warm, humid conditions. Haidan Gong, Minge Gao and Yiwei of Wuxi Suntech's PV test centre detail the results of research undertaken to better understand the properties of different backsheet materials in tropical conditions

As the most commonly used encapsulating materials, ethylene-vinyl acetate (EVA) and polymer backsheets play important roles in module performance by providing protection against environmental exposure. Although cured, EVA will still undergo hydrolysis when exposed to heat and moisture, leading to formation of acetic acid. The failure mechanism of modules under damp-heat conditions has been studied in other literatures [1, 2] [1, 2]. The acetic acid reacted with lead oxide and formed lead acetate, which can cause power degradation of the module. Most polymer backsheets cannot completely block the water ingress into the module. Therefore, the water vapor transmission rate (WVTR) of the backsheet is crucial to the module power degradation in a high-humidity environment. In the past, there were two different points of view. One was that a backsheet with a low WVTR should be used to obstruct moisture ingress as much as possible to inhibit the hydrolysis reaction of EVA. Another was that a breathable backsheet was preferable, meaning that

the water can easily ingress into the backsheet but also that the acetic-acid gas also can easily release from the module.

At present, there is no definite conclusion about the WVTR selection of backsheets in tropical areas. Most research has focused on the durability of the backsheet itself and paid little attention to the influences of the backsheet's water barrier properties on module durability. In this work, three aspects are discussed: module performance using backsheet with different WVTR, module performance using EVA with different VA contents and correlation between damp heat accelerated ageing and applications in high-humidity environments.

## Experiment section

Four types of commercialised backsheet were used including: glass (backsheets 1), KPO (backsheets 2), CPC (backsheets 3) and PPf (backsheets 4). Silicon-based PV modules incorporating these four different backsheets were produced, using the same manufacturing process. One special module without a backsheet was also produced. Initial stabilisation was undertaken and then modules were exposed to 85°C ambient temperature and 85% relative humidity as described in the IEC 61215 standard. Every 1,000 hours, the electrical performance of modules was tested.

EVA with two different VA contents (28% and 32%) were used. VA content was measured using chemical titration method with NaOH. The FTIR spectra were measured using a Thermal Fisher Nicolet iS50 equipment.

## Results and discussion

### Module performance using backsheet with different WVTR

External influences such as water and oxygen normally can penetrate a backsheet and go into modules as shown in Figure 1. As mentioned before, moisture in the modules can lead to

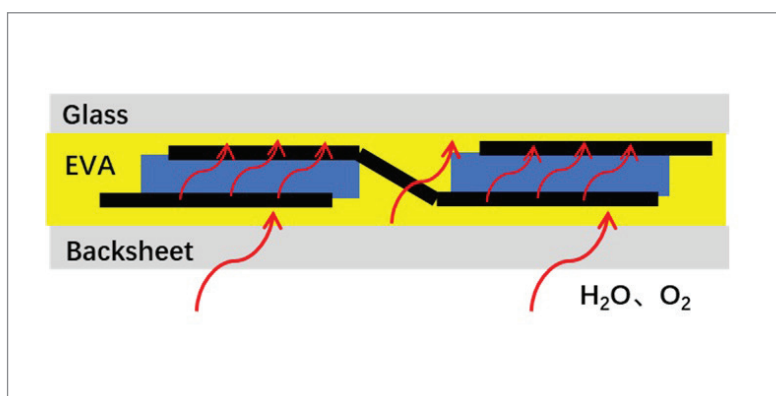


Figure 1: Water and oxygen penetration into module.

	A	B	C	D	E
WVTR (g/m <sup>2</sup> -d)	0 (glass)	125	234	330	∞ (no backsheet)

Table 1: Modules using backsheets with different WVTR.

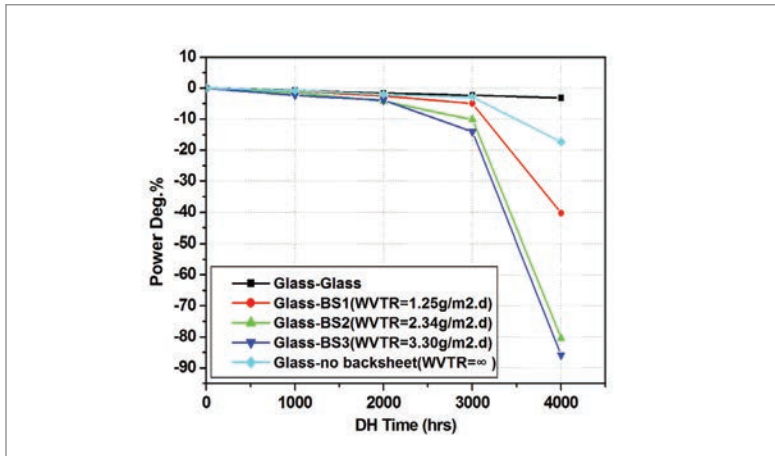


Figure 2. Power loss of modules different backsheets after DH.

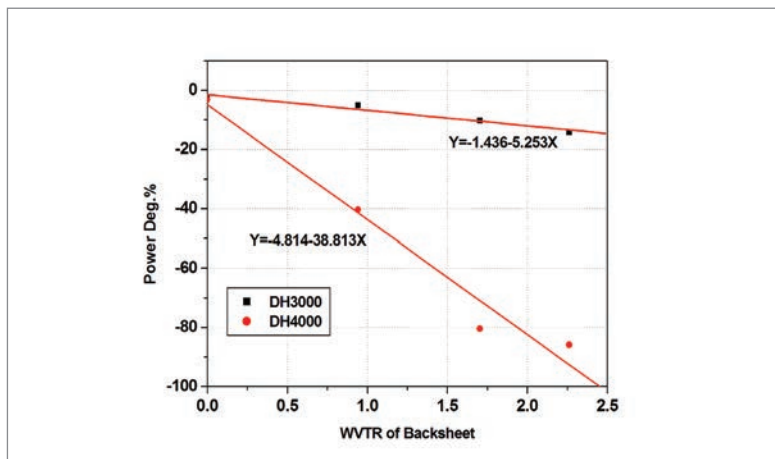


Figure 3. Power degradation vs. WVTR of backsheet.

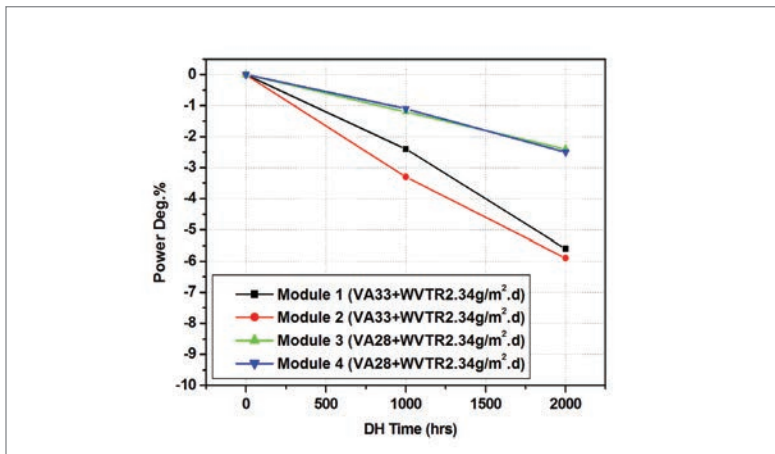


Figure 4. Power loss of modules using different EVA after DH testing.

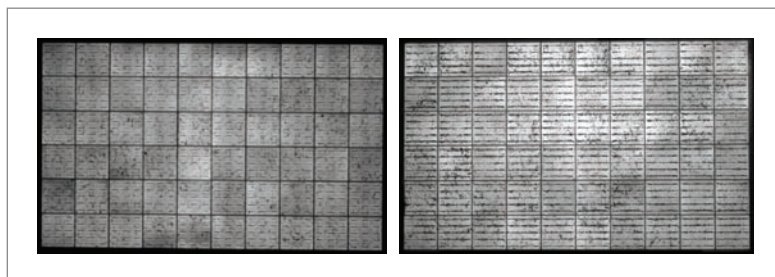


Figure 5. EL pictures of modules using different EVA after DH testing.

cell corrosion. So, the water vapor transmission property of backsheet is crucial to module reliability and durability.

Here, five groups of modules were produced under the same conditions (as shown in Table 1). Groups A to D used four types of backsheet with different WVTR and Group E were special modules without backsheets, meaning that the water vapor could totally ingress into the backsheet and the acetic-acid gas also could easily release from the modules.

These modules went through damp heat ageing for up to 4,000 hours and the module power loss was shown in Figure 2. It is clear that with increasing damp-heat time, modules using different backsheets showed different power losses. After DH 4,000h, modules using backsheet WVTR in the range of 0-40 g/m2.d (Group A to Group D), the power degradation increased linearly with increasing WVTR in a humid environment (as shown in Figure 3). The modules completely blocking water (backsheet A) showed limited power loss because these modules prevent the cell corrosion from acetic acid. The EL pictures after damp heat ageing are also shown in Table 2. The cell and ribbon corrosion conditions correspond to the power loss.

Interestingly, the modules without backsheet (Group E) showed low power degradation, and almost no cell or ribbon corrosion could be observed after 3,000h DH testing. But those modules showed large power degradation and obvious cell and ribbon corrosion after 4,000h DH testing. For modules without backsheet, in the first 3,000 hours of DH testing, the hydrolysis reaction of the EVA mainly occurred on the rear side of the module; the acetic-acid gas could also easily release from the module. But in the last 1,000 hours of DH testing, the water vapor penetrated the cell and ingressed into front side of the module, hydrolysis reaction of front side EVA is inevitable and the acetic-acid gas can't easily release through the cell.

### Module performance using EVA with different VA content

The VA content is also a key value which affects the quality of EVA. In addition, the ester group will hydrolyse in a humid environment. EVA with 28% and 32% VA content were used in modules to see how they would perform in a humid environment. As shown in Figure 4, after DH 2,000h, modules using high VA-content EVA showed higher power degradation and more severe cell and ribbon corrosion. In Figure 5, modules with a higher VA content showed more cell corrosion after damp heat. This result corresponds to the power degradation results in Figure 4.

### Correlation between damp heat accelerated ageing and applications in high humidity environment

In the natural environment, temperature, humidity and light are the three main factors that affect the



reliability and durability of modules.

In order to predict a product's lifetime in real applications, several accelerated ageing models have been created and the Arrhenius model is the most known. In a high humidity environment, temperature and humidity play the major role in module ageing. Combining temperature and humidity factors, the Hallberg-Peck model[3] is commonly used to predict the ageing process in a high-humidity environment. The Hallberg-Peck model equation is as follows:

$$AF = \left(\frac{RH_t}{RH_u}\right)^3 \times e^{\left(\frac{E_a}{K}\right) \times \left(\frac{1}{T_u} - \frac{1}{T_t}\right)} \dots \dots \dots eq1$$

- AF: accelerated factor
- Ea: activation energy of this failure mode
- K: boltzmann constant
- Tu: absolute temperature under usage
- Tt: absolute temperature under test
- RHu: relative humidity under usage
- RHt: relative humidity under test

Exceeded ageing time = Desired lifetime/AF ...eq2

In the Hallberg-Peck model, the exceeded ageing time is related to the temperatrue and humidity in the application area as well as the activation energy of the modules' failure mode. The activation energy of the modules' failure is a the key parameter in this model and usually it is an empiric value. Three real cases were studied to obtain the activation energy of this failure mode.

**Case 1: modules installed in Southeast Asia in March 2012; average environmental temperature, 28.2°C, and average relative humidity, 61.8%.**

As shown in Figure 6, after only eight years operation, the PR of the whole PV plant show a high level of degradatioon, close the theoretical degradation over 25 years.

Four modules were taken from the PV plant to measure the power output under a Class AAA pulse solar simulator. The results are shown in Table 3. It can be observed that the average power degradation of the modules encapsulated with BS WVTR 1.5 + VA33 EVA after eight years' operation is 28.5% and the average power degradation of the modules encapsulated with BS WVTR 1.5 + VA28 is 20%. We also took four modules from the warehouse, with the same encapsulation material and same production period (W32, 2011) as the modules from the PV plant, to receive 2,000h of damp heat testing. The results are shown in Table 4. It can be observed that there is a good correlation between 2,000h damp heat accelerated ageing and eight years of operation in a Southeast Asian tropical environment. The average power degradation of the modules encapsulated with BS WVTR 1.5 + VA33 EVA after 2,000h of damp heat testing is 26% and the average power degradation of the modules encapsulated with BS WVTR 1.5 + VA28 is 16%.

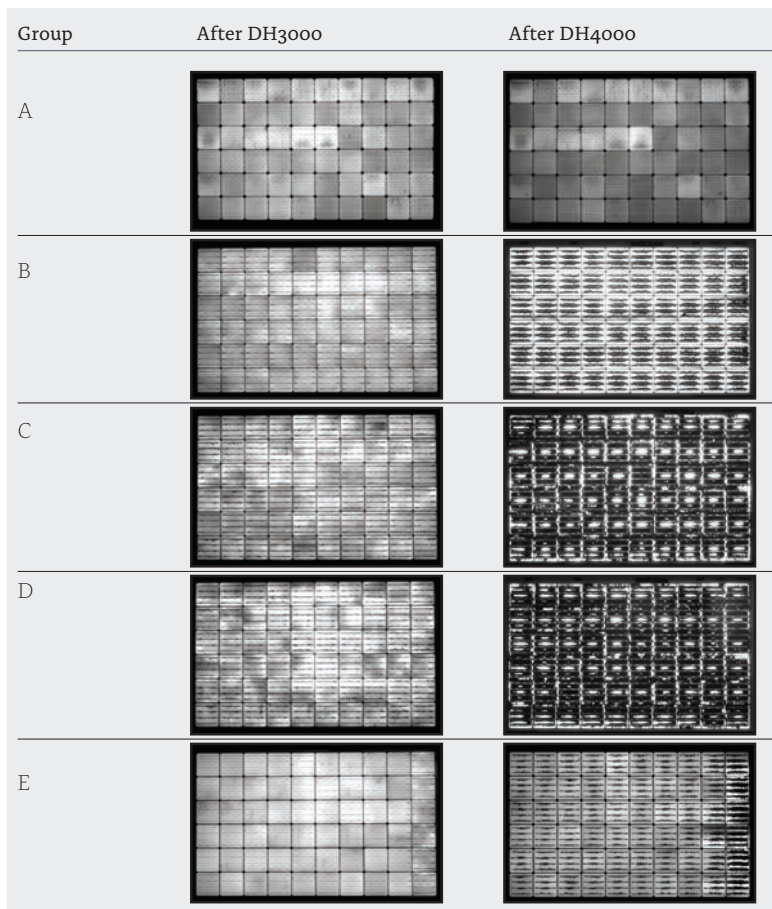


Table 2: EL pictures of modules with different backsheets after DH.

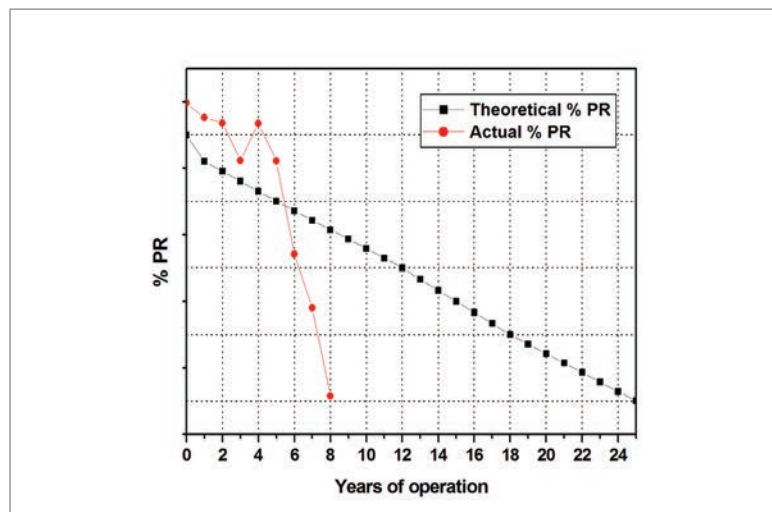


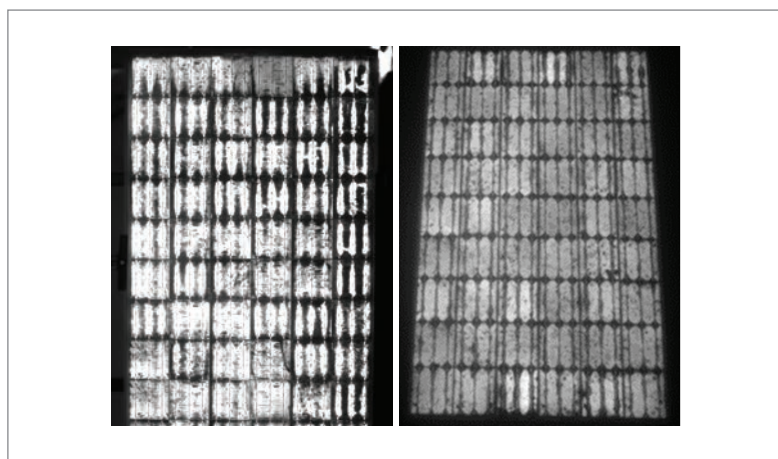
Figure 6. Actual PR degradation case installed in Southeast Asia.

No.#	Pmax @initial	Pmax @after 8years	Deg.%	Material
1	294.2	200.9	32%	BS WVTR 1.5 + VA33 EVA
2	287.5	214.4	25%	
Avg. Deg.%			28.5%	
3	290.1	256.6	12%	BS WVTR 1.5 + VA28 EVA
4	291.3	209.9	28%	
Avg. Deg.%			20%	

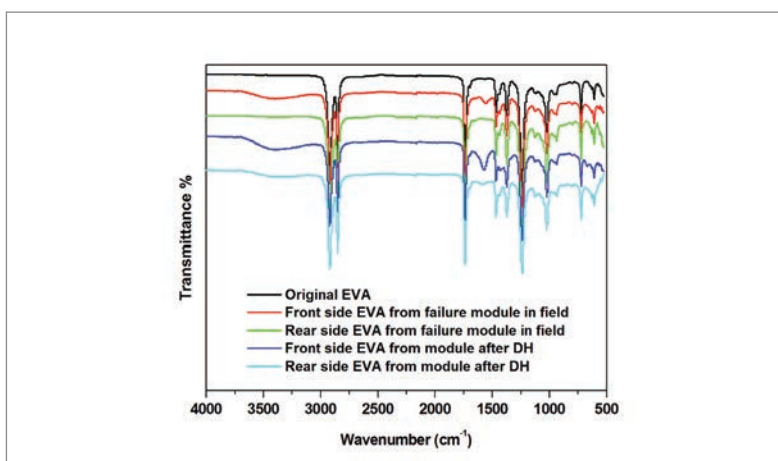
Table 3. Power output of modules from Southeast Asia PV plant under class AAA pulse solar simulator.

No.#	Pmax @initial	Pmax @DH1000	Pmax @DH2000	Deg.% @DH2000	Material
1	280.9	276.1	205.8	27%	BS WVTR
2	278.5	277.0	208.1	25%	1.5 + VA33 EVA
Avg. Deg.%				26%	
3	213.6	206.4	188.4	12%	BS WVTR
4	213.5	209.5	170.7	20%	1.5 + VA28 EVA
Avg. Deg.%				16%	

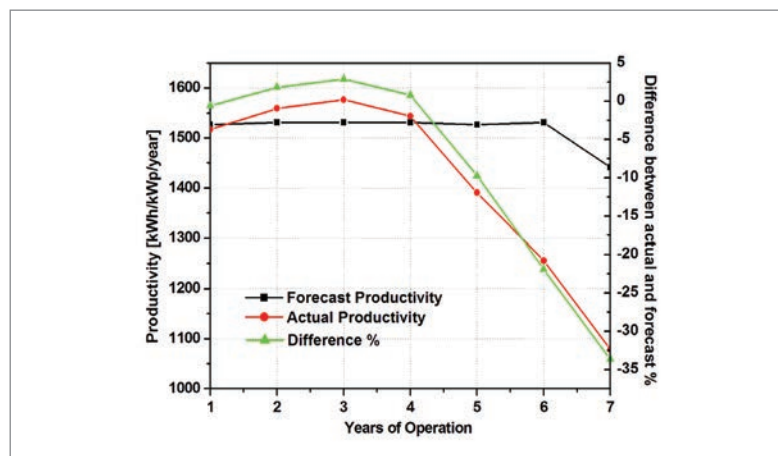
**Table 4. Power output of modules from warehouse under class AAA pulse solar simulator.**



**Figure 7. Left: module after installation in a high-humidity area for eight years; right: module after DH 2,000 hours.**



**Figure 8. FTIR spectra of EVA from modules in field and after DH.**



**Figure 9. Actual PR degradation of modules installed on Island A.**

The electroluminescence (EL) after DH 2,000h showed similar appearances to the EL of modules aged in the Southeast Asian PV plant for eight years (Figure 7). Furthermore, Fourier-transform infrared spectroscopy (FTIR) was also applied to analyse the failure mechanism of the modules installed in the Southeast Asian PV plant and the modules after damp heat test (Figure 8). It was found that these modules have similar failure mechanisms. Lead acetate can be detected on the front side EVA. It is commonly believed that water vapor will penetrate into modules and lead to EVA hydrolysis. The resulting acetic acid will react with lead oxide in ribbons and cells. The formed lead acetate will cause resistance increases and cell darkening in EL. The difference is, lead acetate and peak EVA hydrolysis can't be detected on the rear side EVA in a failed module in the field. However, lead acetate and peak EVA hydrolysis can be detected on the rear side EVA of the module after damp heat testing. This result showed that the water vapor can ingress into the rear side of the module but also can diffuse to the outside through the backsheet in the field because the moisture concentration is different between inside and outside the module during day and night. When the water vapor penetrates a cell and ingresses into the front side of the module and can't easily diffuse through the cell, a hydrolysis reaction in front side EVA occurs. However, for the indoor ageing test, the water vapor will reach equilibrium both inside and outside the module during the whole ageing test, so the hydrolysis reaction of rear side EVA is inevitable.

Power degradation value, the EL images and FTIR showed that the indoor 2,000hrs of damp heat testing is equivalent to eight years operation in Thailand area. So according to the eq2, the AF is 35.04.

**Case 2: modules installed on tropical Island A in 2012; average environmental temperature, 26.9°, and average relative humidity, 78.5%.** As shown in Figure 9, only after six years' operation, the actual yield of electrical energy has 21.9% loss. In the EL image shown in Figure 10, cell corrosion also can be observed. Those modules are encapsulated with the BS WVTR 1.5 + VA33 EVA and BS WVTR 1.5 + VA28 EVA. According to Table 5, there is a good correlation between 2,000hrs damp heat accelerated ageing and six years of operation in the Island A environment. So according to the eq2, the AF is 26.28.

**Case 3: modules installed on tropical Island B in 2013; average environmental temperature, 27.2°C, and average relative humidity, 81.7%.** As shown in Table 6, only after four years of operation, the actual yield of electrical energy shows a 17.6% loss. In the EL image shown in Figure 11, cell corrosion also can be observed. Those modules are encapsulated with the BS WVTR 1.5 and VA28 EVA. According to Table 4, there is a good correlation between the 2,000 hours of damp heat accelerated ageing and four years' operation



in the Island B environment. So according to the eq2, the AF is 17.52.

According to these three real cases, we can calculate the failure activation energy (Ea) of the failure mode in tropical areas; the related data are listed in Table 7. The Ea is about 0.425 to 0.482. Then we can use this Ea and Hallberg-Peck model to calculate the different indoor extended damp heat testing time at different temperature and relative humidity area.

### Conclusion

This work mainly focuses on the influence of backsheets WVTR on module performance in high-humidity environments. Theoretical modelling and field case data showed that long time damp heat accelerated ageing can simulate the module ageing pattern in a high-humidity field environment. Using the Hallberg-Peck model, the activation energy was calculated in areas with different temperatures and relative humidity. In addition, results showed that modules using backsheets WVTR in the range of 0-4.0 g/m<sup>2</sup>-d, the power degradation increased linearly with increasing backsheets WVTR in a humid environment. Finally, module performance using VA content 28% and 32% were compared. It was found that high VA content EVA will lead to higher power degradation and cell corrosion.

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- [2] Peike C, Hoffmann S, Hulsmann P 2013 Solar Energy Materials & Solar Cells 116 49-54
- [3] Hallberg O, Peck D S 1991 Qual. Reliab. Eng. 7 169-180

### About the Authors



Haidan Gong leads of the PV test centre at SUNTECH. She studied polymer material at the Changzhou University of Jiangsu and received her master's degree in 2008. She has been with Suntech since 2008. Her current research interests include failure analysis in modules and materials.



Yiwei Guo is the material testing engineer of PV test centre at Suntech, which focuses on the testing and evaluation of PV material. He has been with Suntech since 2008.



Minge Gao is a material testing engineer at the PV test centre at Suntech. She graduated from Yangzhou University majoring in polymer materials in 2007. She has been with Suntech since 2008.

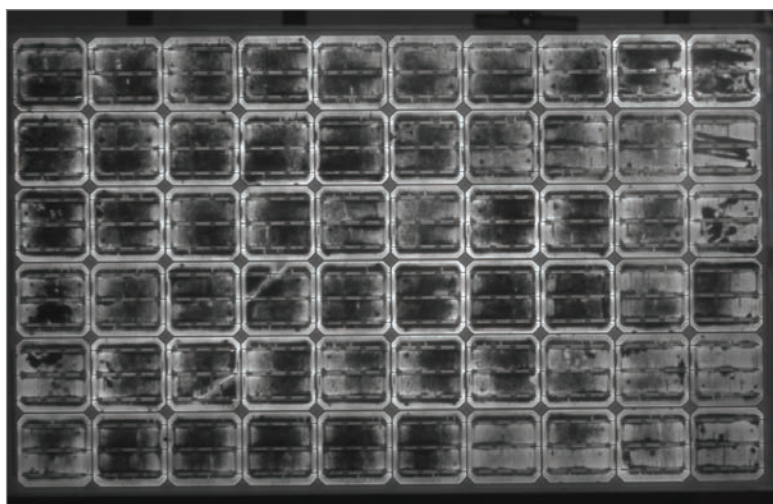


Figure 10. Module after installation on Island A for six years.

No.#	Pmax @initial	Pmax @after 8years	Deg.%	Material
1	245.8	178.2	27%	BS WVTR 1.5 + VA33 EVA
2	240.0	207.0	13.8%	BS WVTR 1.5 + VA28 EVA

Table 5. Power output of modules from Island A PV plant under class AAA pulse solar simulator.

	2013	2014	2015	2016
Yield (KWh)	85	85	75	70
% Yield Loss			11.8%	17.6%

Table 6. Actual yield of electrical energy from modules on Island B.

	Avg. Temperature (°C)	Avg. Relative humidity (%)	AF	Calculated Ea (eV)
Southeast Asia solar plant	28.2	61.8	35.04	0.425
Island A solar plant	26.9	78.5	26.28	0.482
Island B solar plant	27.2	81.7	17.52	0.440

Table 7: The failure activation energy in tropical areas.

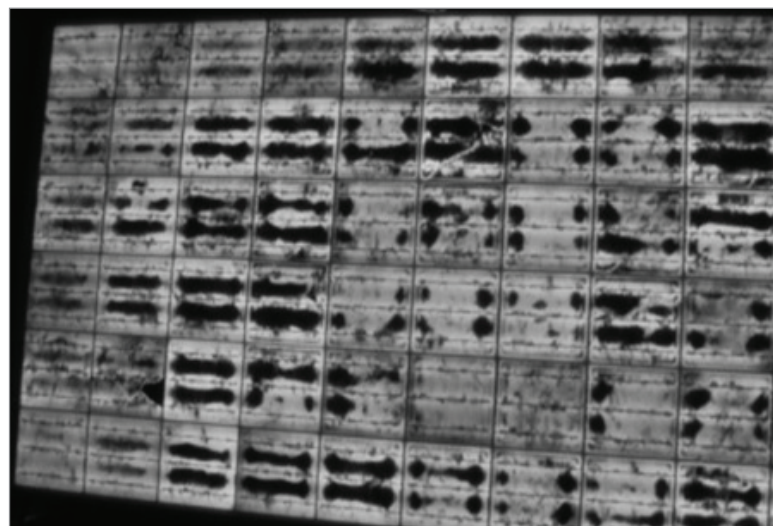


Figure 11. Module after installation on tropical Island B for four years.



# Screen-printing process development towards 20 $\mu\text{m}$ front-side Ag electrodes on Si solar cells

Florian Clement, Sebastian Tepner, Michael Linse, Linda Ney, Noah Wengenmeyr, Maximilian Pospischil, Andreas Lorenz & Ralf Preu, Fraunhofer Institute for Solar Energy Systems ISE, Freiburg, Germany

## Abstract

For the work reported in this paper, a new model of the screen-printing process was set up in order to improve the understanding of the screen-printing process, with a focus on the interaction between Ag paste and the screen. Initial results have shown that the wall slip behaviour of the paste can be significantly improved by adapting the screen chemistry, enabling lower finger resistances and reduced finger widths. In this experiment, a mean contact finger width  $w_f = 26\mu\text{m}$ , combined with a mean finger resistance  $R_f = 99\Omega/\text{m}$ , showed the high potential of the newly developed screen chemistry using single-step screen printing. Moreover, finger resistance values well below  $1,000\Omega/\text{m}$  were achieved for nominal finger widths  $w_n$  down to  $15\mu\text{m}$ , resulting in printed finger widths below  $20\mu\text{m}$  at finger heights  $h_f = 18\mu\text{m}$ . This demonstrates the high potential of the single-step screen-printing process on the way to ultra-fine-line contacts in combination with multi-busbar cell layouts. PERC-type Cz-Si solar cells fabricated with a five-busbar cell layout and a nominal screen opening  $w_n = 24\mu\text{m}$  have produced efficiencies of up to 22.1%, while the initial busbarless Si solar cells for multiwire interconnection with a  $18\mu\text{m}$  nominal screen opening have demonstrated a significant Ag reduction of about 65%.

## Introduction

One of the main challenges in silicon (Si) solar cell metallization is to decrease printed finger width and silver (Ag) consumption. Over the last two decades significant improvements have been made by paste, screen and machine development, reducing the average printed finger width from over  $100\mu\text{m}$  in 2005 to  $20\mu\text{m}$  in 2019 [1,2]. Nevertheless, it is planned to further improve the front-side metallization process as a key technology for the production of silicon solar cells.

Although screen-printing technology has now become established on the market, before other emerging printing technologies are able to surpass the flatbed screen-printing process in its robustness against the production environment, its throughput rate and its stable printability, there are several areas that can still be addressed in R&D [3]. Specifically, the technological limits of the printing process and the associated components are going

to have to be shifted in the direction of narrower contact widths ( $<20\mu\text{m}$ ) with sufficient contact heights. The adaptation and optimization of not only the screen manufacturing process but also the screen chemistry play a crucial role when fine-line printing is desired [1,4].

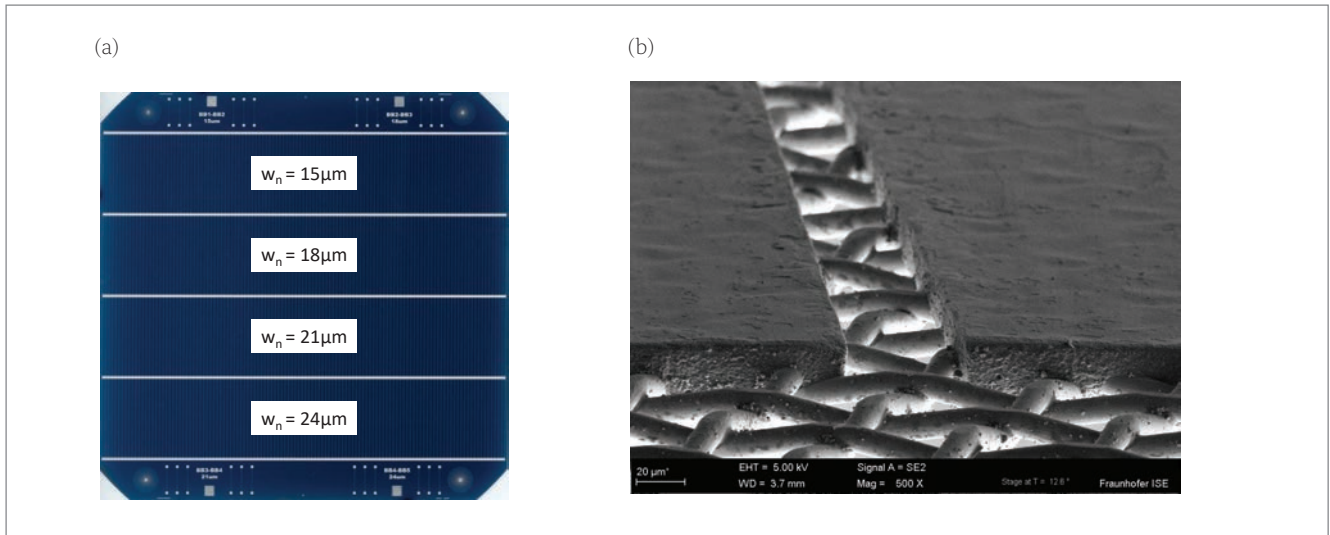
In addition to experimental work on printing-parameter optimization, the development of a model for the theoretical description of the printing process will enable the identification and efficient optimization of key influencing factors during the printing process. Furthermore, silver consumption in the screen-printing process needs to be improved by realizing contact fingers with an improved shape and homogeneity. Finally, the reduction of process costs in  $\text{€}/\text{Wp}$  is another major goal of the activities at Fraunhofer ISE.

This paper presents the latest improvements regarding the flatbed screen-printing process aimed at ultra-fine-line contacts. A theoretical model is set up to understand the interactions between screen, paste, substrate and the printing process itself. For this very purpose, Tepner et al. [1] performed a series of rheological investigations and printing experiments to study the paste–screen interaction during the different phases of the screen-printing process.

Various types of screen mesh and different screen chemistries (e.g. emulsions, surface coatings) are investigated in order to improve the screen properties for a reliable fine-line printing process. A test layout with four segments (decreasing nominal finger width  $w_n$ ) was therefore designed which allows an inline measurement of grid resistance (and thus mean finger resistance) for each nominal finger width (see Fig. 1). Finally, passivated emitter and rear contact (PERC) type Si solar cells are produced and characterized in order to demonstrate high solar cell efficiencies in combination with a lower Ag consumption.

Throughout this paper, the fundamental basis of a theoretical model of the screen-printing process is discussed, starting with a presentation of the latest work on the rheological investigation of the paste–screen interaction and its correlation to printing performance. Furthermore, an overview is given of the screen modelling and simulation approach published

**“The adaptation and optimization of not only the screen manufacturing process but also the screen chemistry play a crucial role when fine-line printing is desired.”**



**Figure 1. (a) The newly designed test layout with four segments with decreasing nominal finger widths  $w_n$  (here: 24, 21, 18, 15  $\mu\text{m}$ ) on a single wafer. The distances and number of contact fingers correspond to a typical solar cell layout, and thus allows a direct inline measurement using an industrial I–V tester. (b) SEM image of a high-precision screen [4].**

by Ney et al. [5] and Tepner et al. [6]. To conclude, an evaluation is offered of the different types of screen configuration from various screen suppliers by means of a printing test and cell experiment.

### Overview of fundamental investigations of the screen-printing process

A theoretical multidimensional model of the screen-printing process is set up in order to understand the screen-printing process in more detail. The model is developed in three steps:

1. Fluid–structure interaction: the paste–screen interaction is investigated in order to derive the design goals for the wire and emulsion surface properties which will optimize the flow and slip behaviour of metal pastes during the different process phases in screen printing.
2. Screen architecture modelling: a model is developed which predicts the size, the geometric form and the exact location of all individual openings within a screen channel, along with their dependency on all screen design parameters (e.g. mesh count, wire diameter, screen angle, screen opening width).
3. Combination of fluid–structure interaction and screen architecture modelling: steps 1 and 2 above are combined in order to model and optimize the entire screen-printing process on the Si wafers.

Up until now, the focus has been on the first and second steps. Tepner et al. [1] showed that the interface between the paste and the emulsion surface requires significant slip behaviour when an optimized screen snap-off during printing is desired. In that study, a functional coating was applied onto the screen (emulsion surface and mesh wires) by plasma-enhanced physical vapour

deposition (PECVD). The surface properties of the applied coating allow an increased paste transfer and reduced spreading on the substrate. In order to verify this hypothesis by Tepner et al. [1], contact angle measurements of respective paste solvents were carried out, and the corresponding work of adhesion  $W_a$  on the surface was calculated.

Table 1 presents the measurements of contact angles  $\theta$  of paste solvent A on various coated surfaces. An exponential correlation between the work of adhesion  $W_a$  and the ability to slip at the coated emulsion surface was discovered. At high contact angles, the work of adhesion between the surface and the paste solvent is reduced, resulting in an increased slip velocity at the paste–emulsion interface. Fig. 2(a, b) presents a schematic overview of the process mechanics, showing how more paste volume is pushed into the screen channel during the flooding phase of the screen-printing process. Furthermore, high slip velocities during the snap-off mechanics will result in a reduction in shearing forces induced by the paste sample. By achieving this particular flow behaviour, the critical yield stress of the paste will not be surpassed, and therefore potential spreading on the substrate will be reduced or even prevented. For this reason, the two best paste-coating candidates were tested during screen printing.

In Fig. 2(c), the metallization results for paste A with three different screens (uncoated reference, coating C and coating D) are presented. There is a significant reduction in printed finger width  $w_f$  for the coated surfaces because less spreading occurs on the substrate. Furthermore, in the case of the 27  $\mu\text{m}$ -wide screen opening the paste transfer is increased, resulting in an increased cross-sectional area  $A_f$  of the printed contact finger and a reduced lateral finger resistance  $R_{\text{Finger}}$  for coating C

For the second step of the presented theoretical model of the screen-printing process, Ney et al. [5,6] developed a screen simulation approach, with

which it is possible to investigate the dependency of the open area OA within a screen opening on all relevant screen design parameters (e.g. channel length, mesh count, wire diameter, screen opening width, position on the screen).

Fig. 3(a) illustrates the definition of the parameter  $\sigma_{OA}$ , which describes how much the open area deviates from the mean value across the channel length. In Fig. 3(b), simulation results for different screen angles and screen opening widths are presented, revealing that high screen angles show promise of less deviation of OA at small screen openings. This result indicates that a further reduction in lateral finger resistance  $R_{\text{finger}}$  is expected, because local reductions in printed finger height will be minimized.

Furthermore, Tepner et al. [6] expanded on this simulation approach to investigate the existence of wire crossings in screen openings; they showed that this simulation method can be used to find screen patterns with extraordinary features (e.g. 'knotless' configurations at screen angles above  $0^\circ$ , without the drawbacks of conventional 'knotless' screens). In future studies, the presented approaches and results will be combined in order to optimize the screen-printing process in terms of printing performance, throughput rate, and cost and reliability of the screen manufacturing process.

## Screen-printing process development

Screen-printing process development was undertaken to realize contact fingers with finger widths  $w_f$  below  $20\mu\text{m}$  and fewer finger interruptions suitable for a multi-busbar ( $>5$ ) front-side metallization. The results of two independent test runs – experiment A and experiment B – are discussed next.

### Experiment A

In the first test run, four different screens were evaluated [4]:

1. 480-0.011-22.5°: mesh count 480, wire diameter  $11\mu\text{m}$ , screen angle  $22.5^\circ$
2. 430-0.013-22.5°: mesh count 430, wire diameter  $13\mu\text{m}$ , screen angle  $22.5^\circ$
3. 380-0.014-30°: mesh count 380, wire diameter  $14\mu\text{m}$ , screen angle  $30^\circ$
4. 380-0.014-22.5°: mesh count 380, wire diameter  $14\mu\text{m}$ , screen angle  $22.5^\circ$

Coating C was applied to each screen. Selected results of the first test run are shown in Figs. 4 and 5. Finger openings/widths below  $20\mu\text{m}$  are achieved in the screen and on textured Si wafers with anti-reflection coating (ARC). The lowest finger resistance values are obtained with the finest mesh and lowest wire diameter, as expected.



## The innovative solution for quality control of coatings on PERC cells

- ▶ QC for multi- and c-Si based solar cell manufacturing
- ▶ Thickness measurement of AR coatings and passivation layers
- ▶ Long-term stability monitoring of deposition process
- ▶ Easy recipe based push button operation
- ▶ Software interface for data transfer
- ▶ Wafer size up to  $220 \times 220 \text{ mm}^2$



	Uncoated reference	Coating A	Coating B	Coating C	Coating D
Contact angle [°]	14.3±1.3	16.7±2.7	36.1±0.9	52.9±1.8	58.3±2.0

**Table 1. Contact angle measurements for paste solvent A on different coating surfaces.**

No clear evidence of an influence of the different screen angles is seen here.

Finger resistance  $R_{\text{Finger}}$  values well below  $1,000\Omega/\text{m}$  using a 480-0.011 screen mesh (mesh count: 480, mesh wire diameter  $11\mu\text{m}$ ) show that nominal finger widths  $w_n$  down to  $18\mu\text{m}$  can be printed with sufficiently low finger resistance values for solar cells with a busbarless layout intended for multiwire interconnection. The values for the fingers printed with a nominal finger width  $w_n = 21\mu\text{m}$  and  $w_n = 24\mu\text{m}$  enable the realization of a five or six busbar cell without significant fill factor (FF) losses. However, a nominal finger width  $w_n = 15\mu\text{m}$  is still challenging for a reliable solar cell metallization using a single-step screen-printing process, because of the strongly inhomogeneous finger geometry (see Fig. 4(a), top).

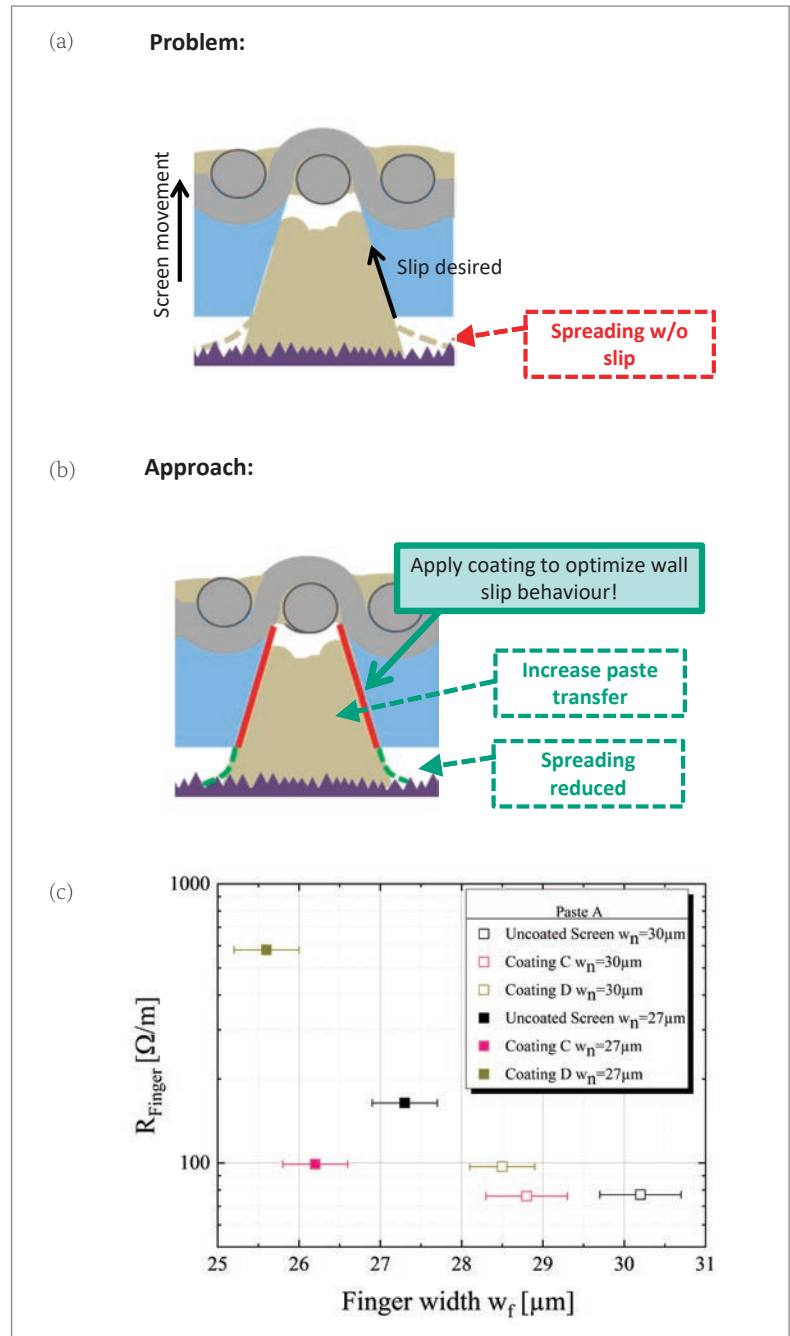
**Experiment B**

In the second test run, a screen with screen angle  $0^\circ$ , a so-called ‘knotless’ screen, was integrated. The following screens were evaluated [7]:

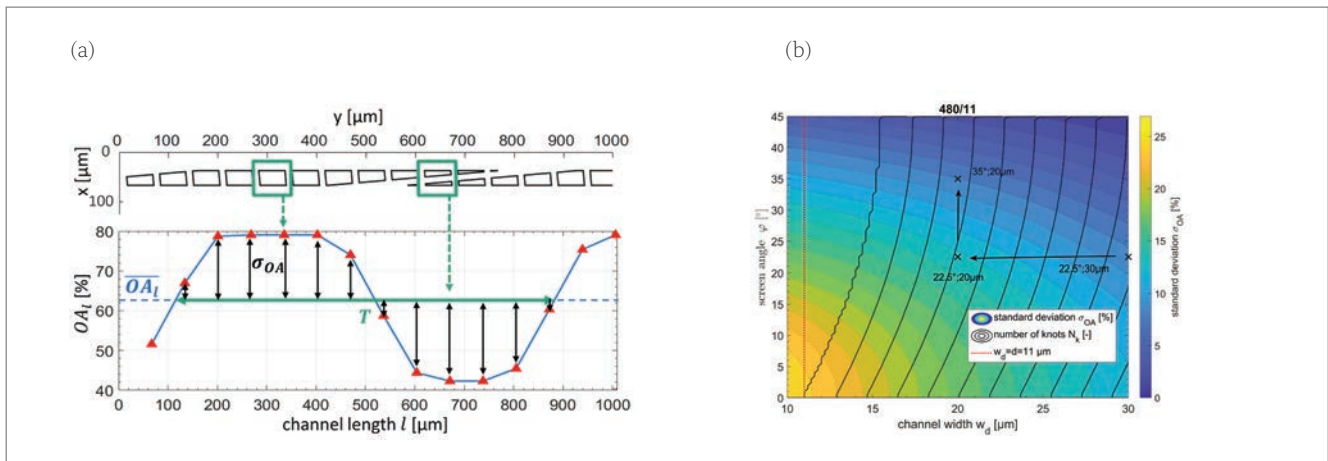
- 380-0.014-30°: mesh count 380, wire diameter  $14\mu\text{m}$ , screen angle  $30^\circ$
- 440-0.013-30°: mesh count 440, wire diameter  $13\mu\text{m}$ , screen angle  $30^\circ$
- 440-0.013-0°: mesh count 440, wire diameter  $13\mu\text{m}$ , screen angle  $0^\circ$  (‘knotless’)
- 480-0.011-30°: mesh count 480, wire diameter  $11\mu\text{m}$ , screen angle  $30^\circ$

Selected results of the second test run are shown in Figs. 6 and 7. In comparison to the first test run, nominal finger widths  $w_n$  down to  $15\mu\text{m}$  can be realized with an adequately low finger resistance. The  $0^\circ$  angle ‘knotless’ screen yields the best performance in terms of finger geometry and resistance. On textured Si wafers with ARC, a record finger geometry is achieved with an average finger width  $w_f = 19\mu\text{m}$  and an average finger height  $h_f = 18\mu\text{m}$ . The lowest finger resistance values are also obtained with the ‘knotless’ screen;  $R_{\text{Finger}}$  values well below  $1,000\Omega/\text{m}$  using this screen demonstrate that a nominal finger width  $w_n = 15\mu\text{m}$  can be printed with sufficiently low finger resistance values for solar cells with a multi-busbar module integration. The values for  $w_n = 18\mu\text{m}$  to  $24\mu\text{m}$  allow the realization of five- or six-busbar cells. Although possible for the ‘knotless’ screen, a nominal finger width  $w_n = 15\mu\text{m}$  is still a challenge to achieve with conventionally angled screens.

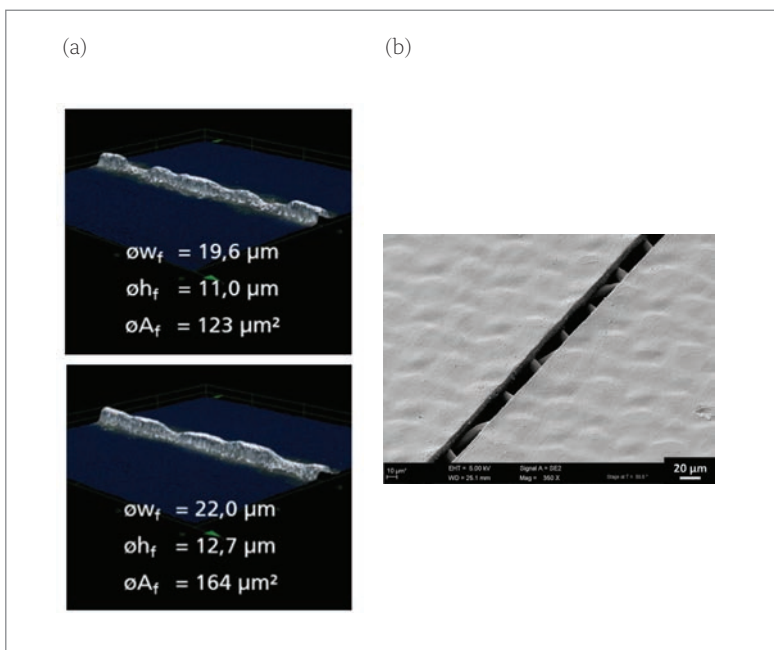
“There is a significant reduction in printed finger width  $w_f$  for the coated surfaces because less spreading occurs on the substrate.”



**Figure 2. (a, b) Optimization approach for the paste–screen interaction. Screen chemistries (C, D) are coated onto the emulsion surface to enhance the slip behaviour during flooding and screen snap-off. (c) Correlation between the printed finger width  $w_f$  and the corresponding lateral finger resistance  $R_{\text{Finger}}$ . The application of coating C results in a significant reduction in printed finger width  $w_f$  because of less spreading on the substrate. Moreover, for the  $27\mu\text{m}$ -wide screen opening the paste transfer is increased. For coating D, with a screen opening  $w_n = 27\mu\text{m}$ , some challenges during the manufacturing process need to be resolved in order to ensure a satisfactory printing result [1].**



**Figure 3.** (a) Simulated oscillating behaviour of the local open area  $OA_l$  (blue curve) along the channel length  $l$ , with screen angle  $\varphi = 5^\circ$  and  $w_d = 30\mu\text{m}$ . From this, the standard deviation  $\sigma_{OA}$  of the local open area can be derived. (b) Dependency of  $\sigma_{OA}$  and the number of knots (contour lines) on the screen angle  $\varphi$  and channel length  $w_d$ , with a constant mesh count  $MC = 480/\text{inch}$  and a constant wire diameter  $d = 11\mu\text{m}$  [5].



**Figure 4.** (a) Selected 3D microscope measurements of a single-step screen-printed contact finger on a textured Si wafer with ARC, printed using a 480-0.011 mesh with screen chemistry coating C and nominal finger widths  $w_n = 15\mu\text{m}$  (top) and  $w_n = 18\mu\text{m}$  (bottom). The measured mean values for the finger width  $w_f$ , height  $h_f$ , and cross section  $A_f$  are shown. (b) SEM image of a screen with a 480-0.011 mesh with screen chemistry coating C [4].

### Si solar cell results

In this work, cell runs with industrial pre-processed Cz-Si PERC-type solar cells from two different cell suppliers are presented. This means that all front-end processes, including two-side passivation, were carried out by an external cell supplier, while all back-end processes were done at the PV-TEC back-end lab at Fraunhofer ISE.

#### Experiment 1

In the first experiment, four different screens (360-0.016-22.5°, 380-0.014-22.5°, 440-0.013-0° ‘knotless’,

480-0.011-22.5°) were used in three different print runs (2017, 2018, 2019). In all runs, the same pre-processed Cz-Si PERC-type solar cells were used from cell supplier A. In run ‘2019’, a five-busbar and a busbarless cell layout were realized.

The process flow and cell results are presented in Fig. 8. The best cell efficiency  $\eta_{\text{max}} = 22.1\%$  (screen 430-0.013-0° ‘knotless’) was independently confirmed by Fraunhofer ISE CaLab [7]. The results demonstrate a significant efficiency increase  $\Delta\eta$  of almost 1%<sub>abs</sub>, and at the same time a clear reduction in printed finger widths as well as in Ag consumption, in comparison to the starting point in run ‘2017’. An Ag reduction of around 35% for the five-busbar layout from ‘2017’ to ‘2019’, and a printed finger width  $w_f = 22\mu\text{m}$  for the multi-busbar cell layout in run ‘2019’, underline the significant potential of the newly developed fine-line screen-printing process.

#### Experiment 2

The process flow and the cell efficiencies for the second experiment are presented in Fig. 9. Here, pre-processed Cz-Si PERC-type solar cells from cell supplier B are used. In this experiment, the focus is on a direct comparison of screen angles 30° and 0° [7]; both of these screens have the same mesh count (440) and wire diameter (24 $\mu\text{m}$ ). Moreover, two different Heraeus front-side pastes were used: paste A, which is the same as in the first experiment, and paste B.

The ‘knotless’ screen configuration leads to a substantial increase of 0.3%<sub>abs</sub> in cell efficiency. However, the cell efficiencies for the ‘knotless’ screen are lower than those obtained in the first experiment, because of the different cell supplier.

#### Summary

In the work reported in this paper, a new theoretical model of the screen-printing process was set up in order to improve the understanding of the screen-printing process, with a particular focus on the interaction between the paste and the screen.

**“A nominal finger width  $w_n = 15\mu\text{m}$  is still challenging for a reliable solar cell metallization using a single-step screen-printing process.”**

Initial results have indicated that the wall slip behaviour of the paste can be significantly improved by adapting the screen chemistry, which allows a reduction in average finger resistances at reduced finger widths. A mean contact finger width  $w_{f0} = 26\mu\text{m}$ , combined with a mean finger resistance  $R_{\text{Finger0}} = 99\Omega/\text{m}$ , demonstrates the high potential of the newly developed screen chemistry using single-step screen printing. It was shown that contact fingers with a width  $w_f = 19\mu\text{m}$  and a height  $h_f = 18\mu\text{m}$  are possible in just one printing step; this outstanding result was achieved by using a 'knotless' screen (440/0.013/0°, nominal screen opening  $w_n = 15\mu\text{m}$ ).

Moreover, finger resistance  $R_{\text{Finger}}$  values well below  $1,000\Omega/\text{m}$  were obtained for nominal finger widths  $w_n$  down to  $15\mu\text{m}$ , which confirms the high potential of the single-step screen-printing process on the way to ultra-fine-line contacts in combination with multi-busbar cell layouts. PERC-type Cz-Si solar cells, fabricated with a five-busbar cell layout and a nominal screen opening  $w_n = 24\mu\text{m}$ , yielded maximum efficiencies  $\eta_{\text{max}}$  of up to 22.1%. The initial multi-busbar solar cells with an  $18\mu\text{m}$  nominal screen opening demonstrated a significant reduction in Ag.

**Acknowledgements**

The authors would like to thank all co-workers at the Photovoltaic Technology Evaluation Center (PV-TEC) at Fraunhofer ISE. This work was partly financed by the Federal Ministry of Economic Affairs within the framework of the FINALE project, funded under Contract No. 0324098B. The authors would also like to thank Koenen, Kissel + Wolf and Murakami for supporting this work.

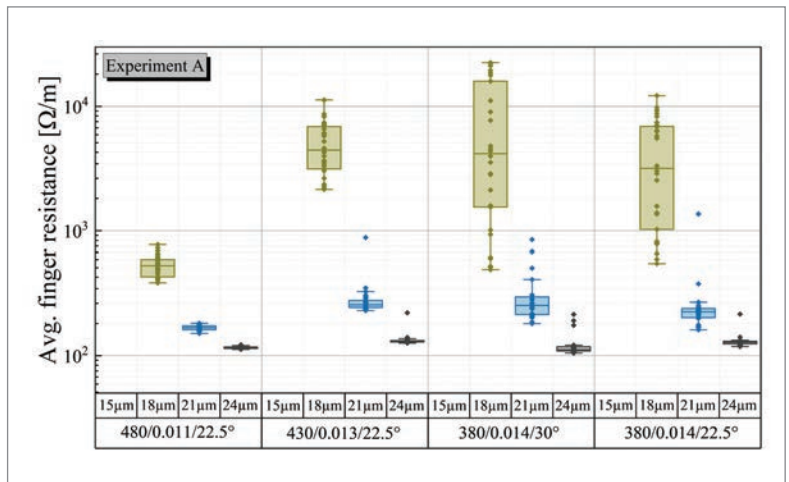


Figure 5. Finger resistance values obtained in the first test run with four different screens and four different nominal finger widths on each screen (see Fig. 1). The values for the nominal finger width  $w_n$  are shown above the corresponding screen parameters. For a nominal finger width  $w_n$  of  $15\mu\text{m}$ , no measurement is possible because of strong inhomogeneities along the printed fingers [4].

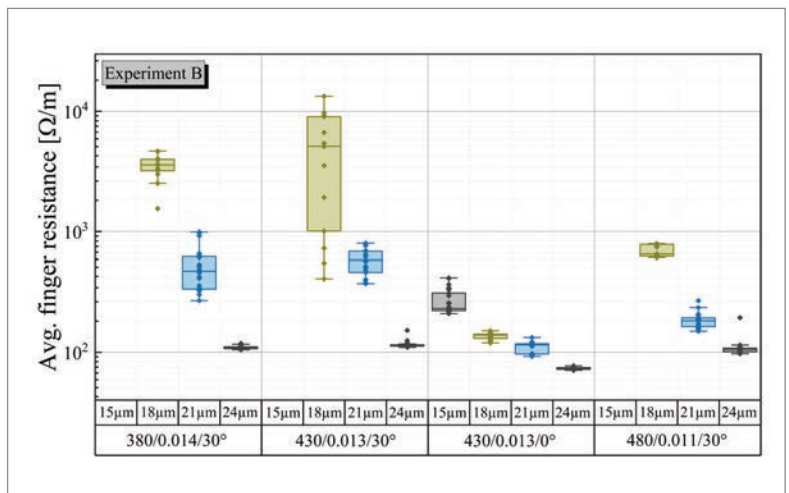


Figure 6. Finger resistance values obtained in the second test run with four screens and four different nominal finger widths on each screen (see Fig. 1). The values for the nominal finger width  $w_n$  are shown above the corresponding screen parameters [7].

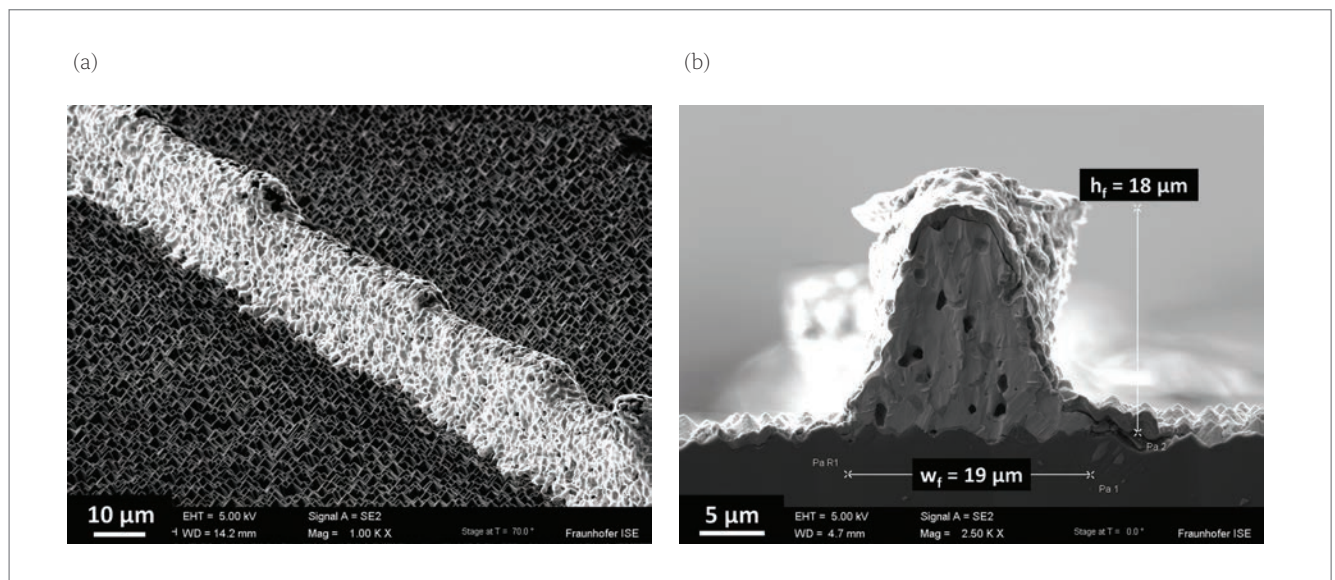
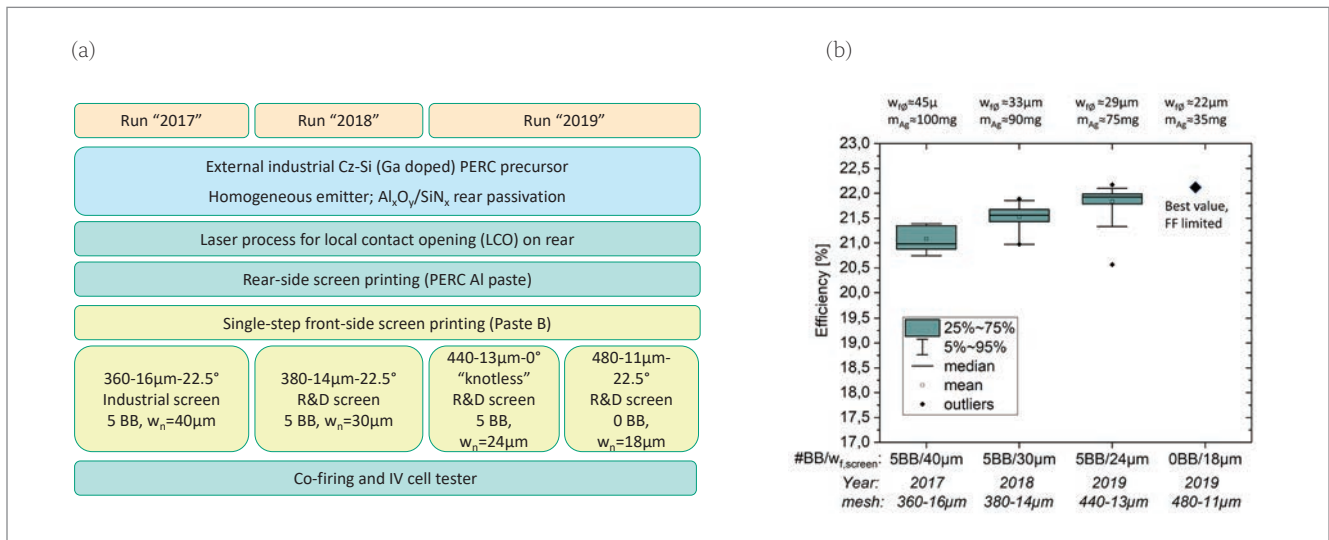
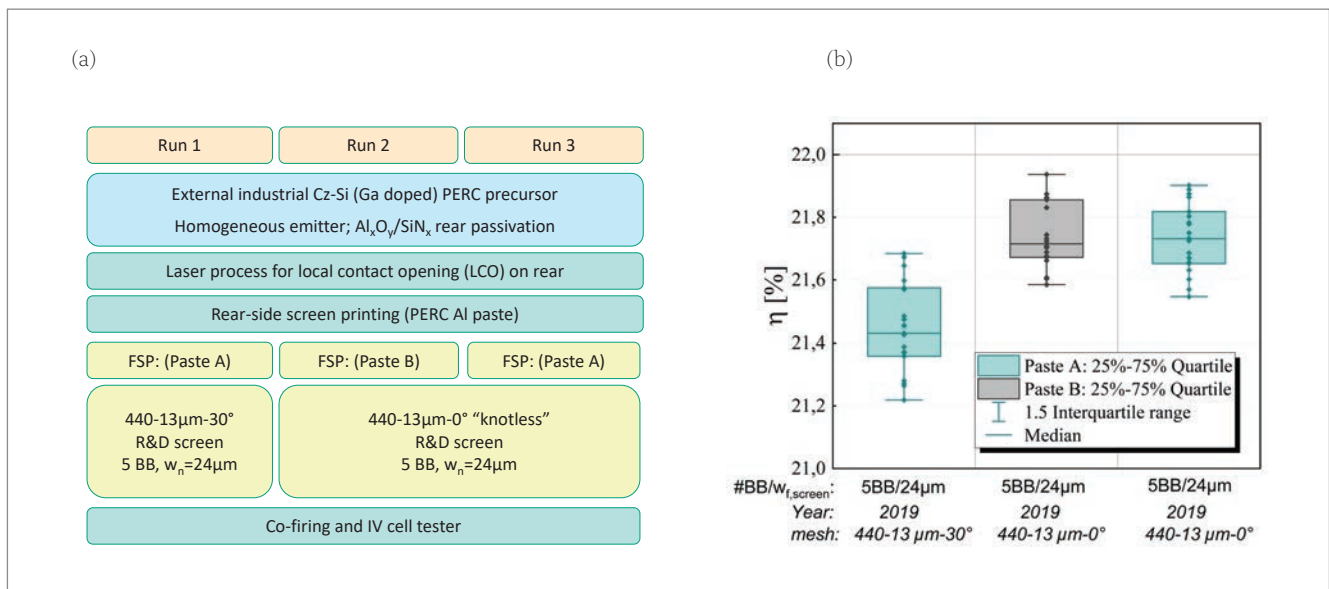


Figure 7. (a) SEM image of the electrodes printed with a 440/0.013/0° screen and a nominal finger width  $w_n = 15\mu\text{m}$ . An average aspect ratio of 0.9 at an average finger width of  $19\mu\text{m}$  was reported. (b) An angled tilted view of the printed finger, shown to illustrate the uniformity of the finger shape along the contacts by using this screen configuration [7].





**Figure 8. (a) Experiment process flow. (b) Cell efficiencies obtained for p-type Cz-Si PERC solar cells, as well as mean values for the finger widths and Ag consumption (paste lay-down, wet).**



**Figure 9. (a) Experiment process flow. (b) Cell efficiencies obtained for p-type Cz-Si PERC solar cells. The front-side finger grid was printed using two different screens and two different pastes. The 'knotless' 0° screen used here is the same one as in the first experiment (see Fig. 8).**

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**"The 'knotless' screen yields the best performance in terms of finger geometry and resistance."**

**About the Authors**



Dr.-Ing. Florian Clement is head of the Production Technology – Structuring and Metallization department at Fraunhofer ISE. He studied physics at the Ludwig Maximilian University of Munich and the University of

Freiburg and obtained his Diploma degree in 2005, followed by his Ph.D. from the University of Freiburg in 2009. His research focuses on new structuring and metallization technologies for silicon solar cells, in particular printing technologies. In 2019 he co-founded HighLine Technology GmbH, a Fraunhofer ISE spin-off.



Sebastian Tepner studied electrical engineering and information technology at the University of Bremen, Germany. Since 2016 he has been working at Fraunhofer ISE in the Production Technology – Structuring and Metallization department. His research focuses on process development for screen-printing applications and dispensing technology. He is currently working towards his Ph.D. in the field of screen-printing process modelling and simulation at Fraunhofer ISE.



Michael Linse studied print media technologies at Stuttgart Media University HdM and completed his bachelor thesis on advanced screen- and stencil-printing technologies for crystalline silicon solar cells in 2010 at Fraunhofer ISE. Since then, he has been working as a process engineer on screen-printing-related projects in the Production Technology – Structuring and Metallization department at Fraunhofer ISE.



Linda Ney received her Diploma degree in the field of renewable energy systems from the Technical University of Dresden. Since 2017 she has been working at Fraunhofer ISE, focusing on the optimization of screens for solar cell manufacturing. In 2019 she started her Ph.D., concerning the development of industry-related production processes for PEM-fuel cells, as well as ageing und stability studies of catalyst inks and pastes.



Noah Wengenmeyr studied energy and environmental technologies at the Kempten University of Applied Sciences, Germany. Since 2017 he has been working at Fraunhofer ISE in the Production Technology – Structuring and Metallization department. His research focuses on process development for screen-printing applications. Besides his work at Fraunhofer ISE, he is

**“The wall slip behaviour of the paste can be significantly improved by adapting the screen chemistry, which allows a reduction in average finger resistances at reduced finger widths.”**

a master’s student in sustainable systems engineering at the Albert Ludwig University of Freiburg.



Dr.-Ing. Maximilian Pospischil studied mechanical engineering at the Technical University of Munich (GER) and Delft (NL), and received his Diploma degree from the TU Munich in 2009. In 2010 he joined Fraunhofer

ISE in Freiburg as a Ph.D. student, focusing on the development of an industrial multi-nozzle dispensing technology for solar cell front-side metallization, and was awarded his Ph.D. in 2016 by the University of Freiburg. Since then he has been head of the Dispensing Technology team. In 2019 he co-founded HighLine Technology GmbH, a Fraunhofer ISE spin-off.



Dr.-Ing. Andreas Lorenz is head of the Printing Technology group at Fraunhofer ISE. After receiving his Diploma degree in 2006, he worked six years as a research engineer and junior product manager for a global machine manufacturer. In 2012 he joined Fraunhofer

ISE and worked on the development of rotary printing processes for solar cells. He received his Ph.D. in 2018 and since then has been responsible for leading several research projects in the field of solar cell metallization.




Dr. Ralf Preu is director of the PV Production Technology division at Fraunhofer ISE. He studied physics at the Universities of Freiburg and Toronto, and economics at the University of Hagen, Germany, and holds a Ph.D. in electrical engineering. He joined Fraunhofer ISE in 1993 and has worked in various fields in PV, including system monitoring, silicon solar cell and module technology, characterization and simulation. His main focus is R&D of advanced silicon solar cell technology and its transfer to industrial production. He teaches photovoltaics at the University of Freiburg.

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**Enquiries**

Florian Clement  
 Fraunhofer Institute for Solar Energy Systems ISE  
 Heidenhofstraße 2  
 79110 Freiburg, Germany

Tel: +49 (0)761 4588 5050  
 Email: florian.clement@ise.fraunhofer.de



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# Plating for passivated-contact solar cells

Sven Kluska, Thibaud Hatt, Benjamin Grübel, Gisela Cimiotti, Christian Schmiga, Varun Arya, Bernd Steinhäuser, Frank Feldmann, Jonas Bartsch, Baljeet Singh Goraya, Sebastian Nold, Andreas A. Brand, Jan Nekarda, Markus Glatthaar & Stefan W. Glunz, Fraunhofer Institute for Solar Energy Systems ISE, Freiburg, Germany

## Abstract

Passivated-contact solar cell designs, such as TOPCon or silicon heterojunction solar cells (SHJs), enable cell efficiencies greater than 24%, and are promising candidates for the next revolution in mass production after the passivated emitter and rear cell (PERC). Plated metallization (Ni/Cu/Ag or Cu/Ag) fits well with new constraints on low-temperature processing and the combination of low material costs and highly conductive bifacial metal grids for these types of solar cell. For TOPCon solar cells the combination of bifacial laser contact opening (LCO) and Ni/Cu/Ag plating allows highly conductive grid lines with low contact resistivities for a boron emitter on the front side and TOPCon on the rear side. LCO achieves low contact recombination, which enables further reduction of the TOPCon layer thickness. Bifacially plated i-TOPCon solar cells were fabricated at Fraunhofer ISE, achieving maximum cell efficiencies of up to 22.7% with significantly reduced cost of ownership (COO) compared with bifacial screen-printing metallization. Plating has always been considered a highly interesting option for metallizing SHJ solar cells. Many research groups (ISE, CSEM, ASU, UNSW) and companies (Sunpreme, Kaneka) are working on plating development, while GS Solar already uses plating in production. Fraunhofer ISE has established an innovative process sequence called *NOBLE* (native oxide barrier layer for selective electroplating), which allows bifacial plating of SHJ cells. The NOBLE sequence includes physical vapour deposition (PVD) of metal seed layers, which enable reliable mechanical and electrical contact, homogeneous plating current distributions/heights and low COO.

## Introduction

The PV industry passed a milestone in recent years, in migrating from multicrystalline aluminium back-surface field (Al-BSF) technology to the mono passivated emitter and rear cell (PERC) design. This technology shift was made possible by continual wafer, cell and module technology improvements and significant reductions in production cost for PERC technology. Furthermore, the Al-BSF design has reached its solar cell efficiency limitations, in contrast to the still steeply rising cell-efficiency learning curve for industrial PERC technology; the range of the efficiency potential of PERC solar cells is estimated to be 24% [1]. Passivated-contact solar cells – such as tunnel oxide passivated-contact (TOPCon) [2] and silicon heterojunction (SHJ) cells – are promising candidates for enabling solar cell efficiencies to be achieved in mass production

beyond the efficiency limit of PERC. Various research institutes and solar cell manufacturers have in fact already demonstrated solar cell efficiencies beyond 24%. This technology transition will most likely occur with a migration from p-type to n-type mono wafers.

Passivated-contact solar cells are already achieving high cell efficiencies, and have been well established for many years in mass production at various solar cell manufacturers (SunPower, Panasonic, Sunpreme, ...). However, a major task in passivated-contact solar cell development is to further decrease production costs. Back-end processes are a significant cost driver for TOPCon and SHJ solar cells. Screen printing is the conventional and well-understood metallization technology employed for PERC solar cells, and is also typically used for metallizing TOPCon and SHJ solar cells. The bifacial grid design, which is common for these solar cell types, significantly increases the material costs, now that silver (Ag) or silver–aluminium (AgAl) pastes must be printed on the front and rear sides of the solar cell in order to also achieve low grid resistances on the rear side. If increasing PV growth is forecast to a TW market scale, the silver consumption turns out to be a massive cost driver for solar cell production (1TW would use 100% of today's annual worldwide Ag production [3]).

Replacing Ag with copper (Cu) would enable raw material costs to be reduced by a factor of 100. The plating of Cu or stacks of Ni/Cu/Ag is a well-known technology in the PV industry. This paper shows in the following sections that Cu-plated contacts align well with all back-end technology requirements of TOPCon and SHJ solar cells. Plating technology holds the potential to significantly reduce production costs for passivated-contact solar cells. The main advantages of Cu-plated contacts for these solar cell designs are:

- Low cost of ownership (COO)
  - Low material costs
  - Synergetic cost reductions, such as TOPCon thickness reduction
- Compatibility with existing mass-production back-end tool equipment
- Potential for efficiency gains
  - Narrow contact width

**“A major task in passivated-contact solar cell development is to further decrease production costs.”**

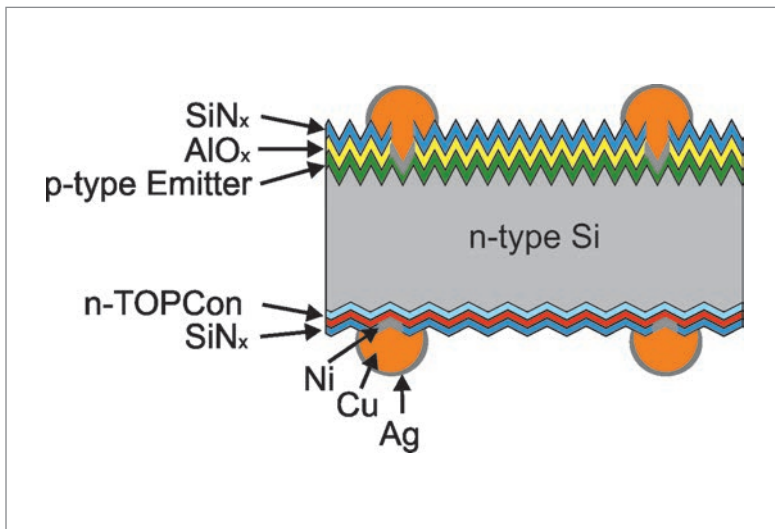


Figure 1. Schematic of a TOPCon solar cell with bifacially plated Ni/Cu/Ag contacts.

- o Highly conductive finger at low process temperatures
- o Low contact resistance and contact recombination

#### Plating metallization for TOPCon solar cells

Bifacially plated Ni/Cu/Ag metal contacts can help to further reduce manufacturing costs and increase the cell efficiency of industrial TOPCon (i-TOPCon)

solar cells. The replacement of Ag with low-cost Cu as the main conducting material enables a reduction in the back-end production COO for bifacial solar cells with metal grid patterns on both sides.

A robust process sequence for plated contacts on PERC solar cells has been developed over the last few years [4,5]. The combination of laser contact opening (LCO) and inline plated Ni/Cu/Ag has allowed high-quality contact properties with low COO for PERC solar cells using existing mass-production tools. The implementation of plated Ni/Cu/Ag contacts for bifacial TOPCon solar cells is based on these developments. The technological benefits of LCOs and plated Ni/Cu/Ag are:

- Low contact resistivities on n-type TOPCon layers and lightly boron-doped emitter
- Low contact recombination on
  - o TOPCon: allows further reductions in TOPCon thickness, because of shallow laser-damage depth
  - o boron emitter: enables  $V_{oc}$  improvements
- Narrow contact width (<25 $\mu$ m) with low line resistivity

The concept of the n-type TOPCon solar cell was introduced by Feldmann et al. in 2013 [6]; it features a boron-doped front-side emitter and a

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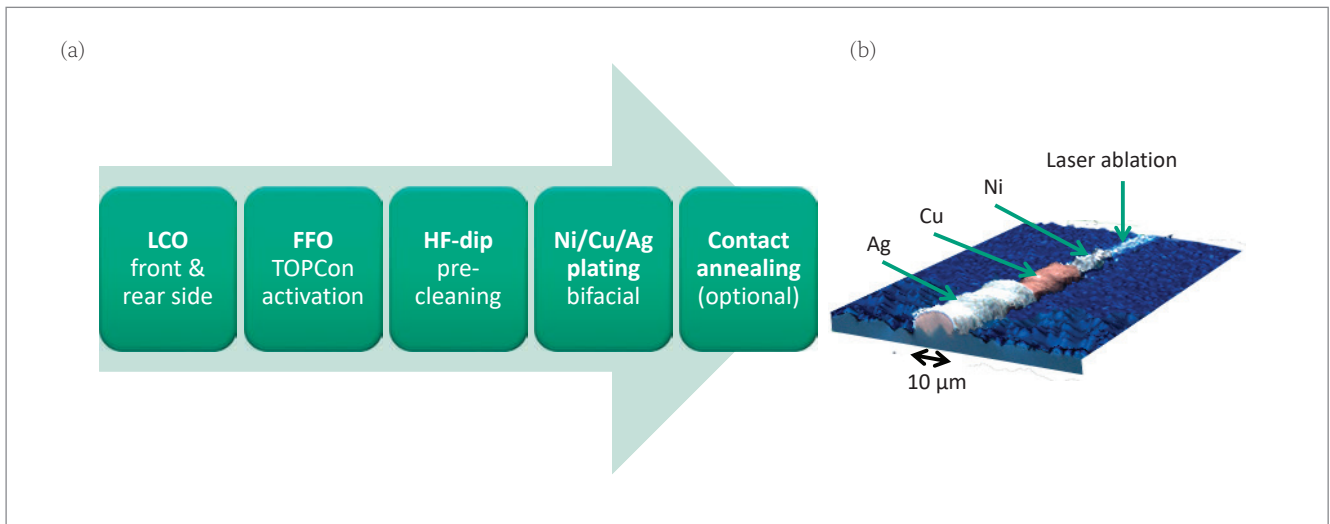
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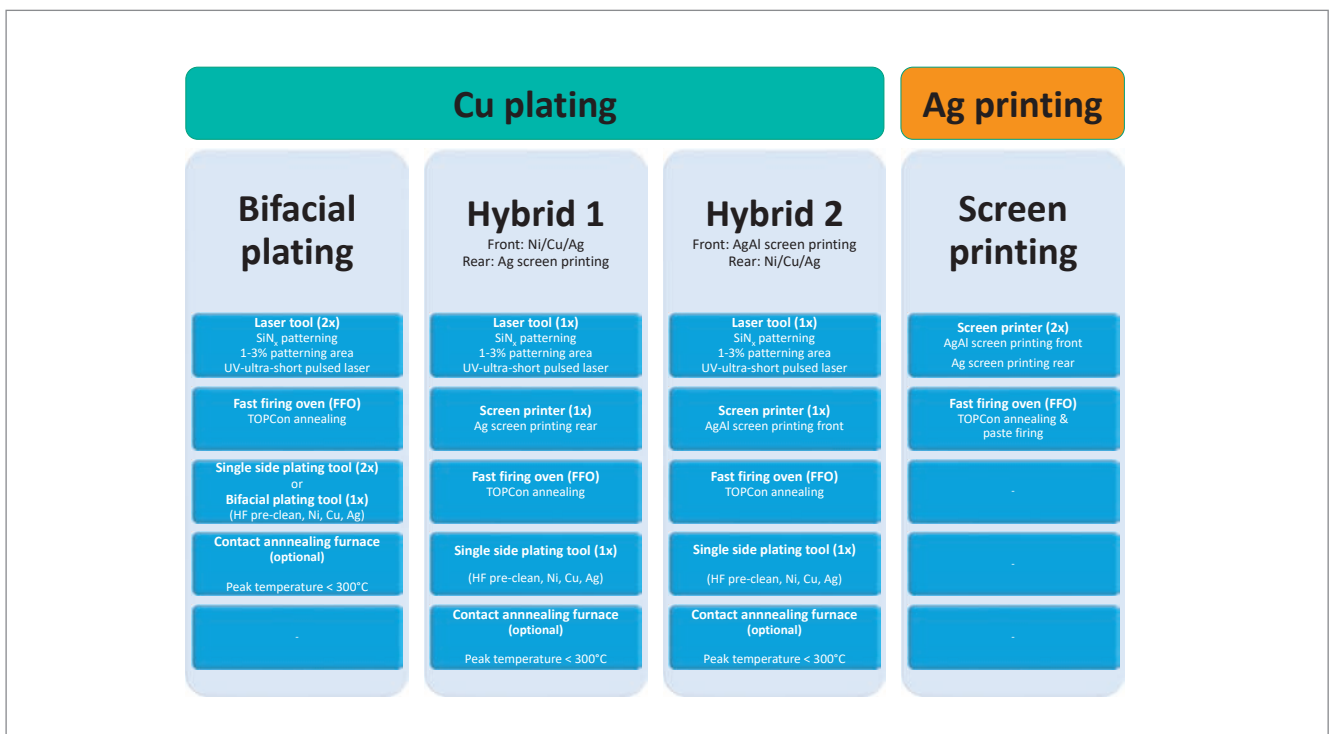
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**Figure 2. (a) Back-end process flow for bifacially plated TOPCon solar cells. (b) Composite microscope image of the contact finger after LCO, Ni (1μm), Cu (10μm) and Ag (0.5μm) plating.**



**Figure 3. Overview of back-end solutions for i-TOPCon solar cells with plated Ni/Cu/Ag contacts.**

passivated contact on the rear side. Since the first introduction of this technology, the definition of industrially feasible process sequences was the main focus for technology developments, starting from PECVD, LPCVD and sputter developments for TOPCon deposition, and then moving on to metallization processes that enable high cell efficiency and low COO.

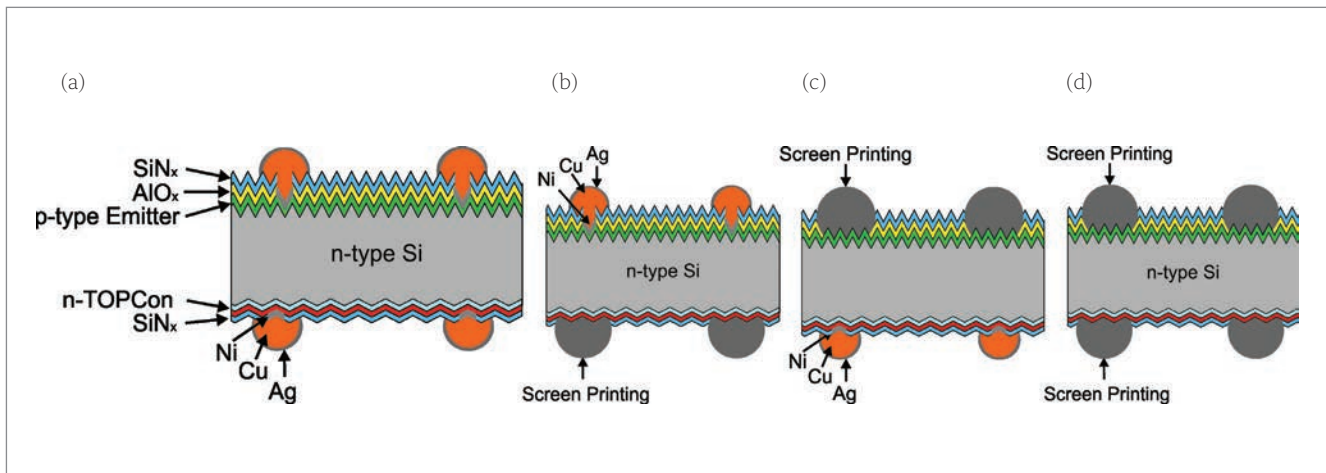
The metallization of i-TOPCon solar cells poses new challenges compared with Ag or Al screen-printing processes in the well-understood PERC process sequence. Low contact recombination (preferably using thin TOPCon layers), low contact resistivities (on boron-doped emitters and TOPCon layers), narrow finger width and low

COO are desired. In particular, the combination of low contact resistivities and the avoidance of spiking through the TOPCon layer turns out to be a major topic for screen-printing metallization [7]. The combination of laser structuring and plated Ni/Cu/Ag is a viable alternative in the ongoing developments of screen-printed i-TOPCon solar cells [8,9].

**Process sequence and back-end solutions**

Plated contacts for passivated-contact solar cells were introduced in recent years by companies such as SunPower and Tetrasun [10]. The first introduction of plated contacts in TOPCon solar cells at Fraunhofer ISE were aimed at contacting





**Figure 4. Schematics of i-TOPCon solar cells: (a) with bifacially plated Ni/Cu/Ag contacts; (b, c) hybrid designs (Hybrid 1 and Hybrid 2) with plated and screen-printed contacts; (d) with screen-printed contacts.**

		$V_{oc}$ [mV]	$J_{sc}$ [mA/cm <sup>2</sup> ]	$\eta$ [%]	FF [%]	pFF [%]
Screen printing	Best	690	39.9	22.7	82.3	83.5
	Average	686	39.9	22.4	81.8	83.4
Hybrid 1	Best	692	40.3	22.7	81.6	83.4
	Average	688	40.3	22.7	81.8	83.4
Hybrid 2	Best	689	39.8	22.4	81.8	83.0
	Average	688	39.8	22.3	81.4	83.3
Bifacial plating	Best	690	40.4	22.7	81.4	83.5
	Average	687	40.3	22.4	80.7	83.1

**Table 1. Measured I–V parameters for i-TOPCon solar cells (masked measurement area 145×145mm<sup>2</sup>, total cell area 158.75×158.75mm<sup>2</sup>).**

the boron-doped emitter to enable cell efficiencies of up to 23.4% [11]. These attempts were followed by the introduction of laser-defined plated Ni/Cu/Ag contacts on both sides for bifacial i-TOPCon solar cells [12]. Fig. 1 illustrates the design of an i-TOPCon solar cell with bifacially plated Ni/Cu/Ag contacts.

The back-end process sequence for TOPCon solar cells with metal-plated contacts developed at Fraunhofer ISE is shown in Fig. 2(a). The plated contacts are defined by local laser ablation of SiN<sub>x</sub> anti-reflection coatings (ARC) using ultrashort pulse laser systems. The combination of UV-ps laser systems and textured surfaces guarantees reliable contact adhesion because of the laser-induced nano-roughness on the pyramid sides [13,14]. TOPCon layer activation can be performed by fast-firing oven (FFO) annealing after laser ablation. The FFO activation can also be exploited as laser-damage annealing in order to further reduce contact recombination [15]. HF pre-cleaning before plating removes the process-induced and native oxide layer to ensure clean silicon–nickel contact interfaces.

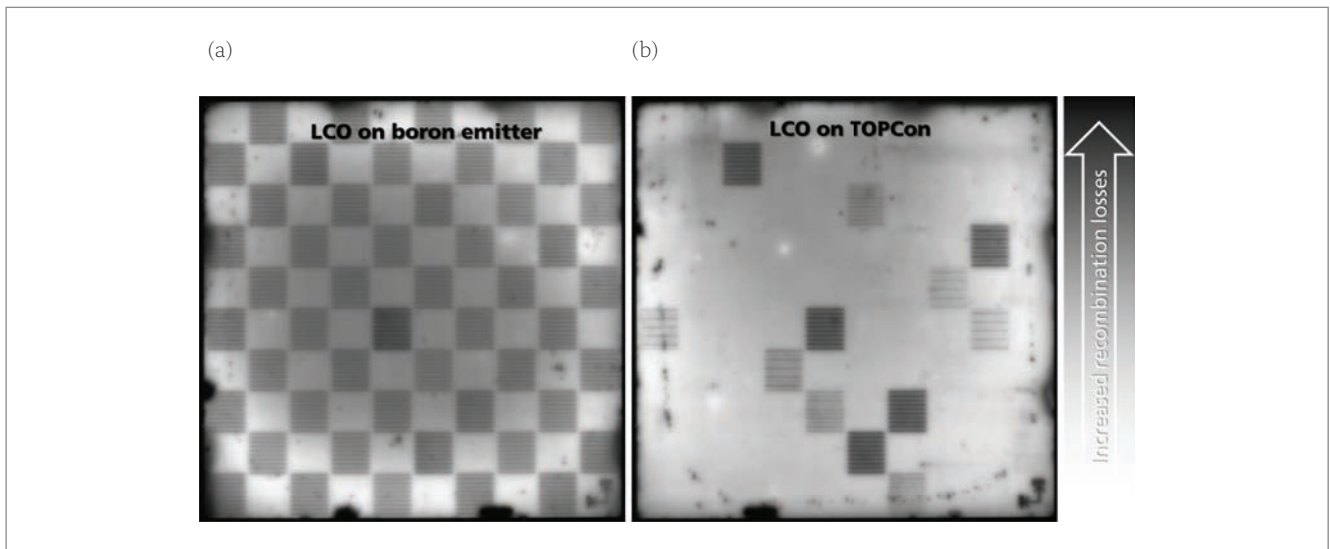
Various plating tool designs (inline plating, batch plating) are applicable to bifacially plated TOPCon solar cells. The solar cells presented in this work are plated using an inline plating process of a thin Ni interface layer (<1μm), a Cu (1–10μm) layer, and an Ag surface finish (<0.5μm). Only electroplating processes – such as light-induced [16], forward bias

[17] or direct contact plating [18] – were used to deposit the metal layers. Fig. 2(b) shows a composite microscope image of the contact finger cross section after each process step.

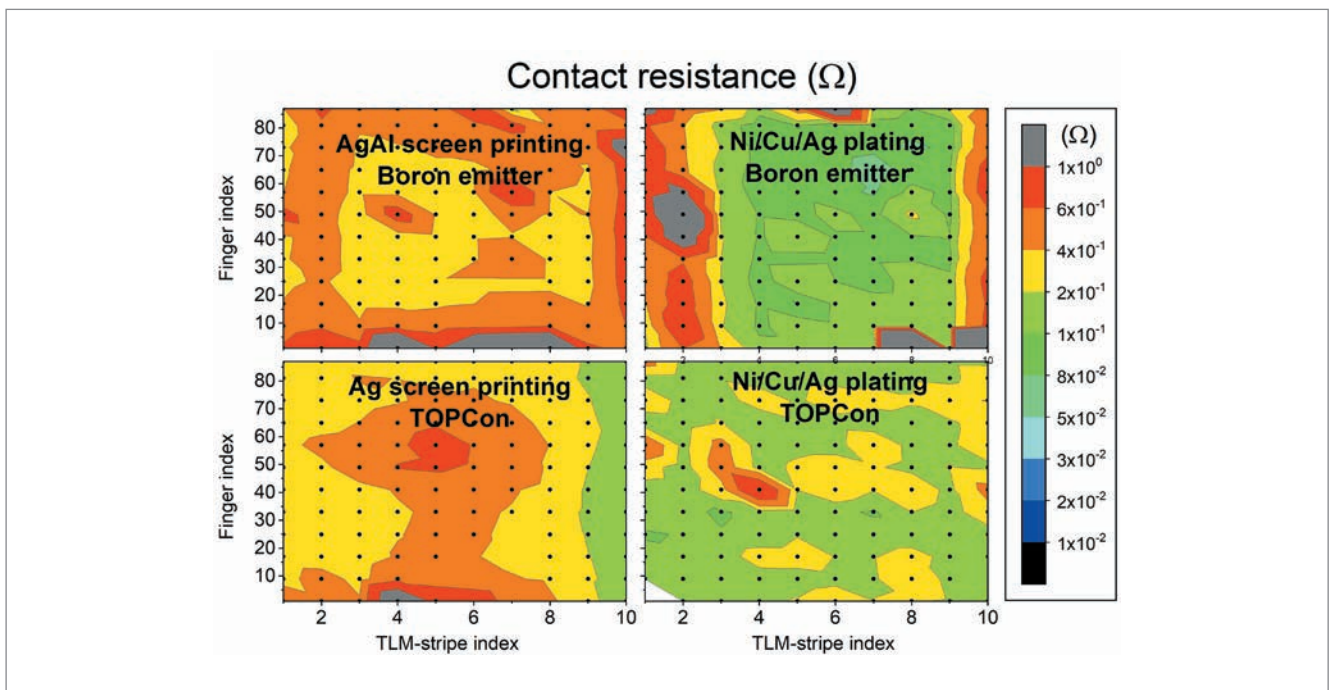
The process sequence shown in Fig. 2 is an industrially feasible approach for integrating plated Ni/Cu/Ag metal contacts in i-TOPCon solar cells. The contact metallization can be either a bifacially plated contact design or a combination of plated and screen-printed contacts. Fig. 3 shows three back-end sequences with metal-plated contacts on the boron-doped emitter, on the TOPCon, or on both sides. The *Hybrid 1* and *Hybrid 2* designs refer to combinations of screen-printed and plated contacts on either side of the solar cell.

### Solar cell integration and contact characteristics

Industrially manufactured i-TOPCon precursors without metallization were used to demonstrate plated i-TOPCon solar cells employing the four back-end processing options shown in Fig. 3. The precursors were taken out of the regular mass-production line and optimized for screen-printed metallization. There were no specific changes in design or in processing for all the precursors before metallization. The reference group with bifacially screen-printed metal contacts was fully processed at the manufacturer's site; for the hybrid approaches,



**Figure 5.** PL measurements for characterizing the contact recombination of samples with lasered test fields of LCO variations: (a) on the boron-doped emitter; (b) on TOPCon. Note that the same LCO parameter variation was performed on both images, but only parameters with high laser powers are visible in the case of TOPCon.



**Figure 6.** Measured contact resistance mapping of cut i-TOPCon precursors ( $158.75 \times 158.75 \text{ mm}^2$  cut into 10 strips) with boron-doped emitter or TOPCon layers and either screen-printed or metal-plated contacts. The black dots represent the positions of the TLM measurements. Note the difference in mean contact width of  $40 \mu\text{m}$  for screen printing and  $25 \mu\text{m}$  (LCO width:  $18 \mu\text{m}$ ) for plating.

the screen printing and firing/TOPCon activation was also covered by the manufacturer.

The plating metallization for all process groups with metal-plated contacts was realized at Fraunhofer ISE, as was the TOPCon activation of the bifacial plating precursors. Since the FFO/TOPCon activation process at Fraunhofer ISE was not optimized for these precursors, the implied  $V_{oc}$  (the cell  $V_{oc}$  potential before metallization) was about 5–10mV below that of the optimized FFO/TOPCon activation process at the manufacturer’s site.

Table 1 shows the measured  $I-V$  parameters of the fabricated i-TOPCon solar cells (see Fig. 4). The measurements were performed using a  $145 \times 145 \text{ mm}^2$

shadow mask because of edge artefacts due to shipping and manual handling. All the processed groups yield mean cell efficiencies between 22.3 and 22.7%. The best screen-printing reference achieves a solar cell efficiency of 22.7%, while the best back-end groups Hybrid 1 and 2, with combinations of screen printing and plating, yield cell efficiencies of 22.4% and 22.7%, respectively. The more detailed analysis in the following sections reveals that,

**“The application of LCO patterning and Ni/Cu/Ag plating enables the creation of ultrafine-line contacts for i-TOPCon solar cells.”**

even for the hybrid groups, the reduced contact recombination and narrower contact width seem to enable improvements in  $V_{oc}$  and  $J_{sc}$ . However, these improvements are statistically not significant in this experiment because of the small sample/group size and the wide spread of the results in each group.

The bifacially plated group demonstrates a best cell efficiency of 22.7%. The decreased shading fraction due to the narrow contact width of 25 $\mu$ m leads to increased  $J_{sc}$  compared with the process groups with screen-printed front-side contacts.

#### Reducing contact recombination/enabling thinner TOPCon layer

Since the precursor design for the fabricated solar cells is already optimized for the application of screen-printed contacts, the TOPCon layer thickness is sufficient to prevent metal spiking for screen-printed contacts in the reference group.

Photoluminescence (PL) imaging, shown in Fig. 5, was carried out on the same precursor material to further analyse the contact recombination due to laser-induced damage by the LCO process. A large laser parameter variation was performed with increasing laser power, starting from the threshold power, to properly ablate the SiN<sub>x</sub> capping layer. The recombination due to laser damage is observed in the PL image by the darkening of the LCO test fields. The darkened areas are visible on the boron emitter side, independently of the applied laser power. In contrast to that, only a few test fields

with large laser powers are darkened on the sample, where LCO was performed on the TOPCon side. This demonstrates that only large laser powers well above the ablation threshold induce contact recombination on this industrially optimized TOPCon layer thickness. Consequently, even lower TOPCon thicknesses would be possible without increasing contact recombination. Similar findings of Haase et al. [19] identified a reduction of the poly-Si thickness down to 75nm to be sufficient for damage-free laser contact openings with UV-ps laser systems. The boron-doped emitter contact recombination increases, as expected, when passivation layers are removed from diffused crystalline silicon surfaces.

#### Reducing contact resistance

Earlier publications have already demonstrated contact resistivities below 1m $\Omega$ cm<sup>2</sup> for plated Ni/Cu/Ag contacts on lightly boron-doped emitters (with surface doping concentration less than 10<sup>19</sup>cm<sup>-3</sup>,  $R_{sheet} = 140\Omega/sq$ ) [20] and n-type TOPCon layers [12]. Random samples of the fabricated i-TOPCon solar cells were further characterized in order to determine the contact resistance. The samples were cut into strips of 1cm, and measured using transmission line measurements (TLMs); the strips were mapped over all the fingers on each strip.

The summarized contact resistance measurements are shown in Fig. 6. The plated contacts feature decreased finger widths down to

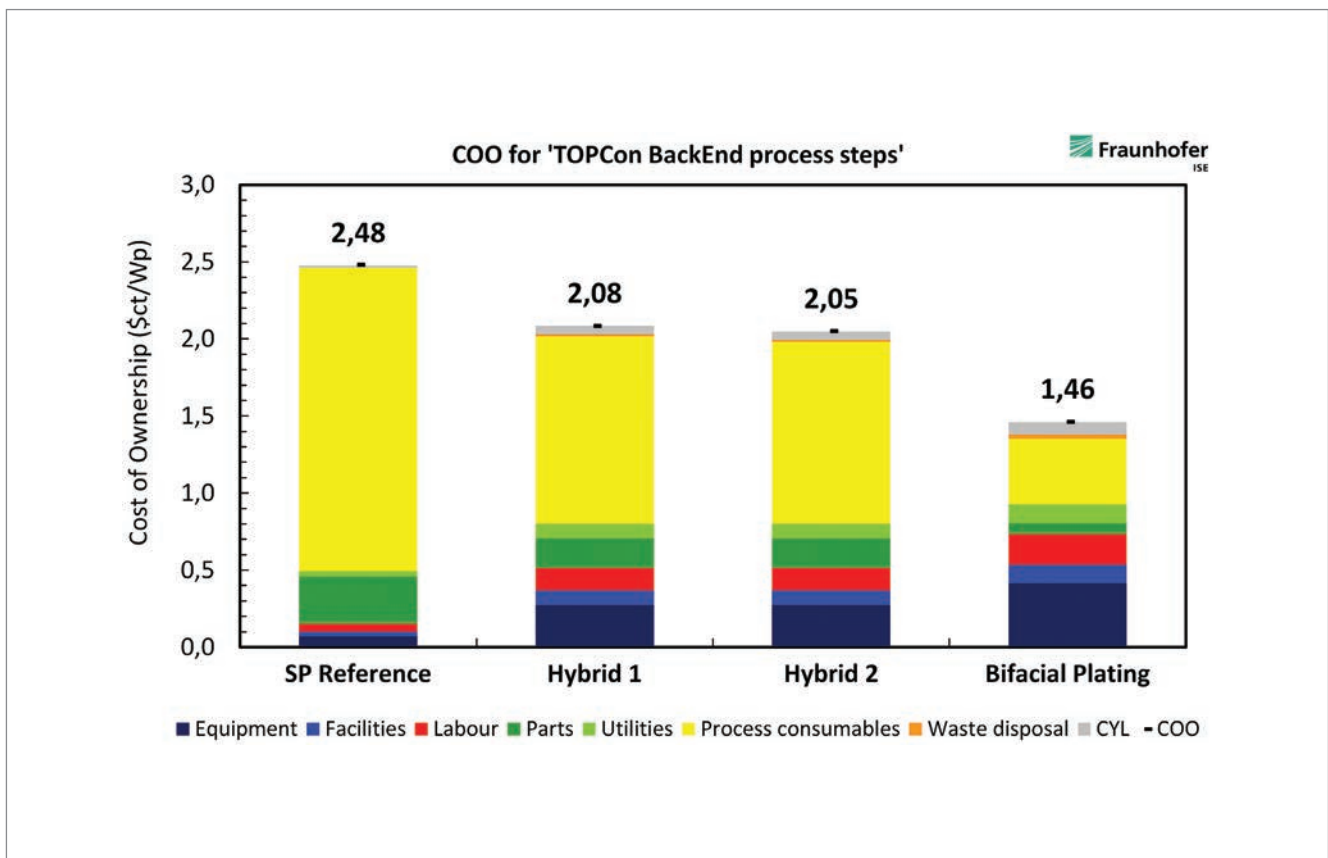


Figure 7. COO calculations for the four back-end process sequences given in Fig. 3.



25µm compared with 40µm for screen printing. For plated contacts, the contact resistance is limited by the Ni–Si interface area, which is defined by the LCO width (18µm). Although the plated fingers have only half the contact/interface width, the measured contact resistance in Fig. 6 is below the values for screen printing for both surface types (boron emitter/TOPCon).

**Reducing shading losses by means of highly conductive ultrafine-line contacts**

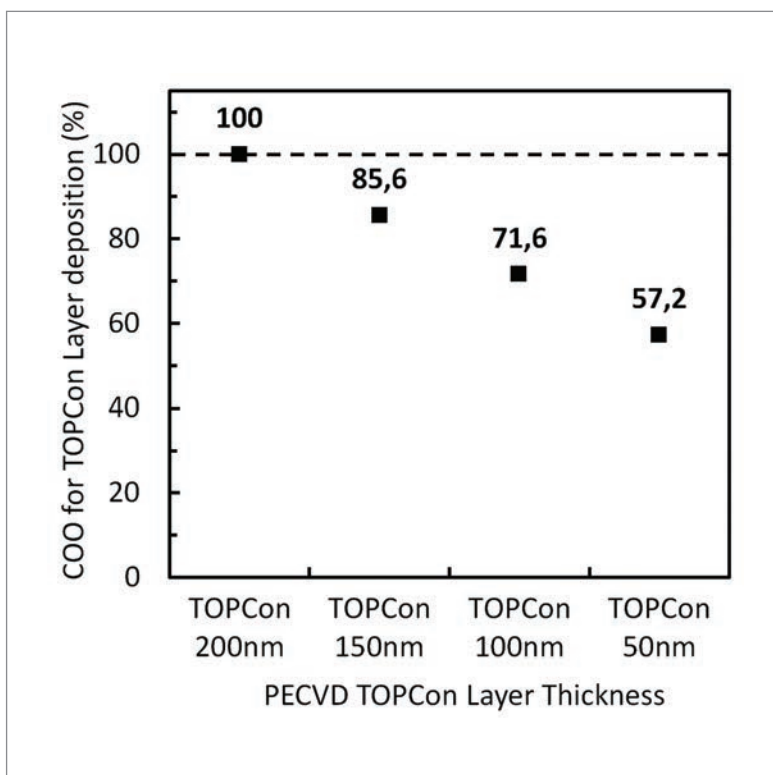
The application of LCO patterning and Ni/Cu/Ag plating enables the creation of ultrafine-line contacts for i-TOPCon solar cells. State-of-the-art mass-production LCO tools allow contact opening widths of 12–18µm, while lab-type tools allow even lower LCO widths, which are below 5µm and limited by the pyramid texture size.

The plating width is scalable by the amount of metal plating. Assuming isotropic growth, the width can be approximated by the LCO width plus twice the plating height. After contact annealing [21], the conductivity of plated Ni/Cu/Ag layers is similar to the conductivity of bulk Cu. Measurements performed on plated Ni/Cu/Ag layers at Fraunhofer ISE show line resistivities of 17.3mΩmm<sup>2</sup>/m (compared with the value 17.21mΩmm<sup>2</sup>/m for Cu in the literature [22]). Depending on the interconnection design (number of busbars), these low line resistivities allow finger widths down to 25µm and finger heights of 5µm, without significant limitation by the grid resistance.

**Cost calculations**

Bifacial grid designs enable further cell efficiency gains for i-TOPCon solar cells. Besides the benefits of bifacial grid designs, however, there are also increased requirements concerning the line conductivity of the rear-side metallization. For both-side screen-printed solar cells, this leads to the need for high Ag lay-down on the front and rear sides. The introduction of plated Ni/Cu/Ag contacts in a bifacial grid design therefore allows material costs to be drastically reduced. In combination with the potential for efficiency gain discussed above, bifacially plated Ni/Cu/Ag metallization for i-TOPCon solar cells may be the most promising approach for metallization.

To evaluate the COO of the back-end processes described in Fig. 3, advanced cost calculations using the SCost modelling approach [23] were performed; these calculations assume TOPCon solar cells with a bifacial grid design. A paste lay-down of 90mg per wafer side (180mg/wafer paste lay-down) is assumed for the screen-printing reference. The front side (boron-doped emitter) and rear side (TOPCon) are metallized with fire-through AgAl and Ag pastes, with assumed Ag content of 88% and 92%, respectively. The paste costs are dominated by the Ag raw material cost, and so other contributions to costs are not significant.



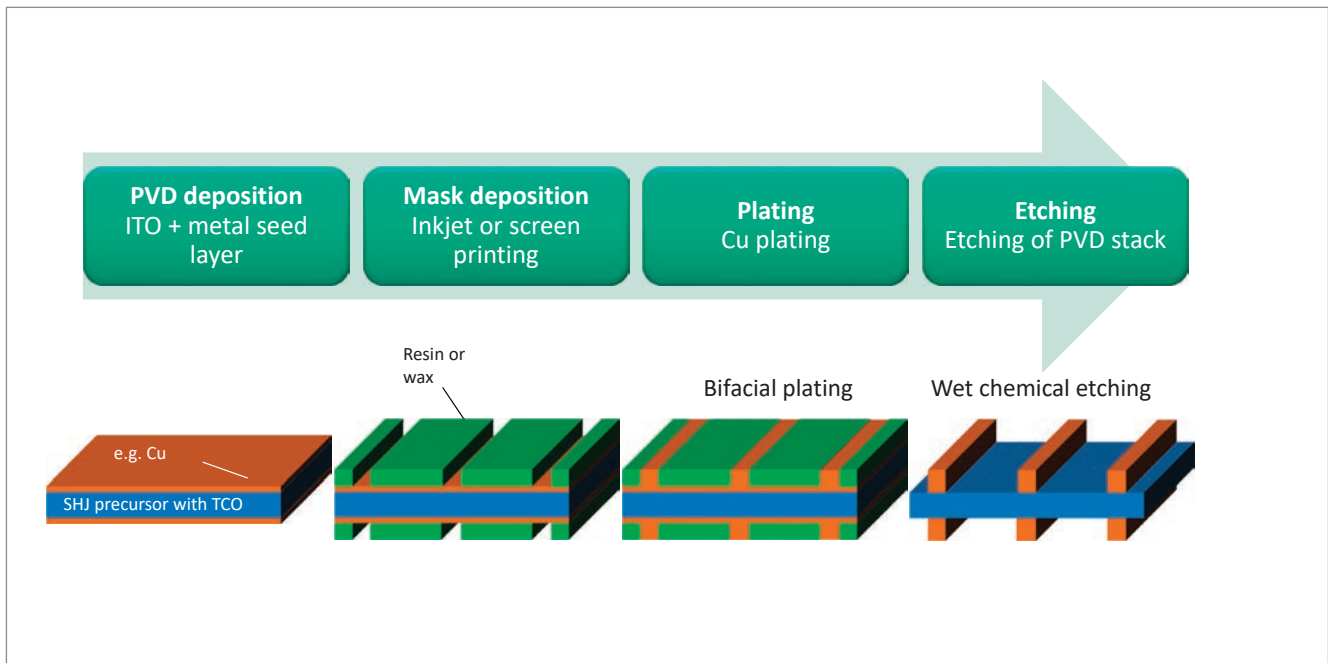
**Figure 8. Normalized COO of the PECVD TOPCon process with decreasing TOPCon layer thickness.**

**“Decreasing the TOPCon layer thickness from 200nm to 50nm can reduce the COO of the TOPCon process by 43%.”**

The assumptions for the plating equipment are fairly conservative. The lead gained in screen-printing tool development compared with plating is taken into account by the increased investment costs, reduced throughput and higher labour costs for plating. The equipment throughputs are assumed to be 7,200 wafer/h and 5,000 wafer/h for screen printing and plating, respectively. The lower throughput of plating is not based on technological restrictions but on the lack of scaling effects compared with the tool developments in screen printing over the last decade.

Fig. 7 shows the COO ratios for each of the back-end sequences. The COO for bifacial plating indicates a benefit of more than 40% compared with the screen-printing reference. The major cost driver for the screen-printing reference process sequence is the process consumables (yellow) – i.e. the Ag and AgAl pastes. Introducing plating can dramatically decrease the raw material costs. Because of scaling effects over the last decade, the equipment costs for screen printing are significantly lower than those for young technologies, such as plating. With increasing market penetration, however, similar scaling effects are expected for plating.

The hybrid concepts demonstrate a cost benefit of more than 16% compared with the screen-printing reference process. The difference between the two hybrid designs is due to the different



**Figure 9. Back-end process sequence for plated SHJ solar cells using organic masking processes.**

paste costs in each: Hybrid 1 requires Ag pastes for contacting the TOPCon layer, compared with AgAl pastes for Hybrid 2. Overall, all the back-end sequences involving plating, whether it be hybrid or bifacial, allow drastic cost improvements as a result of lower consumable costs. In the case of an increasing market penetration of plated contacts for TOPCon solar cells, the scaling effects and improvements in throughput will lead to further reductions in equipment costs.

#### **Reducing TOPCon thickness to under 100nm**

The implementation of plated Ni/Cu/Ag for contacting TOPCon surfaces has the potential to enable the TOPCon thickness to be decreased without increasing contact recombination. Fig. 8 summarizes the cost calculations for bifacially plated TOPCon solar cells with different TOPCon layer thicknesses in terms of the normalized COO reduction; the figure shows the normalized COO of the TOPCon process for decreasing TOPCon layer thickness. It can be seen that decreasing the TOPCon layer thickness from 200nm to 50nm can reduce the COO of the TOPCon process by 43%.

#### **NOBLE – plated Cu metallization for Si heterojunction solar cells (SHJ)**

Plating has always been considered a highly interesting option for metallizing SHJ solar cells. The plating processes fit in very well with the strict constraints of low-temperature processing, as well as offering the possibility of realizing highly conductive Cu grid lines at low material

cost. Many research groups (e.g. PhG-ISE, CSEM, ASU, UNSW) and companies (e.g. GS Solar, Sunpreme, Kaneka, Silevo) are carrying out work on plating, while today's largest SHJ solar cell manufacturer, GS Solar, already uses plating in production.

The reason why plating is so interesting for SHJ solar cells is that these cells cannot withstand temperatures above  $\sim 250^{\circ}\text{C}$ . Hence, printing Ag pastes that are cured at a low temperature and with fairly low conductivity need to be used, which results in a high amount of silver being required per cell, especially in a bifacial cell design. The situation becomes even worse when the interconnection of the cells for module fabrication is considered: experience has shown that even greater amounts of silver need to be used to allow soldered interconnection technology. Alternative interconnection technologies, such as SmartWire Connection Technology (SWCT) or the use of electrically conductive adhesives (ECAs), enable the amount of printed silver to be reduced, but incur additional costs in module assembly, as these alternative interconnection technologies are more expensive.

A review of state-of-the-art plating processes for SHJ solar cells was published by Lachowicz et al. in 2018 [24]. The formation of locally plated contacts on transparent conductive oxide (TCO) surfaces requires masking of the non-grid areas; otherwise the entire TCO surface would be plated. Physical vapour deposition (PVD) of metal seed layers feature excellent adhesion on indium tin oxide (ITO) and help to uniformly distribute the plating current, allowing fast simultaneous bifacial plating. Therefore, the most common plating approach, shown schematically in Fig. 9, is:

**“The NOBLE sequence includes PVD metal seed layers for reliable contact adhesion on TCO, and homogeneous plating current distributions.”**

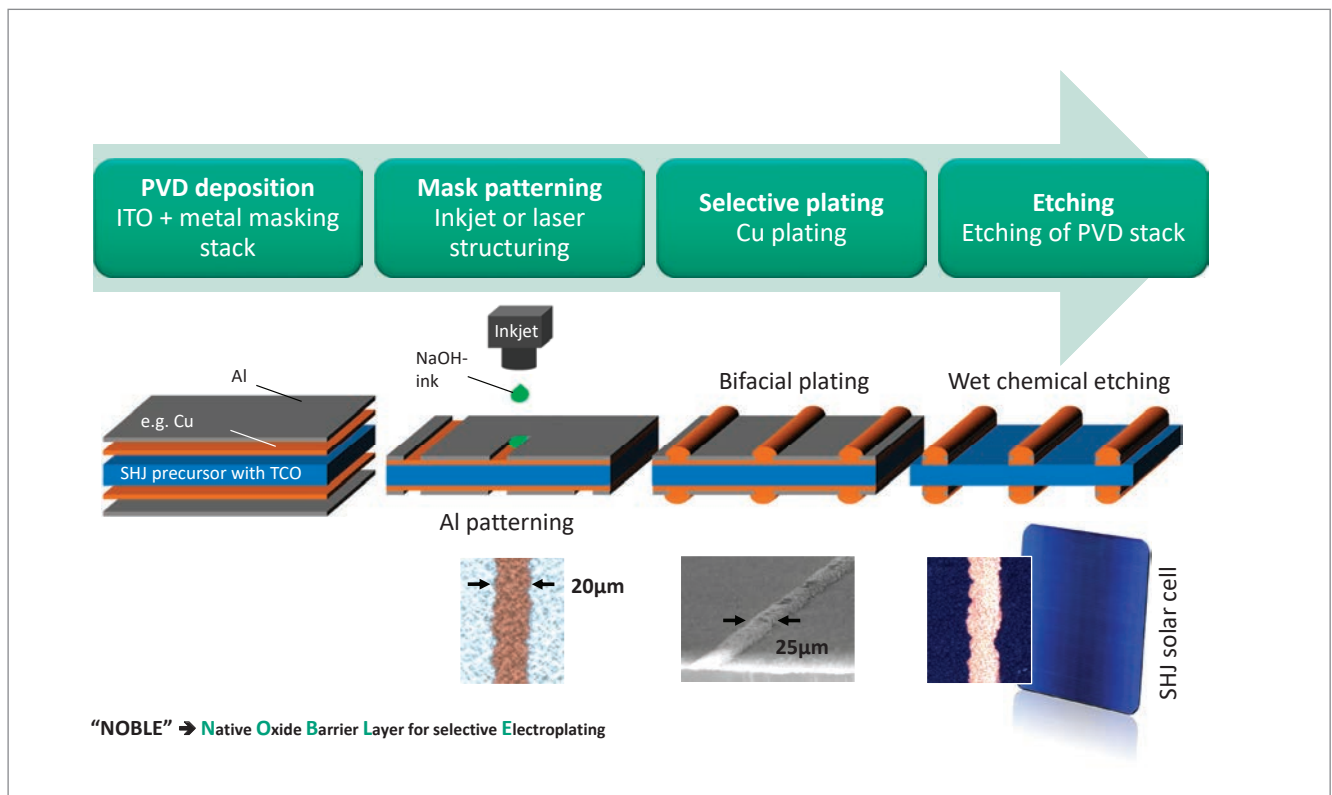


Figure 10. NOBLE process sequence for SHJ solar cells with bifacially plated Cu metallization.

- Deposit a full-area PVD metal seed layer on ITO
- Deposit a structured organic masking layer (e.g. resin or wax)
- Plate the contact grid
- Strip the masking layer
- Etch back the PVD seed layer

This approach is well established in printed circuit board (PCB) manufacturing, where photolithography with dry-film resists is typically used for masking. For solar cell applications, however, inkjet printing is often considered for depositing the mask. The fact that most of the area needs to be covered by the mask (~97%) leads to high consumable costs and lengthy processing times. To reduce consumable costs, a double-print process with a thin masking layer over most of the area, which is thicker close to the openings in the layer, has been introduced [25] and further developed [26]. This masking approach is still found in industrial production, but the treatment of waste water polluted with the organic masking material leads to high costs.

#### NOBLE process sequence and back-end solutions

At Fraunhofer ISE, the intention is to tackle the cost issues with an organic mask by means of the so-called *NOBLE* process (**n**ative **o**xide **b**arrier **l**ayer for selective **e**lectroplating) [27,28]. The NOBLE sequence includes PVD metal seed layers for reliable contact adhesion on TCO, and homogeneous plating current distributions.

Instead of an organic mask, an Al layer is deposited, which allows the use of the natively grown  $\text{AlO}_x$  surface in the subsequent plating processes as a non-conductive masking layer. Sandwiched between TCO and Al is a second thin metal layer, which can be freely chosen to optimize the seed layer contact interface properties (contact resistance, contact adhesion). Possible choices for this metal layer include Cu, Ag or Ni. The metal layers can be deposited by PVD in the same tool used for the TCO layers, but with the tool equipped with additional targets. The thickness of the metal layers is in the range 10–100nm.

The Al layer is structured by inkjet printing of alkaline ink [28], laser ablation, or laser-induced forward transfer (LIFT) [29]. The structuring step only requires patterning of the grid area, which is typically about 3% of the wafer surface. The subsequent plating process requires optimized plating electrolytes and reverse pulse plating in order to avoid parasitic plating on the oxidized aluminium surface [30,31]. Both these requirements are compatible, however, with state-of-the-art mass-production inline plating tools. In the final step, the PVD metal layers are chemically etched. The NOBLE process sequence is shown schematically in Fig. 10; all the required tools are available for mass production.

#### Solar cell integration and contact characteristics

One of the origins of NOBLE lies in the success of solar cells metallized by plating on PVD metal seed



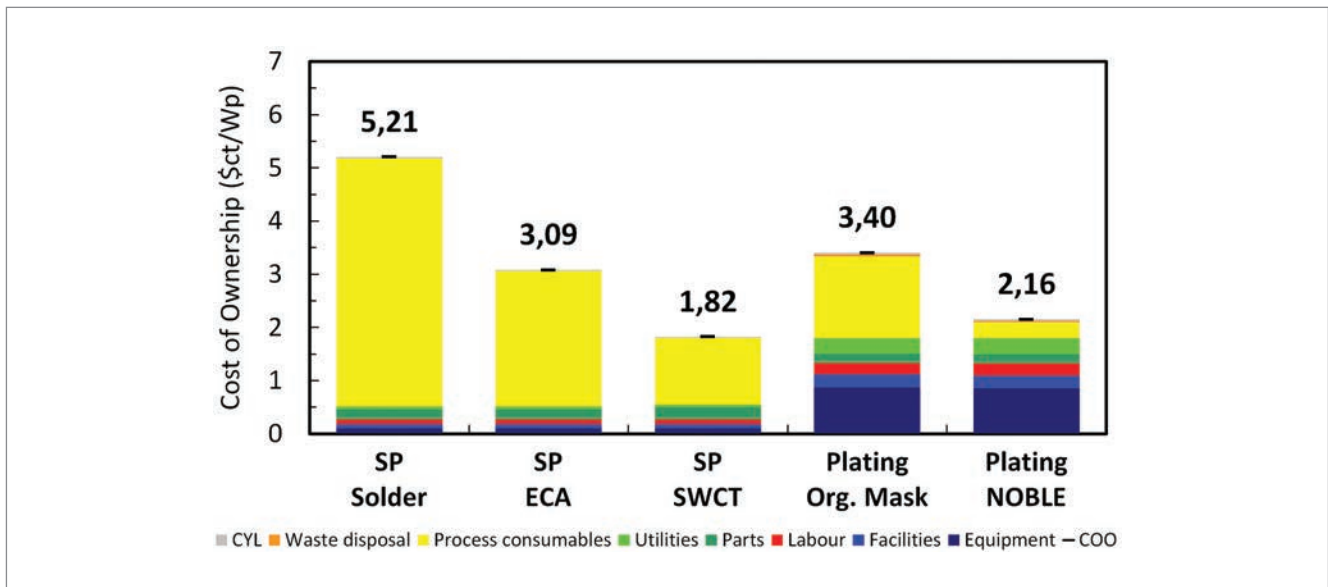


Figure 11. COO calculations for various metallization technologies used for bifacial SHJ solar cells (SP = screen printing). The contributions to the total COO (bold) include consumables and depreciation associated with the metallization processes.

“The integration of Cu-plated contacts can further decrease the production costs of passivated-contact solar cells.”

layers masked with an organic resist. Impressive results by CSEM [24] demonstrated solar cell efficiencies  $\eta$  of up to 24.7% with reliable module

interconnection using soldering or SmartWire interconnection. There is no reason to believe that with the NOBLE sequence, efficiencies similar to those with an organic mask could not be reached.

The contact resistance is defined by the PVD seed layer and proper interface conditioning before plating. The conductive full-area PVD seed layer allows homogeneous plating current distribution, which in turn enables homogeneous plating height

# PV Manufacturing & Technology Quarterly report



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Interconnection/ Metallization	Printing consumables	Paste or resist lay-down	Printing area (front+rear)
Soldering 5BB			
Ag screen printing	Low-curing Ag paste	365mg/wafer	11.4%
ECA 5BB			
Ag screen printing	Low-curing Ag paste	205mg/wafer	8.2%
SWCT			
Ag screen printing	Low-curing Ag paste	100mg/wafer	4.1%
Soldering 5BB			
Organic mask	Hotmelt ink	600mg/wafer	7.3%
Soldering 5BB			
NOBLE (inkjet)	1% NaOH	0.7µl/wafer	7.3%
SWCT			
NOBLE (inkjet)	1% NaOH	0.7µl/wafer	4.1%

**Table 2. Consumables for the printing processes (Ag screen printing and mask patterning) for different metallization and interconnection approaches for SHJ solar cells.**

distribution over the entire wafer. The contact geometry for NOBLE is defined by the mask patterning width and isotropic growth around the mask opening.

The first demonstration of selective Cu plating for SHJ metallization was published in 2017 [29]. At that time, the selectivity was achieved by a thin ALD- $\text{AlO}_x$  layer and LIFT seed layer patterning. The first monofacial SHJ solar cells created using this process achieved a solar cell efficiency of 22.2%, in comparison to 21.7% for the screen-printed reference solar cell.

In subsequent developments, the focus was on the implementation of a native  $\text{AlO}_x$  layer as a masking layer, along with inkjet-based patterning processes. The first SHJ solar cells metallized with the printed NOBLE sequence shown in Fig. 10 were published by Hatt et al. in 2019 on small-area [28] and large-area [32] solar cells, achieving cell efficiencies of 20.2% and 20.0%, respectively. More recently, large-area cells with solar cell efficiencies of up to 21.2% were fabricated with the NOBLE back-end sequence. The recent developments were limited by non-optimized mask patterning and PVD seed layer processes. Current process developments are now centring on optimizing these process steps in order to develop the full potential of the NOBLE process for plated SHJ solar cells.

**Cost calculations**

The COOs for the different back-end approaches are shown in Fig. 11. The COO calculations assume a SHJ solar cell with bifacial grid design, having 120 and 200 fingers on the front and rear sides, respectively. For solder interconnection, five busbars per wafer side are assumed, each with a width of 500µm. The other interconnection scenarios are ECA interconnection and SWCT, both of which do not require any printed metal busbars, which therefore saves on silver. In the case of SWCT, the small wire pitch allows a higher finger resistance with even lower paste lay-down.

The metallization processes are: bifacial Ag screen printing, plating with organic mask, and NOBLE. The assumed Ag paste or resist lay-down for the metallization or mask patterning processes are summarized in Table 2.

In the COO calculations for the metallization sequences shown in Fig. 11, one of the main cost drivers for screen-printing metallization approaches is the metallization consumables. A price of €589/kg was assumed for the Ag printing paste (low-temperature Ag pastes are, however, more expensive). The reduced paste lay-down made possible by using ECA or SWCT results in significant reductions in silver costs.

In terms of cost, plated Cu metallization with or without an organic mask is clearly superior to screen-printed metallization with busbars. The cost of the organic mask, however, is of the same order as the cost of the silver when SWCT interconnection is used. It is here that the NOBLE process has a clear advantage, even when the cost benefit with regard to waste water treatment is not taken into account. Nevertheless, both plating approaches can still be attractive, since interconnection by ECA or SWCT may help to reduce costs for metallization, although typically increasing interconnection costs. The metallization equipment depreciation for the two plating approaches is relatively high as a result of the required add-ons to the PVD tool; however, the depreciation is mostly due to the high investment costs for inkjet printers and plating tools, compared with state-of-the-art screen printers. It can be expected that tool prices will fall, however, if plating is adopted in an increasing number of SHJ production lines.

**Conclusion**

The integration of Cu-plated contacts can further decrease the production costs of passivated-contact solar cells.

### Plating metallization for i-TOPCon solar cells

Bifacial and hybrid (plating/screen printing) TOPCon solar cells with laser-defined and plated Ni/Cu/Ag contacts demonstrate efficiencies of up to 22.7%, and open the way to further reducing the resistive, recombination and optical losses of i-TOPCon solar cells. Low contact resistance and low finger line resistivity allow finger widths less than 25µm, while low contact recombination enables a reduced TOPCon thickness to less than 100nm. Future work will need to focus on estimating the minimum TOPCon thickness that would allow low contact recombination for laser-defined plated Ni/Cu/Ag contacts.

The cost calculations show that the introduction of plated contacts, especially in the form of a bifacially plated grid, enables the back-end processing cost for TOPCon solar cells to be lowered. Further cost savings can be achieved by reducing the TOPCon layer thickness, because of the shallow laser-damage depths associated with ultrashort-pulse laser ablation.

### NOBLE Cu-plated contacts for SHJ solar cells

The NOBLE back-end sequence is a low-cost and low-temperature metallization approach for industrial SHJ solar cells. It offers the potential to realize metal grids with excellent electrical performance, suited to reliable module interconnection (e.g. busbar solder interconnection) and low grid resistance for creating high-efficiency bifacial SHJ solar cells.

NOBLE achieves a low COO as a result of the dramatically reduced cost of consumables, independently of the interconnection technology used, with the prospect of further significant cost reductions with regard to equipment and labour. Compared with organic masking, the NOBLE approach avoids organic waste water while decreasing the material costs and amount of patterning consumables.

### Acknowledgements

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## About the Authors



Sven Kluska studied physics at the Albert Ludwig University of Freiburg and received his Diploma degree in 2010, and his Ph.D. in the field of laser chemical processing for silicon solar cells in 2011. His research interests include electrochemical processing for solar cell applications with a focus on plating metallization. He is currently co-head of the Electrochemical Processes group.



Thibaud Hatt studied chemistry at the Joseph Fourier University in Grenoble and at the University of Strasbourg, where he received his master’s. He worked on Li-ion batteries at the CEA-LITEN, and then on developing wet-processes for polyamide-imide materials in the fibres industry. He joined Fraunhofer ISE in 2017 as a Ph.D. student to develop electrochemical processes, with a focus on plating metallization on TCOs for silicon heterojunction solar cells.



Benjamin Grübel received his master’s in electrical engineering and information technology in 2017 from the Karlsruhe Institute of Technology KIT in Karlsruhe, for which he carried out research on the interfacial oxide layers on laser-structured and plated contacts on silicon solar cells. Currently a Ph.D. student at Fraunhofer ISE in the Electrochemical Processes group, his current field of research is electrochemical metal deposition (plating) on polycrystalline silicon for high-efficiency silicon solar cell applications.



Gisela Cimiotti studied surface and material sciences at the University of Aalen. During her time as senior technologist at RENA GmbH, she was involved in the introduction of the plating technology for silicon solar cell production. Since 2012 she has been working at Fraunhofer ISE in the Electrochemical Processes group, where she focuses on plating.



Christian Schmiga received his Diploma degree in physics from the Georg August University of Göttingen, Germany. Since 2007 he has been with Fraunhofer ISE, where he is project manager for high-efficiency silicon solar cells. His research interests include the evaluation of cell efficiency potentials, the industrial transfer of new solar cell concepts, and the development of cell technologies from lab to line environments, with a focus on n-type cell structures and aluminium alloys.



Varun Arya studied microsystems engineering at the Albert Ludwig University of Freiburg and received his master's in 2016, with a thesis topic of design and fabrication of micro-sized single-mode waveguides made from flexible and non-toxic implantable polymer materials. Since 2017 he has been a doctoral candidate at Fraunhofer ISE, where his current research concerns temporal and spatial laser beam shaping, along with process development for minimal damage ablation of the solar cell dielectric layer for electroplated contacts.



Bernd Steinhauser studied physics at the Albert Ludwig University of Freiburg. In 2017 he received his doctoral degree from the University of Constance on the topic of multifunctional doped passivation layers for solar cell applications. Since 2009 he has been working at Fraunhofer ISE, and is currently a post-doctoral researcher. His research topics include surface passivation, dielectric layer deposition, laser ablation and plating on both p- and n-type silicon solar cells.



Frank Feldmann studied electrical engineering and information technology at the Technical University of Aachen (RWTH) in Germany from 2005 to 2010. In 2015 he received a Ph.D. from the Albert Ludwig University of Freiburg for his work on the TOPCon technology. He is currently is a post-doctoral researcher at Fraunhofer ISE.



Jonas Bartsch studied chemical engineering at the University of Karlsruhe and received his Diploma degree in 2007. He joined Fraunhofer ISE to pursue a Ph.D. in the field of advanced front contacts for silicon solar cells with plating technology. After receiving his Ph.D. from the Albert Ludwig University of Freiburg in 2011, he continued to work with plating at Fraunhofer ISE and is currently co-head of the Electrochemical Processes group.



Baljeet Singh Goraya studied renewable energy engineering and management at the Albert Ludwig University of Freiburg, and received his M.Sc. in 2016. He has since worked at IPVF, France, and rejoined Fraunhofer ISE in 2019. His current field of research is technology assessment and techno-economic evaluation, with a focus on PV manufacturing cost calculations, technology transfer and road-mapping activities for both established and emerging PV technologies.



Sebastian Nold studied industrial engineering at the University of Karlsruhe, Germany, and the University of Dunedin, New Zealand. He received his Diploma degree in industrial engineering from Karlsruhe in 2009, and his Ph.D. from the Albert Ludwig University of Freiburg in 2018. He has been with Fraunhofer ISE since 2008, working in the fields of cost modelling, technology assessment and techno-economic evaluation of silicon PV production technologies.



Andreas Brand studied physics and laser technology at RWTH Aachen, Germany. He has many years of experience in ultrashort pulse lasers and their applications from his time at the Fraunhofer Institute for Lasertechnology in Aachen. In 2011 he joined Fraunhofer ISE to pursue a Ph.D. in the field of laser micro-machining of thin layers on semiconductors. He has been the head of the Laser Process Development team since 2017.



Jan Frederik Nekarda studied physics at the Ludwig Maximilian University of Munich and the Albert Ludwig University of Freiburg. He joined Fraunhofer ISE in 2005 and received a Ph.D. from the University of Constance in 2012. Since 2018 he has been the head of the PV Production Technology – Structuring and Metallization department.



Markus Glatthaar received his Ph.D. in physics in 2007 from the University of Freiburg. After his Ph.D. studies in organic solar, he worked as a postdoc at Fraunhofer ISE in the field of crystalline silicon solar cell characterization. Since 2012 he has headed the Advanced Development for High Efficiency Silicon Solar Cells department at Fraunhofer ISE.



Stefan W. Glunz received his Ph.D. from the University of Freiburg in 1995. He is the director of the Photovoltaics – Research division at Fraunhofer ISE and professor for Photovoltaic Energy Conversion at the Albert Ludwig University of Freiburg. His research interests include the design, fabrication and analysis of high-efficiency solar cells.

#### Enquiries

Sven Kluska

Tel: +49 761 4588-5382

Email: sven.kluska@ise.fraunhofer.de

# TOPCon technology: What exactly is it and how mature is it in production?

Radovan Kopecek, Jan Hoß & Jan Lossen, International Solar Energy Research Center (ISC) Konstanz e.V., Germany

## Abstract

Over the last few years, passivated-contact nPERT solar cells, referred to as *TOPCon* cells, have been receiving increasing interest among solar cell manufacturers. At the beginning, the development was mostly initiated by n-type solar cell producers, but it is now also attracting the attention of many PERC producers, who are approaching the limits of their standard production lines. In this paper the situation of solar cell production in China is summarized, and an attempt is made to answer the question of whether passivated contacts could replace PERC technology, which will eventually reach its efficiency limit in the future. The most relevant passivated-contact technologies in R&D and production are reviewed, and the major bottlenecks impacting on a successful industrialization are evaluated. Some parallels are outlined between the situation today and the evolution from homogeneous Al-BSF technology to PERC in the past.

## Introduction

Since 2016, when LONGi began introducing their low-cost Cz-Si wafers to the PV market, mc-Si and homogeneous Al-BSF technologies have been rapidly losing market share, as evidenced by Fig. 1. Back then, there was stiff competition between passivated emitter and rear cell (pPERC) and passivated emitter, rear totally diffused (nPERT) technologies, but PERC later prevailed – mostly because of the cheaper price of p-type wafers and associated processing sequences and materials (e.g. Ag and Al pastes). An additional advantage of PERC was the fact that the process sequence was closer to that for p-type standard cells, which facilitated a

gradual adaptation of existing production lines.

PERC technology subsequently became, much more quickly than anyone expected, the leading solar cell technology, with the highest production capacity and the lowest cost of ownership (COO). Towards the end of 2019, mono PERC production capacity reached 95GWp (see Fig. 2), which corresponds to a total annual solar cell production of more than 120GW, equating to a 75% market share.

Standard PERC cell efficiencies, however, are expected to reach their limits soon; scientists in the PV community estimate that this will happen at an average production efficiency value of 22.5–23% [2]. Fig. 2 shows that, during the period Q2 2019 to Q3 2019, an increasing share of PERC production lines had been upgraded to produce cells with selective emitters, reaching a total of 75GW. This can be interpreted as an indication that PERC producers are approaching the efficiency limits of this cell technology, and are squeezing out the last efficiency gains from their production lines. To achieve even higher efficiencies with PERC-like solar cells, new technologies will need to be implemented.

This raises the question of which cell concepts will replace PERC as the leading solar cell technology of the future. Or, more specifically: how can the voltage of low-cost industrial solar cells be increased towards 700mV and beyond in order to obtain efficiencies well above 23%? And how can

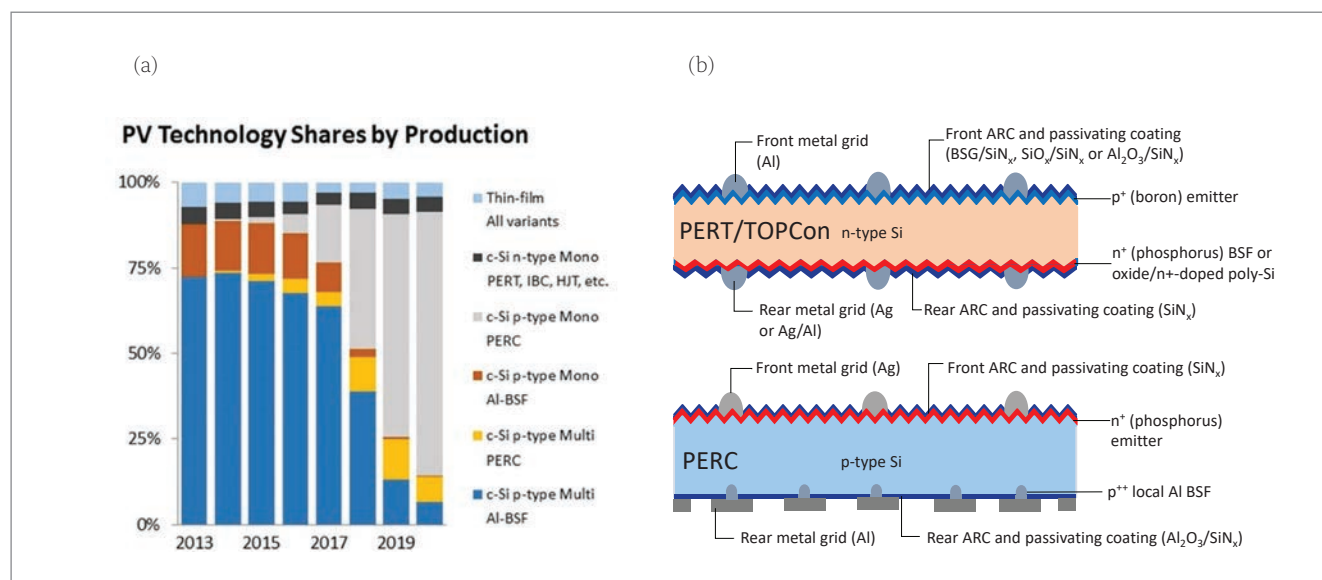


Figure 1. (a) Historical data and forecast for c-Si technology market share from PV ModuleTech [1]. (b) A typical cross section of an n-type PERT solar cell (top) and a p-type PERC solar cell (bottom).



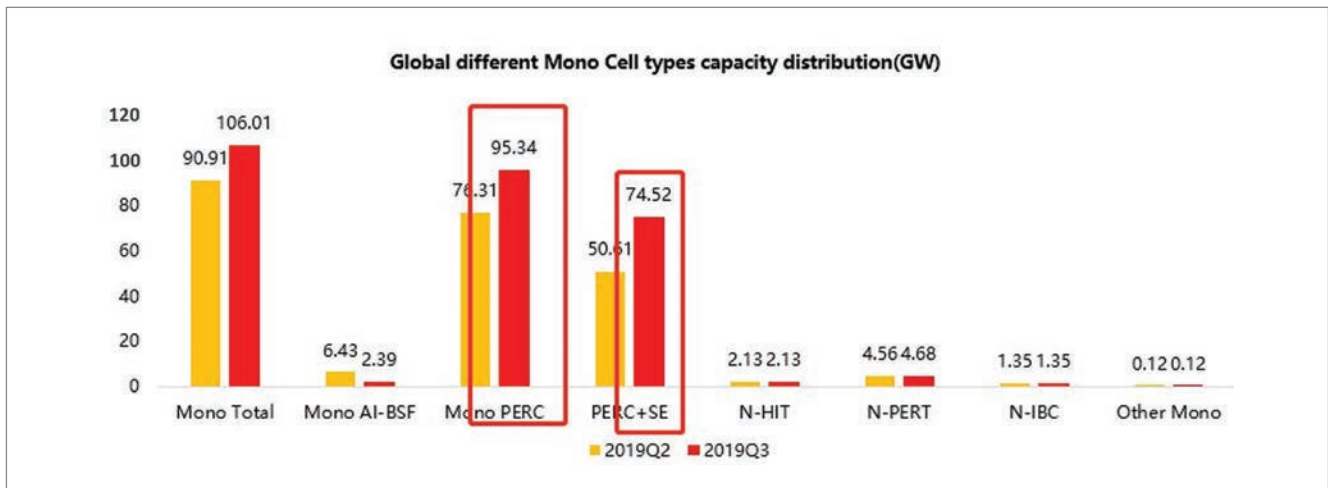


Figure 2. LONGi's data on Cz-Si solar cell technology market share in 2019. (PERC+SE are PERC structures that include selective emitters.)

this be achieved at acceptable costs, i.e. without the addition of too many and too costly new process steps? Fig. 3 shows that cell technologies with passivated contacts ('TOPCon' cells) can achieve the efficiency goal, but at a cost that is currently not competitive with that of PERC.

In 2019 many large PERC manufacturers, such as JinkoSolar and LONGi, reported at important Chinese PV conferences (e.g. PVSEC in Xi'an, SNEC in Shanghai or CSPV in Shanghai) that it is becoming increasingly difficult to maintain steady efficiency gains with standard PERC technology. As contact recombination is a main limiting factor, they

concluded that passivated contacts would need to be implemented as a next step.

Solar cells with passivated contacts, in Asia often referred to as *TOPCon*, a term coined by FhG ISE for their passivated-contact solar cell, have been developed for both p-type and n-type cell concepts. The essential novelty with respect to conventional cell technologies is that diffused or alloyed regions of the cell are replaced by a stack of silicon dioxide and doped polysilicon (poly-Si). The replacement of n-doped regions by oxide/poly-Si stacks with excellent surface passivation was already achieved several years ago; for p-doped poly-Si layers, however,

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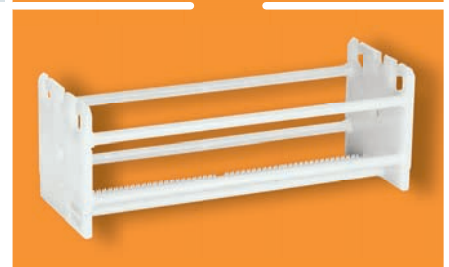
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the process is more challenging [4]. Furthermore, it has to be taken into account that poly-Si layers are optically highly absorptive, making full-area application on the front side unattractive.

Most research institutes and cell manufacturers are therefore developing n-type cell concepts with poly-Si passivated contacts on the rear side, in particular nPERT (Trina Solar, Jolywood, JinkoSolar, SPIC and others) or n-interdigitated back contact (nIBC) cells (Trina, LG electronics) structures. Nevertheless, concepts for cell architectures based on p-type substrates – often called *polyPERC* – also exist [5]. Another alternative is p-interdigitated back-contact (pIBC) solar cells, combining n-poly layers with alloyed local Al contacts [6,7]; however, such a rear-junction cell concept suffers from the limited charge-carrier diffusion length of currently available commercial p-type Cz-Si substrates.

At the 29th International PVSEC in 2019 in Xi’an, an overview of the highest efficiencies obtained for large solar cells in China was presented and is shown in Fig. 4 [8]. An efficiency of 24.58% was achieved with a TOPCon nPERT cell by Trina, and 24.03% with a PERC-type cell from LONGi. While both the cells in question are assumed to use an intricately patterned poly layer on the front side (which is not suitable for cost-effective industrial production), the reduced charge-carrier recombination of the TOPCon rear side, compared with a standard PERC rear side, is clearly visible from the measured high  $V_{oc}$  of the TOPCon cells.

At the beginning of 2020, only a few companies had started pilot production or full production of TOPCon cells: examples are Trina, Jolywood, Linyang, JinkoSolar and SPIC. All of them use low-pressure chemical vapour deposition (LPCVD) of the poly-Si layer, a choice that is motivated by the excellent passivation quality of LPCVD-deposited poly-Si layers, as well as by the availability of corresponding deposition tools. However, it is the authors’ understanding that significant challenges still remain, including the complex process sequence as a consequence of the conformal poly-Si deposition in the LPCVD process, and the necessity to deposit thick poly-Si layers for achieving sufficient passivation in combination with screen-printed firing-through metallization. The latter procedure further reduces the service life of the quartz tubes, one of the drawbacks of LPCVD deposition of poly-Si, which will be discussed in more detail below. These challenges will need to be overcome in order for TOPCon to compete with PERC, which requires not only achieving high efficiencies but also fulfilling the specifications in terms of throughput and yield. Typical specifications associated with these quantities for n-type solar cell production are shown in Table 1.

For a classical diffused nPERT cell, an efficiency of 23% was unattainable. Therefore, all nPERT producers have switched (or are currently switching) to TOPCon, where 23% is possible,

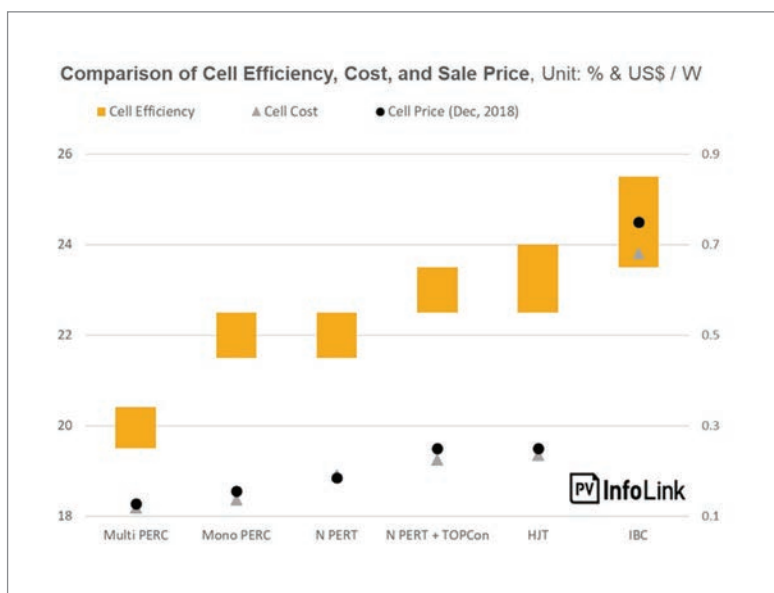


Figure 3. Efficiencies, COOs and selling prices for major c-Si technologies on the PV market [3].

although significant progress will still need to be made in order to fulfil the remaining specifications shown in Table 1. The costs for TOPCon cells must not be more than 1.2 times the costs for PERC, which is not yet the case, mainly because of the conformal deposition of poly-Si in the LPCVD reactors, leading to more complex processes, a lower yield and the short service life of the LPCVD quartz tubes (as well as because of the front and rear Ag metallization).

Consequently, alternative inline processes – such as atmospheric pressure chemical vapour deposition (APCVD), plasma-enhanced chemical vapour deposition (PECVD) and physical vapour deposition (PVD) – have been developed, which allow single-sided deposition of poly-Si. Furthermore, such alternative technologies allow the etching of residual poly-Si deposition from transport belts, holders or carriers, either continuously during the process or entirely outside of the reactor. These techniques will be discussed further later on. ISC Konstanz is evaluating many of these techniques in order to develop a simple and high-throughput process that can be transferred to the market in the coming years.

### Achieving higher voltages as in PERC

A simple way of comparing different c-Si cell technologies is to look at their maximum voltages instead of efficiencies. The open-circuit voltage  $V_{oc}$  is a reliable measure of the recombination at high carrier concentrations, and defines the upper limits for both fill factor and cell power. A comparison of the measured efficiency, on the other hand, is sometimes misleading, as several institutes

**“Standard PERC cell efficiencies are expected to reach their limits soon.”**

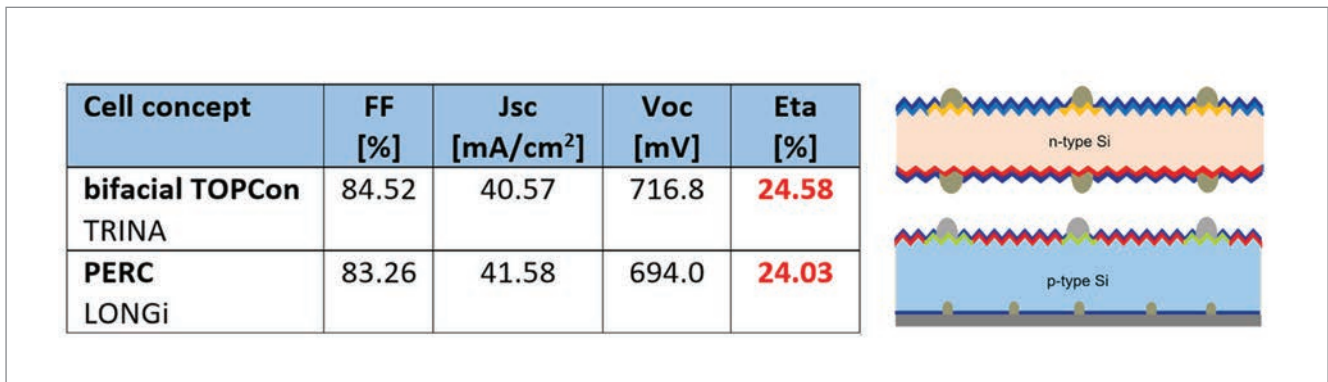


Figure 4. Highest efficiencies, measured at ISFH, for large-area PERT ('TOPCon') and PERC solar cells in China in 2019.

Efficiency [%]	>23
Throughput [wafers/sec]	~13
Capacity [MW/line]	>200
Yield [%]	>98
Cost of cell (relative to PERC)	<1.2
CAPEX (relative to PERC)	<1.3
Size	M4, M6

Table 1. Current manufacturing specification requirements for n-type cells [9].

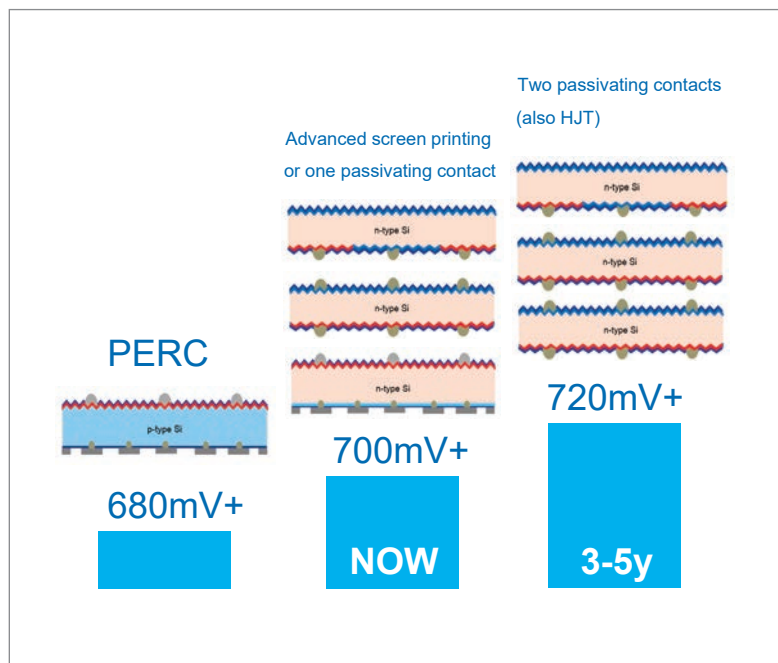


Figure 5. Classification of solar cell technologies in terms of  $V_{oc}$ .

“The costs for TOPCon cells must not be more than 1.2 times the costs for PERC.”

and companies report results from busbar-less measurements, or they report active-area efficiencies by subtracting the shading of the front-side metallization. Fig. 5 shows the three categories with  $V_{oc}$  ranges that can be achieved using low-cost solar cell processes today and that could be achieved in the future.

Typical voltages for PERC solar cells are around 680mV, with slight increases being possible when using selective emitter technologies. A voltage of around 700mV can be reached when applying passivated contacts to one polarity of the cell – for example by replacing a diffused rear side with a silicon oxide poly-Si stack. The latter is much easier for n-type technologies, since in this case the  $PCO_3$  diffusion is on the rear side. Instead of using passivated-contact technology, a reduction of the metallized surface area, for example by the use of point contacts, enables the voltage of the cell to be increased. With a flat boron-diffused surface (rear emitter PERT or IBC), it is possible to obtain voltages of the order of 700mV. Such high voltages without passivated contacts have been achieved by imec in collaboration with Jolywood with their rear emitter nPERT [10], by ISC Konstanz with MoSoN cell technology [11,12], and by ISC in collaboration with SPIC with ZEBRA technology [13].

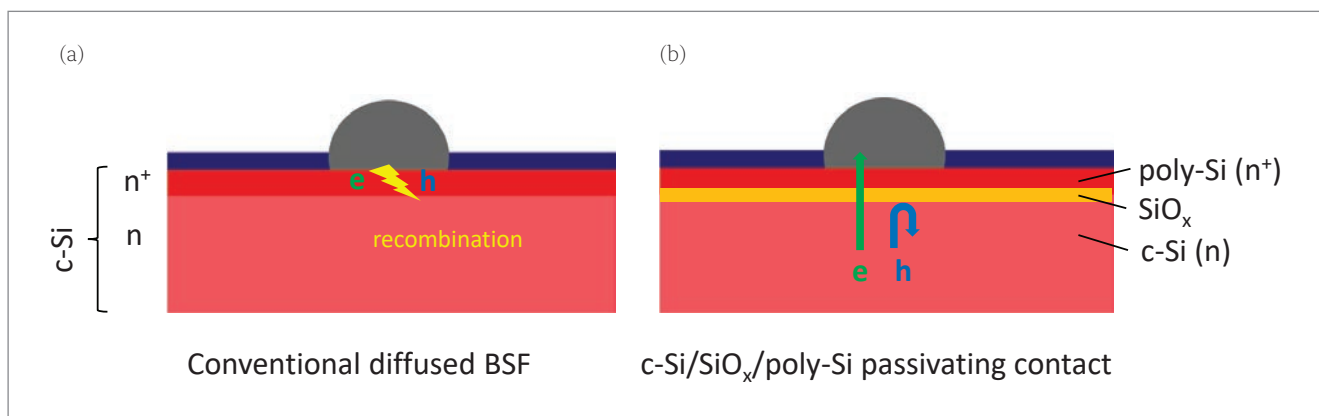
In order to reach 720mV, passivated-contact technology is required for *both* polarities – as also employed for heterojunction (HJT) cells. However, as of now, the equipment for such processes is very expensive, so typical manufacturing specification demands cannot be fulfilled yet. To reach even higher efficiencies, new devices – such as four-terminal tandem technologies with c-Si bottom solar cells and Perovskite solar cells on top – could be the answer within the next five to ten years.

**‘TOPCon’ (passivated-contact technology) – what is it exactly?**

Poly-Si passivated carrier selective contacts employ a thin silicon oxide layer to separate a highly doped poly-Si layer from the bulk absorber of the solar cell, as shown schematically in Fig. 6. This structure allows a high majority-carrier current towards the metal electrode contacting the poly-Si layer. The minority-carrier current, in contrast, is effectively blocked at the interface oxide, which suppresses interface state-mediated charge-carrier recombination at the metal contact.

The basic idea of using the passivated-contact concept (which is well known in bipolar transistor technology) for solar cells dates back to the 1980s. However, it did not receive much attention at that





**Figure 6. Schematic cross sections (not to scale) of: (a) a conventional diffused back-surface field (BSF); (b) a layer stack for a poly-Si passivated contact.**

Efficiency	Cell type	Research institute/company
25.2%	Tunnel layer passivated IBC solar cell	SunPower
25.7%	Front- and rear-contacted TOPCon solar cell	FhG ISE
26.1%	Poly-Si on oxide (POLO) passivated-contact IBC solar cell	ISFH

**Table 2. Highest efficiencies achieved using the different technologies.**

PERC 2010	Substrate mc-Si Cz-Si Low O LID	Passivation AlO <sub>x</sub> Thermal SiO <sub>2</sub> SiC <sub>x</sub>	AlO <sub>x</sub> Spatial ALD Batch ALD, Remote PECVD Plate PECVD	Metallization Evaporated Screen printed LFC Laser opening Chemical opening	Other Cell structure Process flow Stabilization PID Bifacial Yield Cost
TOPCon 2018	Substrate p-type n-type	Thin oxide wet chemical UV Thermal	Poly-Si LPCVD PECVD APCVD Sputter PVD HWCVD EB PVD	Metallization Evaporation Screen printing TCO Plating Al paste	Other Cell structure Process flow UV degradation PID Bifacial Yield Cost

ALD = atomic layer deposition; LFC = laser-fired contact; LID = light-induced degradation; PID = potential-induced degradation; HWCVD = hot-wire chemical vapour deposition; EB PVD = electron beam physical vapour deposition; TCO = transparent conductive oxide

**Table 3. Open questions during PERC development starting in 2010, and during TOPCon development from 2018 onwards (adapted from Chen [17]).**

time, as silicon solar cell efficiency was still more severely limited by other components of the device. It is believed that SunPower was the first company to commercially use passivated-contact technology to increase the efficiency of their IBC cell, but the company never disclosed any details on the cell architecture.

Passivated contacts for solar cells have been receiving ever-increasing attention since 2014, when the group of Prof. Stefan W. Glunz at Fraunhofer ISE researched the fundamental properties of the passivation layer stack using modern characterization methods [14]. Fraunhofer ISE also coined the name *TOPCon* as the abbreviation for ‘tunnel oxide passivated contact’ – initially for a PECVD-deposited Si-layer stack with carbon admixture, but eventually for all kinds of poly-Si layer on a SiO barrier layer. Other research institutes

picked up the topic and contributed valuable insights in areas such as transport through the oxide (ISFH), the influence of doping profile variations (ECN), and alternative deposition methods (ANU, SERIS, ISC, FZJ). Record efficiencies for small-area laboratory cells were achieved by Fraunhofer ISE with 25.7% [15] for two-sided solar cells, and 26.1% for an IBC by ISFH [16] (see Table 2).

**How mature are passivated-contact technologies in production?**

Solar cell architectures which employ passivated contacts (TOPCon) and are produced by different manufacturers today are very similar, even though

**“For passivated-contact nPERT technology, the most critical process is the formation of the poly-Si layer.”**

ISC-LPCVD	Jolywood /SPIC	TRINA	Linyang BSG	Linyang AlO <sub>x</sub>
sde & texture	sde & texture	sde & texture	sde	sde
BBr <sub>3</sub> diffusion	BBr <sub>3</sub> diffusion	BBr <sub>3</sub> diffusion	Clean & oxide	Clean & oxide
Single-side etch	Single-side etch	Single-side etch	LPCVD poly-Si	LPCVD poly-Si
Clean & oxide	Clean & oxide	Clean & oxide	POCl <sub>3</sub> diffusion	POCl <sub>3</sub> diffusion
LPCVD n <sup>+</sup> poly-Si	LPCVD poly-Si	LPCVD poly-Si	Wet process	Wet process
Annealing	P implant	POCl <sub>3</sub> diffusion	SiN <sub>x</sub> rear	SiN <sub>x</sub> rear
SiN <sub>x</sub> rear	Anneal	Anneal	Texture	Texture
Wrap-around etch	Wrap-around etch	Single-side etch and cleaning	BBr <sub>3</sub> diffusion/BSG	BBr <sub>3</sub> diffusion
SiN <sub>x</sub> front	AlO <sub>x</sub> front ALD	SiN <sub>x</sub> rear	Wet process	Wet process
Metallization & FF	Front & rear SiN <sub>x</sub>	SiN <sub>x</sub> front	SiN <sub>x</sub> front	AlO <sub>x</sub> /SiN <sub>x</sub> front
	Metallization & FF	Metallization & FF	Metallization & FF	Metallization & FF

Figure 7. Different process flows for nPERT cells with a rear-side passivated contact.

Company	Capacity [MW]
Jolywood	2,200
Yingli	800
JinkoSolar	800
LG	500
Linyang	500
Trina	500
SPIC	400
<b>Total</b>	<b>5,700</b>

Table 4. Companies with passivated-contact nPERT capacity in 2019 [9].

Boron diffusion	Poly-Si LPCVD
Centrotherm	Tempress
Tempress	Semco
Semco	Centrotherm
Laplace	Laplace
7-Star	Polar
P&Tech	P&Tech

Table 5. Two key steps for TOPCon and selected equipment suppliers [9].

the processing sequences may differ. Table 3 depicts a collection of different technology options that companies have been able to choose from during PERC development since 2010, and now during TOPCon development since about 2018 [17]. These

choices had to be (and still have to be today) carefully evaluated by considering the associated cell efficiency potential and the maturity and cost of the process. Diffusions of the front side are carried out by quartz tube diffusion, in a POCl<sub>3</sub> atmosphere for PERC and in a BBr<sub>3</sub> atmosphere for TOPCon. Other processes had to be (and still have to be) evaluated too – such as the selection of substrate, passivation layers, stabilization treatments, and opening of dielectrics, as well as metallization technology and respective pastes.

For passivated-contact nPERT technology, the most critical process is the formation of the poly-Si layer. Here the question remains how to achieve a sufficiently doped one-sided poly-Si layer so as to keep the process simple and cost effective. However, the metallization remains challenging too, as lower-temperature Ag pastes need to develop in order to achieve a good contact without penetrating the thin oxide layer. The company Toyal is even suggesting the use of low-temperature Al pastes to make this process more cost effective.

Even though these challenges have not yet been completely surmounted, several companies are already moving towards production; see Table 4 for a summary. Jolywood has the highest production capacity; however, this relies on fairly complex ex situ doping of the LPCVD poly-Si layers by ion implantation. The total capacity of all passivated-contact nPERT producers is about 6GW, of which a total of 4GW is accounted for in 2019.

As already discussed, the COO falls short of being competitive with PERC, as all the process flows

involved are still too complex. Fig. 7 shows several process flows published by the major TOPCon producers, along with ISC Konstanz's LPCVD reference process.

What the different processes have in common is that the  $\text{POCl}_3$  diffusion is replaced by the formation of a thin interface oxide and a subsequent LPCVD poly-Si deposition. The resulting silicon thin film is then doped ex situ via  $\text{POCl}_3$  diffusion (Trina, Linyang) or via ion implantation (Jolywood and SPIC). As illustrated by ISC Konstanz's process flow, the doping of the poly-Si layer can also be achieved via in situ doping during deposition, but at the expense of a reduced deposition rate.

A significant difference between the process flows of Linyang and the other companies is the sequential arrangement of the emitter diffusion and the poly-Si deposition. Whereas Linyang uses a process flow in which the  $\text{BBr}_3$ -diffusion is performed after the LPCVD deposition of poly-Si, the other published processes implement the poly-Si deposition after the  $\text{BBr}_3$  diffusion. Both approaches have different advantages and challenges concerning the front- and rear-side passivation.

Emitter passivation can be achieved using either a stack of  $\text{AlO}_x/\text{SiN}_x$  or a combination of boron silicate glass (BSG) and  $\text{SiN}_x$ , as exemplified by the two different Linyang process routes. Even though record efficiencies of above 24% can be realized by an adapted TOPCon process, average efficiencies in production vary between 22.8% ( $\text{SPIC}/V_{oc} = 695\text{mV}$ ) and 23.3% (Linyang with  $\text{AlO}_x/V_{oc} = 695\text{mV}$ ). Jolywood's average efficiency in production is reported to be 23.1% with a  $V_{oc}$  of 700mV, while Trina

**“Doping of the poly-Si layer can also be achieved via in situ doping during deposition, but at the expense of a reduced deposition rate.”**

has published an average efficiency of 23.0% with an average  $V_{oc}$  of 702mV [18]. The record TOPCon efficiency from Trina of 24.58% with a voltage of 717mV is suspected to have been achieved using a selective passivated contact on the front as well, similarly to the record ‘PERC’ cells from LONGi. A very good summary for all high-efficiency solar cell technologies on the market is also given in the report from Tayiang News [19].

In order to obtain not only high efficiencies but also low COO, several bottlenecks of the TOPCon process routes described above need to be addressed. One of the most important questions concerns the technology for poly-Si deposition, as detailed in the following section.

### Comparison of poly-Si deposition technologies

As of now, most cell manufacturers are focusing on developing passivated contacts using LPCVD deposition of poly-Si (Table 5). This choice is motivated by both the excellent passivation quality achieved with these layers, and the availability of industrial-scale deposition tools developed for the deposition of poly-Si in the semiconductor chip industry. While the results based on LPCVD deposition of poly-Si published by various cell manufacturers and research institutes are promising, this technology presents several challenges.

Deposition technique	Features	Schematic
LPCVD	<ul style="list-style-type: none"> <li>- Hot wall CVD</li> <li>- No ion impact needed</li> <li>- Very conformal deposition</li> </ul> BUT: both sided and tubes cracking	<p>(a): Source materials + carrier gas (b): Substrates (c): heater</p>
PECVD	<ul style="list-style-type: none"> <li>-Single-sided deposition</li> <li>-Lower temperature than LPCVD</li> </ul> BUT: wrap around	<p>(a): substrate (b): plasma (c): source gas + carrier gas (d): to pump (e): electrodes</p>
HWCVD	<ul style="list-style-type: none"> <li>- Much higher deposition rate than PECVD</li> <li>-Single sided</li> </ul> BUT: machine not industrial	<p>Evaporator heater element locking plate substrate shifter to pumps Gas showerhead Gas supply</p>

Figure 8. A selection of process technologies for the creation of poly-Si layers for passivated-contact technology.



An inherent disadvantage with many cell concepts is the conformal deposition of the layer, which requires dedicated process steps for single-side etching of poly-Si. Moreover, the lifetime of the quartz tubes is usually limited to a total deposition of around 100µm of poly-Si, owing to the increasing internal stress, which eventually leads to tube breakage. Since typical poly-Si layer thicknesses of 150–300nm are currently required for sufficient passivation after metallization [20,21], the quartz tubes must be replaced after ~700 runs.

In addition, the wafer throughput is limited by the deposition rate of around 3–6nm/min, which is further reduced when adding phosphine for in situ phosphorus doping of the layer. The latter issue can be mitigated by employing ex situ doping, e.g. using POCl<sub>3</sub> diffusion after the poly-Si deposition.

Given the challenges concerning the conformal deposition and the throughput of the LPCVD process, several alternative technologies have been investigated by research institutes around the world (Fig. 8). Possible single-sided deposition methods for poly-Si include different chemical vapour deposition processes (PECVD, HWCVD and APCVD), and various physical vapour deposition (PVD) processes, e.g. sputtering of silicon. Industrial tools are available for all of these processes, but not necessarily for the specific application of depositing highly doped and ultrapure silicon thin films. Research on optimizing these alternative processes for the production of solar cells with passivated contacts is therefore currently gaining increasing attention.

Silicon layers deposited via PECVD have been successfully integrated into TOPCon nPERT cells, leading to efficiencies of around 23% [22]. One of the main challenges of the PECVD-deposited silicon layer is the incorporation of hydrogen, which can lead to blistering of the layer. To avoid such effects, the deposition conditions – in particular temperature, gas flows, pressure and plasma power – need to be carefully optimized, making the optimization of the process more challenging than LPCVD depositions. Additionally, the wrap-around has to be minimized by dedicated carrier designs.

HWCVD deposition of the silicon layer uses hot wires to dissociate precursor gases. As with PECVD, in situ doping of the layers can be achieved, for example using phosphine and diborane as the dopant source. One of the key advantages of HWCVD is the potential to deposit a poly-Si layer with excellent surface passivation at very high deposition rates of up to 42nm/min [23].

Finally, PVD technologies, such as sputtering of silicon, can also be used as an alternative. In

situ boron-doped layers have been successfully integrated into p-type TOPCon cells with sputtered poly-Si and full-area metallization on the rear side, achieving 23% efficiency [24]. Excellent surface passivation has also been demonstrated for ex situ phosphorus-doped layers produced by sputtering of intrinsic silicon [25]. Sputtering of silicon could be an attractive alternative, offering a high-throughput process that produces a hydrogen-free silicon layer, without the need for any toxic gases and hence avoiding blistering of the layers.

## Summary and outlook

Passivated-contact technology implemented in nPERT structures, often referred to as TOPCon in China, is likely to be the next step after PERC technology, which is slowly approaching its limits. The total production capacity of TOPCon in 2019 was 5.7GW. However, there are still many challenges remaining to make this promising technology cost effective and competitive with PERC. The process needs to be simplified, mainly by developing high-throughput processes for single-sided deposition of poly-Si with in situ doping. Some progress in silver paste composition also has to be made in order to further reduce the poly-Si layer thickness while maintaining excellent passivation after metallization. On top of that, replacing Ag metallization either partly or fully by Al metallization, without cannibalizing cell performance, as suggested (for example) by Toyal, would lead to a further essential cost reduction.

PV technologies nowadays are moving towards higher front-side power and higher bifaciality, in order to save balance of system (BOS) costs in utility-scale systems. Since a higher voltage results in a lower temperature coefficient, solar cells with passivated contacts, and other high-voltage devices with high bifaciality factors, will become important in the future in order to achieve 1US¢/kWh in horizontal single-axis tracking (HSAT) bifacial systems. Such a low levelized cost of electricity will allow PV to enter the sustainable TW era in the coming years.

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**“Solar cells with passivated contacts, and other high-voltage devices with high bifaciality factors, will become important in the future in order to achieve 1US¢/kWh in HSAT bifacial systems.”**

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### About the Authors



Dr. Radovan Kopecek obtained his Diploma in physics at the University of Stuttgart in 1998. He also studied at Portland State University (Oregon, USA) and obtained a master's there in 1995. He finalized his Ph.D.

dissertation in Konstanz in 2002, and was a group leader at the University of Konstanz until the end of 2006. Dr. Kopecek is a co-founder of ISC Konstanz, where he has been working as a full-time manager and researcher since 2007, and is currently the head of the Advanced Solar Cells department. He has also been on the board of directors of EUREC since 2016.



Dr. Jan Hoß studied physics at the Karlsruhe Institute of Technology (KIT), Germany. He received his Ph.D. in 2017 from ETH Zurich, Switzerland, where he contributed to the development of a semiconductor

detector for high-energy particles for the Compact Muon Solenoid (CMS) experiment at CERN's Large Hadron Collider. In 2017 Dr. Hoß joined ISC Konstanz as a research associate, where he is involved in developing n-type solar cells with charge-carrier selective contacts, with a major focus on alternative poly-Si deposition technologies.



Jan Lossen studied physics at the Universities of Freiburg and Cologne in Germany. He graduated in 2003 with a thesis on the hot-wire chemical vapour deposition of microcrystalline silicon layers. Over a period of more

than ten years, he worked in different capacities on the production and development of crystalline silicon solar cells at ErSol/Bosch Solar Energy AG. Since 2014 Jan has been a senior scientist and project manager for process transfers at ISC Konstanz, where he is head of the Passivated Contacts group.

### Enquiries

Dr. Radovan Kopecek  
International Solar Energy Research Center  
Konstanz e.V.  
Rudolf-Diesel-Straße 15  
D-78467 Konstanz, Germany

Tel: +49 (0) 7531 / 36 183 – 22  
Email: radovan.kopecek@isc-konstanz.de  
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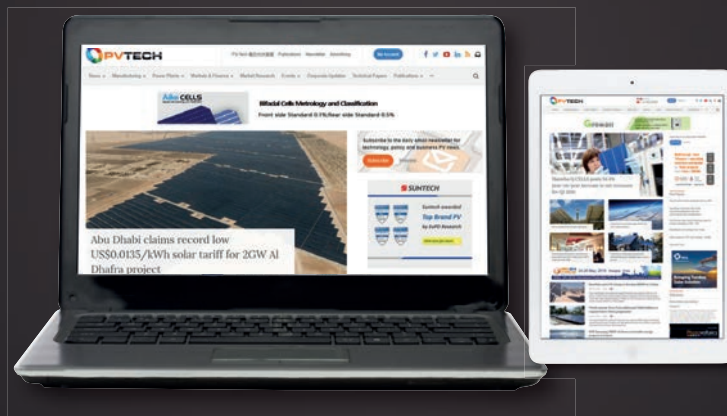


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# Industrial TCOs for SHJ solar cells: Approaches for optimizing performance and cost

Alexandros Cruz<sup>1</sup>, Darja Erfurt<sup>1</sup>, René Köhler<sup>2</sup>, Martin Dimer<sup>2</sup>, Eric Schneiderlöchner<sup>2</sup> & Bernd Stannowski<sup>1</sup>

<sup>1</sup>Helmholtz-Zentrum Berlin, PVcomB, Berlin, Germany; <sup>2</sup>VON ARDENNE GmbH, Dresden, Germany

## Abstract

Silicon heterojunction (SHJ) solar cell technology is an attractive technology for large-scale production of solar cells with a high conversion efficiency beyond 24%. One key element of SHJ solar cells, contrasting with today's widespread passivated emitter and rear contact (PERC) cell technology, is the use of transparent conductive oxide (TCO), which poses challenges in performance and costs but also presents opportunities. This paper discusses these aspects and shows the potential for improving cell efficiency at reduced cost by using new TCOs deposited by direct current (DC) sputtering. In the case of rear-junction SHJ cells, it is possible to reduce, or even avoid, indium usage in such TCOs, with aluminium-doped zinc oxide (AZO) being one possible substitute for indium-oxide-based TCOs. The availability of high-performance TCOs for large-scale mass production, which will encourage the market penetration of SHJ cells, is summarized.

Because of the low-temperature (<200°C) processes and the symmetrical device stack, stress-induced wafer bending and cracking can be avoided, which means *thin* wafers can be utilized, thus saving material costs and energy. The SHJ stack occurs naturally in a bifacial cell design; moreover, SHJ cells have the lowest temperature coefficient in the field, typically  $-0.28\%/^{\circ}\text{C}$ . The combination of bifaciality and low temperature coefficient increases the energy yield of a PV system.

On the other hand, some of the factors limiting a rapid increase in the uptake of SHJ technology are the relatively high equipment costs, mostly for PECVD (but also for PVD), and the adapted cell contacting for module manufacturing (no standard high-temperature soldering). More Ag paste is needed than for standard Si cells, because of the low-temperature curing, yielding lower-conductivity fingers; this, however, depends on the interconnection approach, specifically whether or not busbars are used. Finally, and discussed in more detail in this paper, targets for sputtering the TCO layers on both sides are required, which are costly for the materials that are usually employed.

Indium oxide ( $\text{In}_2\text{O}_3$ ) doped with tin (Sn), referred to as *ITO*, is currently the most commonly used TCO [3–5]. This transparent conductive oxide is well known from the mass production of flat-panel displays (FPD) and exhibits suitable opto-electronic properties, such as low resistivity of thin layers and sufficient transparency in the visible range. An important consideration for FPD production, *ITO* can be processed by photolithography, as it is etchable (in the as-deposited state) and is long-term stable after solid-phase crystallization upon thermal annealing at 150–200°C. Generally, ITO is deposited by direct current (DC) magnetron sputtering on large areas. Even though DC sputtering initially causes some damage of the silicon surface passivation, this is fully annealed at temperatures of around 200°C, which is reached either during sputtering or later during curing of the Ag paste after screen printing.

In contrast to FPDs, TCO has to fulfil additional

## Introduction

Silicon solar cells based on passivated emitter and rear contact (PERC) technology have reached multi-gigawatt levels in mass production, with conversion efficiencies (CEs) of 22% and now approaching 23%. For even higher CEs, passivated contacts are considered to be the next generation of cell technology. Here, silicon heterojunction (SHJ) technology is a promising candidate and is racing out of the starting gate, with a CE of 23–24% having already been demonstrated on full-size wafers, not only in pilot lines but also in large-scale production [1]. While it was Panasonic (formerly Sanyo) who pioneered this technology, various players worldwide have in the meantime been building up their own production lines, such as ENEL Green Energy and Hevel Solar in Europe, and REC, Jinery, GS-Solar and various others in Asia.

The major benefits of SHJ technology were discussed in a recent article by Ballif et al. [2]. Besides the high CE, a key advantage of SHJ is the lean production sequence, with only four main steps required for processing both sides symmetrically:

1. Wet-cleaning and texturing of wafers.
2. a-Si:H deposition by plasma-enhanced chemical vapour deposition (PECVD).
3. Deposition of transparent conductive oxide (TCO) layers by physical vapour deposition (PVD, usually sputtering).
4. Screen printing of silver grids.

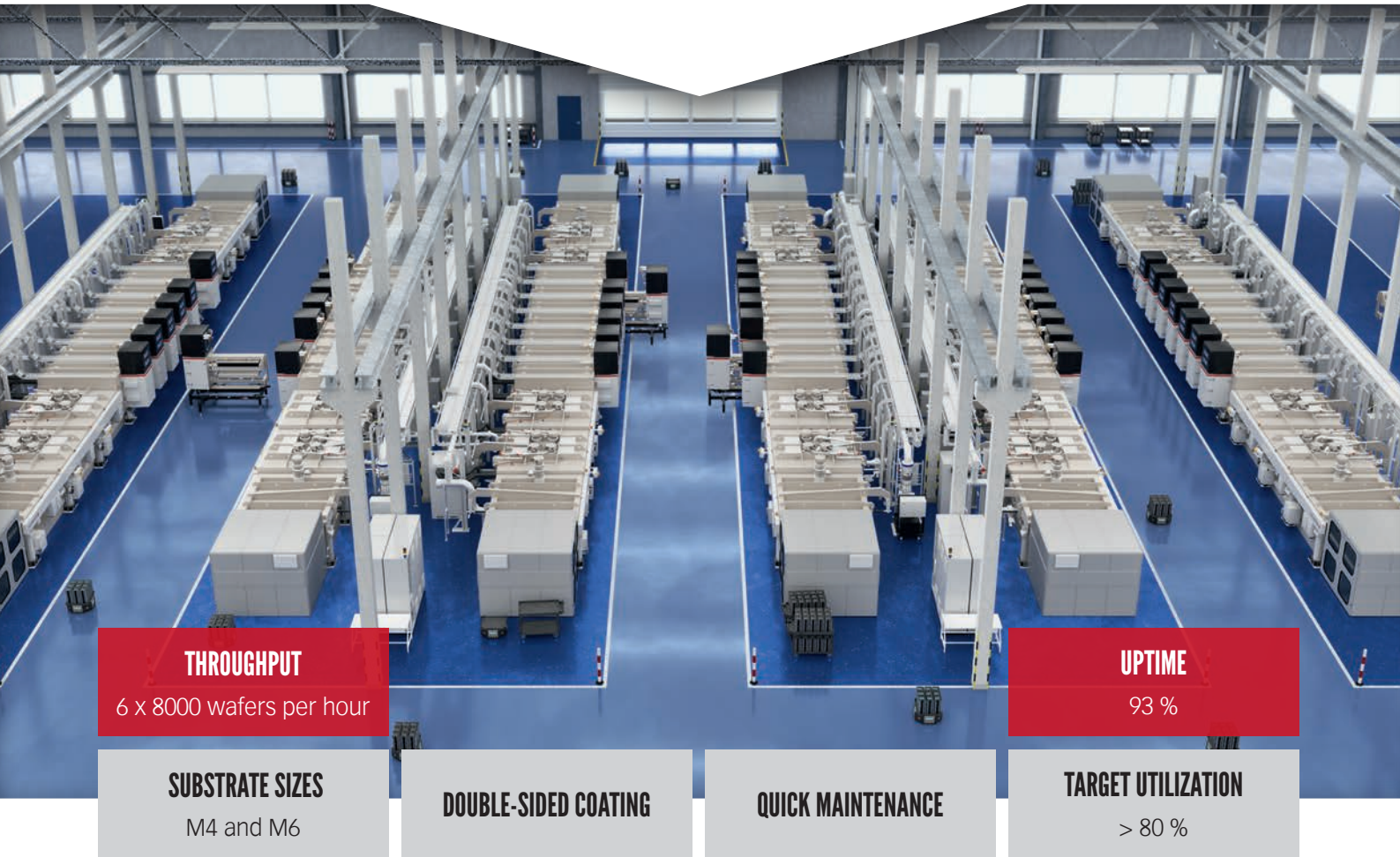


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requirements when applied to the front side of SHJ cells, namely an excellent transparency in the wider wavelength range 300–1,100nm. Fig. 1 shows the absorption spectra of various TCO layers, demonstrating the differences in parasitic absorption in the short- and long-wavelength regimes. Besides this low absorption, low contact resistances with both the n- and p-doped silicon layers, as well as with the metal grid, are mandatory for the TCO layers on both sides.

Last, but not least, the cost constraints of solar cells are extremely stringent, and, to envision PV on a terawatt scale, it is essential to reduce (or better still, avoid) the use of critical or scarce materials, such as indium (In). The latter aspect, however, is still difficult to address, as most device-quality TCOs contain indium. One option is to decrease the thickness of such TCOs, which then requires a second layer to be deposited in order to maintain ideal optical (anti-reflective) performance. This, in turn, increases the number of process steps and, hence, the process complexity and costs.

For the replacement of indium in TCOs, on the other hand, aluminium-doped zinc oxide (AZO) is one of the very few alternative candidates which is considered. As will be discussed in this paper, although this option is an attractive, low-cost and abundant alternative, one has to cope with lower conductivity and poor long-term stability.

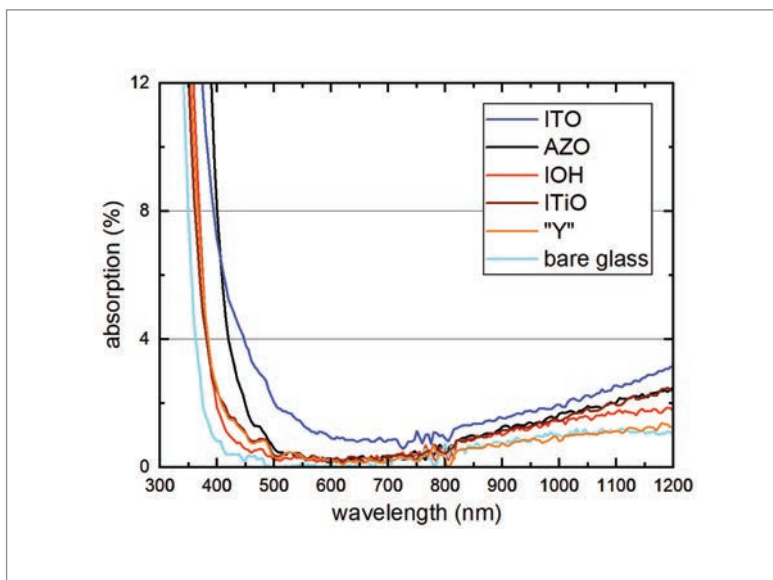
This paper addresses the optimization of TCO for incorporation in SHJ solar cells. A metric is presented for evaluating and benchmarking different TCOs with regard to their suitability for application in SHJ cells. To reduce the optical loss in the front TCO, the use of materials with a high transparency is mandatory. A high charge-carrier mobility, typically  $>100\text{cm}^2/\text{Vs}$ , allows a reduction in carrier density (at constant resistivity), thereby reducing the optical loss due to free-carrier absorption (FCA).

Various ‘high-mobility’ TCO materials based on indium oxide with different dopings have been investigated in the past [6–13]. All of these exhibit excellent properties as TCO layers on glass and most of them a high CE as well. Target manufacturing, however, is difficult and the costs are high for many of these materials.

New TCOs that can be processed in large-scale production from rotatable targets are now available, yielding high mobility and producing SHJ cells with high CE. The circumstances under which AZO as an indium-free and low-cost alternative can be implemented in high-efficiency SHJ cells will be discussed later. A cost comparison of In-based and ZnO-based targets will also be presented.

### TCO for SHJ solar cells

In the past, several TCO materials have been investigated for use in SHJ solar cells. Important requirements for this implementation are



**Figure 1. Optical absorption spectra for various types of TCO layer of thickness  $100\pm 10\text{nm}$  on glass substrate for implementation in SHJ cells.**

high conductivity and high transparency, with processing temperatures below  $200^\circ\text{C}$  (because of the sensitivity of thin-film silicon passivation layers), as well as good contact formation with the neighbouring layers [14].

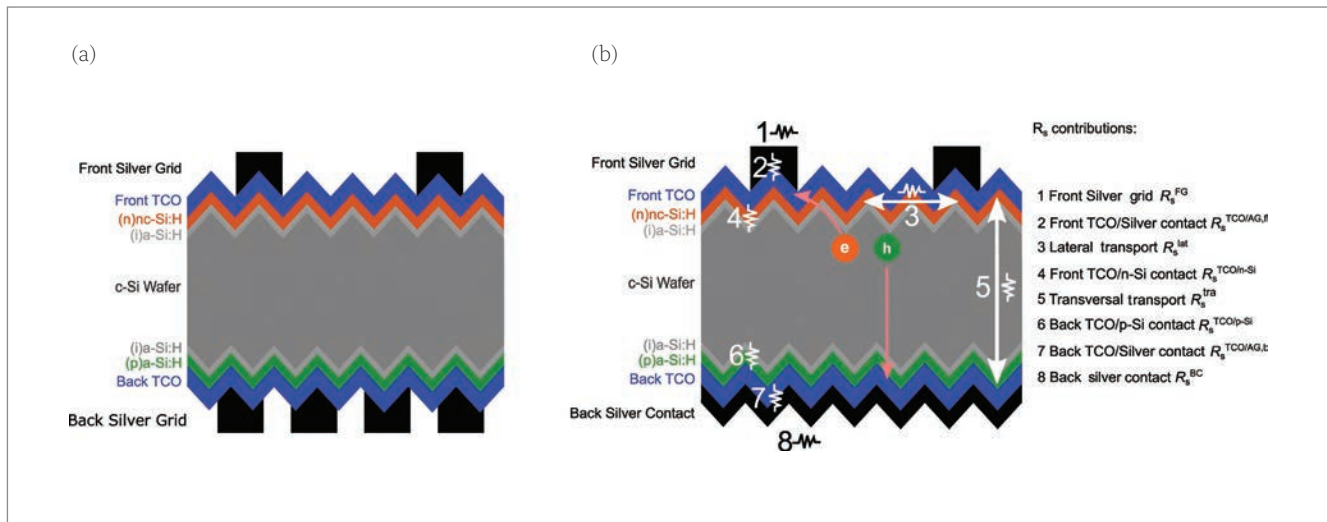
Among some of the relevant TCOs, polycrystalline Sn-doped  $\text{In}_2\text{O}_3$  (ITO) grown at temperatures below  $200^\circ\text{C}$ , which reaches electron mobility ( $\mu_e$ ) around  $40\text{cm}^2/\text{Vs}$  [3–5], has found wide application in SHJ solar cells. In-based TCOs doped with other metals, such as titanium (Ti) [15,16], zirconium (Zr) [6,12,13], molybdenum (Mo) [15,17–19] and tungsten (W) [10,11], yield  $\mu_e$  values greater than  $80\text{cm}^2/\text{Vs}$  at a charge-carrier density ( $n_e$ ) ranging from  $1\times 10^{20}$  to  $3\times 10^{20}\text{cm}^{-3}$ . These layers can be deposited via magnetron sputtering, pulsed laser deposition (PLD), and ion plating with DC arc discharge or reactive plasma deposition (RPD). Out of these, sputtering is the most established method for mass production. An even higher mobility of  $\mu_e > 100\text{cm}^2/\text{Vs}$  can be achieved for solid-phase crystallized (SPC) hydrogen (H)-doped  $\text{In}_2\text{O}_3$  (IOH) [6–9] and cerium (Ce)  $\text{ICeO:H}$  [7] films with  $1\times 10^{20} < n_e < 3\times 10^{20}\text{cm}^{-3}$ . These films are deposited at low temperatures in an amorphous matrix and subsequently annealed at temperatures above  $150^\circ\text{C}$ , which results in high  $\mu_e$  values because of the formation of large grains.

The TCOs introduced above are attractive because of their outstanding opto-electrical performance, but to date mainly ITO and IWO:H have found their way into industrial production. The scarcity of indium, however, is a motivation for the implementation of alternative TCOs. AZO offers the advantage of having more abundant composite materials. AZO layers with a thickness of several hundred nanometres,

**“To envision PV on a terawatt scale, it is essential to reduce the use of critical or scarce materials, such as indium.”**

TCO	Sheet resistance range	Sheet resistance $R_{\square}$ @ $t=75\text{nm}$ [ $\Omega$ ]	Electron mobility $\mu_e$ [ $\text{cm}^2/\text{Vs}$ ]	Carrier concentration $n_e$ [ $10^{20}\text{cm}^{-3}$ ]
ITiO, IOH, ICeO:H, IWO:H	Low- $R_{\square}$	40–70	80–120	1.5–2.0
ITO, IZO	Mid- $R_{\square}$	70–190	30–60	1.5–2.0
AZO	High- $R_{\square}$	170–370	15–25	1.5–2.0

**Table 1. Comparison of the electrical properties of different TCOs.**



**Figure 2. Schematic cross-sectional views of rear-junction silicon heterojunction (SHJ) solar cells: (a) bifacial cell design; (b) monofacial cell design, with the series resistance ( $R_s$ ) components shown.**

sputtered at elevated temperatures  $>250^\circ\text{C}$ , yield good opto-electronic properties [20] and also stability [21]. Thin layers of thickness less than 100nm deposited at temperatures below  $200^\circ\text{C}$ , as required for SHJ cells, in contrast exhibit a poor crystal structure, consequently resulting in low mobility values around  $20\text{cm}^2/\text{Vs}$  and poor long-term stability [22]. Improved stability for SHJ solar cells, however, has been shown by applying an amorphous silicon oxide ( $\text{a-SiO}_2$ ) capping [23].

As indicated by the  $\mu_e$  values obtained, and depending on processing conditions, the different TCOs demonstrate a wide range of electron mobilities. The TCO sheet resistance ( $R_{\square}$ ) ranges can be classified as shown in Table 1. Here, a carrier concentration range  $1.5 \times 10^{20} < n_e < 2.0 \times 10^{20}\text{cm}^{-3}$  is considered: this represents a good compromise for achieving low FCA, good electrical conductivity and good contact formation with neighbouring layers, and a 75nm TCO thickness for anti-reflective properties.

The symmetry in SHJ cell processing and the usage of (n-type) wafers with very high carrier lifetimes allows one to freely choose which contact (n or p) faces the front. The position of the p contact (junction) has an impact on the optimization of the front TCO for obtaining both high transparency and low series resistance  $R_s$  of the cell [24–27]. To demonstrate this, Fig. 2 shows schematic cross sections of bifacial and monofacial SHJ solar cells in a rear-junction configuration with all  $R_s$  contributions indicated. A detailed analysis of  $R_s$  components and

of their contributions in SHJ solar cells can be found in Basset et al. [25] and Wang et al. [28]. The high conductivity, i.e. density and mobility, of electrons in the c-Si wafer, along with the very low contact resistance of the n/TCO contact, favours the choice of the n contact being on the front (rear junction), as the lateral current transport is significantly supported by the wafer. This relaxes the conductivity requirement of the TCO (sheet resistance), thus allowing an optimization towards highest transparency.

To illustrate the effect of the above-mentioned freedom in cell design, Fig. 3 presents simulated  $R_s$  curves together with experimental values extracted from solar cells, with an ITO process variation as a function of the front-TCO sheet resistance. The experimental values validate the trends of the model [27]. As can clearly be seen, the rear-junction design offers an advantage for high-resistive TCOs by benefiting from the lateral support in electron conduction in the Si wafer. The front-junction design, on the other hand, is more favourable for low-resistivity TCO layers; this design takes advantage of the lower *transversal*  $R_s$  contribution, since electrons, having higher mobility than holes, travel to the rear of the wafer (with photogeneration mainly occurring close to the front side). The trade-off between the lateral and transversal  $R_s$  contributions will determine which solar cell design is most suitable, depending on the available TCO sheet resistance.

The  $R_{\square}$  ranges for different TCOs reported in the



literature and as defined in Table 1 are shown in Fig. 3 with the corresponding colour shading. TCOs with low  $R_{\square}$  (red) are more beneficial when implemented in a front-junction device, while TCOs with mid-range  $R_{\square}$  (blue) are in a transitional region where the  $R_s$  difference between front-junction and rear-junction devices is fairly small. In contrast, TCOs with high  $R_{\square}$  (grey) are clearly advantageous when implemented in a rear-junction design; this is favourable for AZO, for example, with it being highly transparent but not very conductive, yet still producing the same SHJ cell efficiency >23% as the ITO reference cell [23]. At the Helmholtz-Zentrum Berlin, SHJ solar cells with both ITO- and AZO-based front TCO have achieved a certified CE above 23.5% [29].

Another approach that takes advantage of the wafer lateral transport support, demonstrated by some research groups [27,30] and in pilot production [31], is to implement *thinner* TCOs, which reduces parasitic absorption, thus maintaining or improving solar cell CE. The implementation of a thinner TCO layer, however, requires a second layer on top – for example,  $\text{SiO}_2$  or  $\text{Si}_3\text{N}_4$  – to maintain the anti-reflection (AR) optimum [32–34].

To accurately quantify the optical performance of different TCOs when implemented in the cell stack, i.e. determine the specific loss in short-circuit current density ( $J_{sc}$ ), simulations with a ray-tracing software tool (GenPro4 [35]) were carried out. Taking into account the TCO-related power loss in the cell due to both an increase in  $R_s$  and a decrease in  $J_{sc}$ , different TCO materials were benchmarked, as shown in Fig. 4. For this purpose, a reference solar cell with CE = 23.3% was considered, without TCO-related losses in  $J_{sc}$  and  $R_s$  (FF). IOH, ITO and AZO were studied as examples of the low- $R_{\square}$ , mid- $R_{\square}$  and high- $R_{\square}$  regimes respectively.

Implementations of both standard 75nm-thick ('thick') and optically optimized thinner ('thin') TCOs were studied. For a fair comparison (i.e. to stay in the AR optimum in every case), *all* cells (with 'thick' and 'thin' TCOs) were finished with an a- $\text{SiO}_2$  capping layer. The contact resistivities at the TCO/Ag and TCO/Si interfaces were assumed to be (low and) equal for all three TCOs, which, of course, is a simplification. This will be discussed later and is presented in Haschke et al. [36]. Further details of the optimized layer thicknesses and simulation results can be found in Cruz et al. [27].

The graphs in Fig. 4 show the TCO-related power loss due to a decrease in  $J_{sc}$  and to an increase in  $R_s$  for rear-junction (Fig. 4(a)) and front-junction (Fig. 4(b)) devices. Clearly, the IOH outperforms the other two TCOs because of its outstanding opto-electronic properties in both cases. In Fig. 4(a), showing the thick ITO and AZO, the materials compensate their CE losses, since the lower-conductivity AZO shows lower parasitic absorption than the ITO. When this is compared with the thinner versions of TCOs, it can be observed that the CE loss slightly decreases as a result of reduced

TCO parasitic absorption. The ITO clearly benefits more from this thinning, because of its comparably higher parasitic absorption, ultimately leading to a slightly better CE than with AZO. This shows that thinner TCOs with improved optics can be implemented in a rear-junction configuration and will be beneficial in terms of CE.

In contrast, looking at the front-junction design in Fig 4(b), it can be seen that the high-conductivity IOH will not suffer from the lower lateral transport contribution by the wafer. The lower-conductivity ITO and AZO, however, increase the resistive losses. Decreasing the thickness of the ITO does not lead to a CE advantage, whereas in the case of the AZO it is clearly disadvantageous. It can be concluded that a high-conductivity TCO, here IOH in the example, can be implemented on both rear- and front-junction solar cell configurations without major differences in CE losses. Lower-conductivity TCOs – such as ITO and AZO – will suffer from the higher lateral  $R_s$  present in the front-junction configuration. Thinning the TCO on rear-junction solar cells is advantageous if the TCO exceeds a certain absorption threshold, even for a TCO with low conductivity, here AZO in the example. In a front-junction design, the thinning will only bring small benefits, or may even be disadvantageous for lower-conductivity TCOs such as AZO.

### Performance of industrial high-mobility TCOs

In order to test high-mobility TCOs sputtered at a high rate by DC sputtering from tube targets, as

“SHJ solar cells with both ITO- and AZO-based front TCO have achieved a certified CE above 23.5%.”

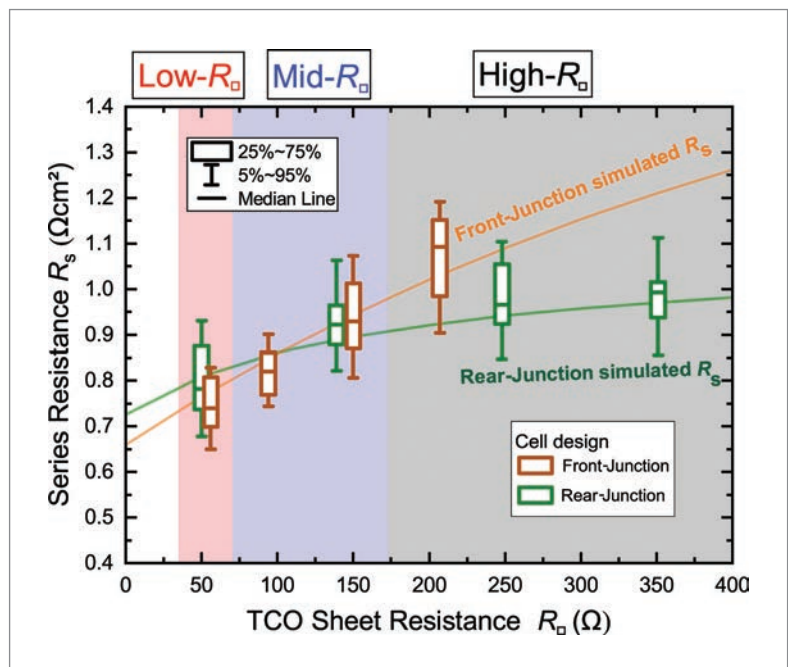
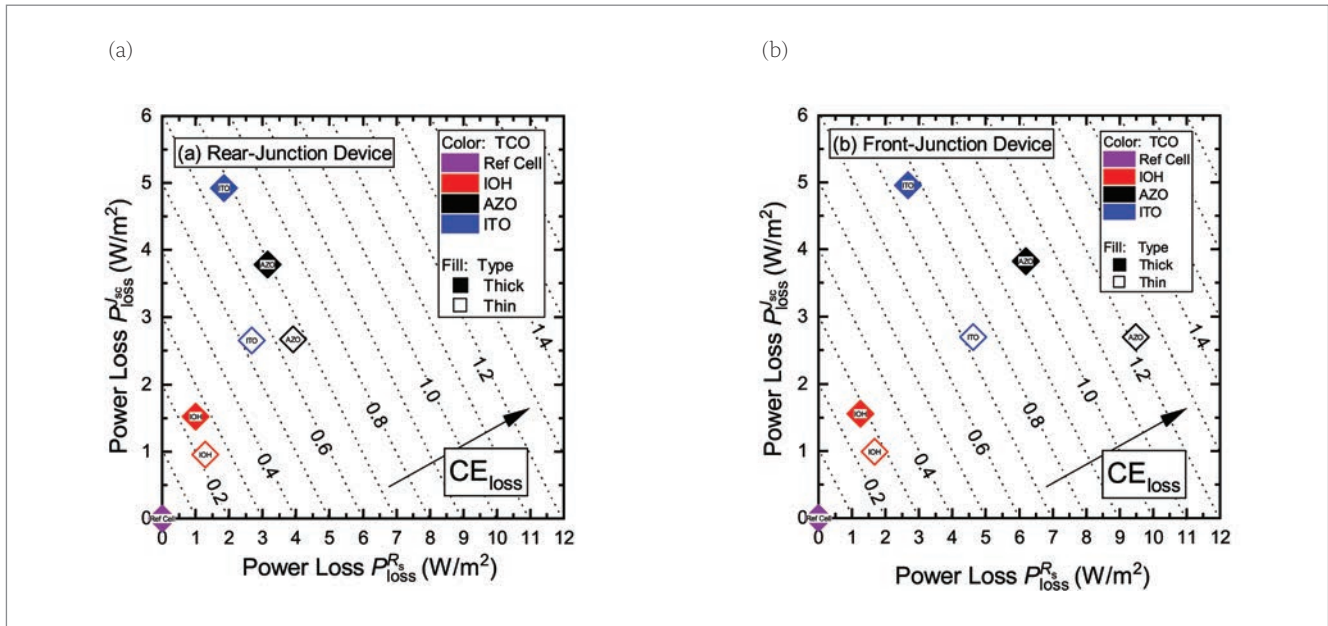


Figure 3. Series resistance versus front-TCO sheet resistance for front- and rear-junction SHJ solar cells. The curves represent simulated results, while the boxes indicate results for measured cells with an ITO variation.





**Figure 4. Current-density-related power loss ( $P_{\text{loss}}^J$ ) and series-resistance-related power loss ( $P_{\text{loss}}^R$ ) for (a) rear-junction and (b) front-junction SHJ cells. Conversion efficiency (CE) loss values are indicated by the dashed lines; these losses are relative to a reference solar cell with 23.3% CE, represented by the purple diamond at (0,0). The filled symbols represent 75nm-thick TCOs (standard) but with an anti-reflection coating (ARC) on top, while the open symbols represent thinner (optimized) TCO layers, also with an ARC.**

performed in large-scale mass production, different materials were used for the front TCO in bifacial rear-junction SHJ solar cells. Two types of high-mobility TCO were tested, namely titanium-doped indium oxide (ITiO) and indium oxide with an undisclosed doping type ('Y'). Additionally, ITO with various doping concentrations was tested, namely containing 97% indium oxide and 3% tin oxide in the target ('97/3') and ITO 99/1. As the reference material, ITO 97/3 was implemented on the rear side of all cells. A group of cells with ITO 95/5 on both front and rear sides was also included.

Corresponding test layers on glass revealed TCO sheet resistances in the range 36–136 $\Omega$  after deposition and annealing for 30 min at 200 $^{\circ}\text{C}$  under ambient conditions, which is comparable to the curing carried out after screen printing. This is a suitable range for the implementation as the front contact in rear-junction SHJ solar cells, as discussed earlier (see Fig. 3). It must be taken into account, however, that TCO layers deposited on glass might exhibit properties (carrier mobility) different from those when the layers are deposited on silicon, as required for solar cells. This has been attributed to two effects [29]: (1) different crystal nucleation and, hence, grain structure; (2) different hydrogen content which diffuses from the silicon layer into the TCO.

The ITiO and Y layers exhibit high mobilities of up to 90 $\text{cm}^2/\text{Vs}$ , but with different charge-carrier densities, namely  $2 \times 10^{20} \text{cm}^{-3}$  and  $\sim 0.8 \times 10^{20} \text{cm}^{-3}$  respectively. For ITO97/3 and ITO99/1 films, lower mobility values, of around 60 and 70 $\text{cm}^2/\text{Vs}$  at charge-carrier densities of  $2.7 \times 10^{20} \text{cm}^{-3}$  and  $1.8 \times 10^{20} \text{cm}^{-3}$  respectively, were measured. As a result of the very low charge-carrier density, the Y films showed the

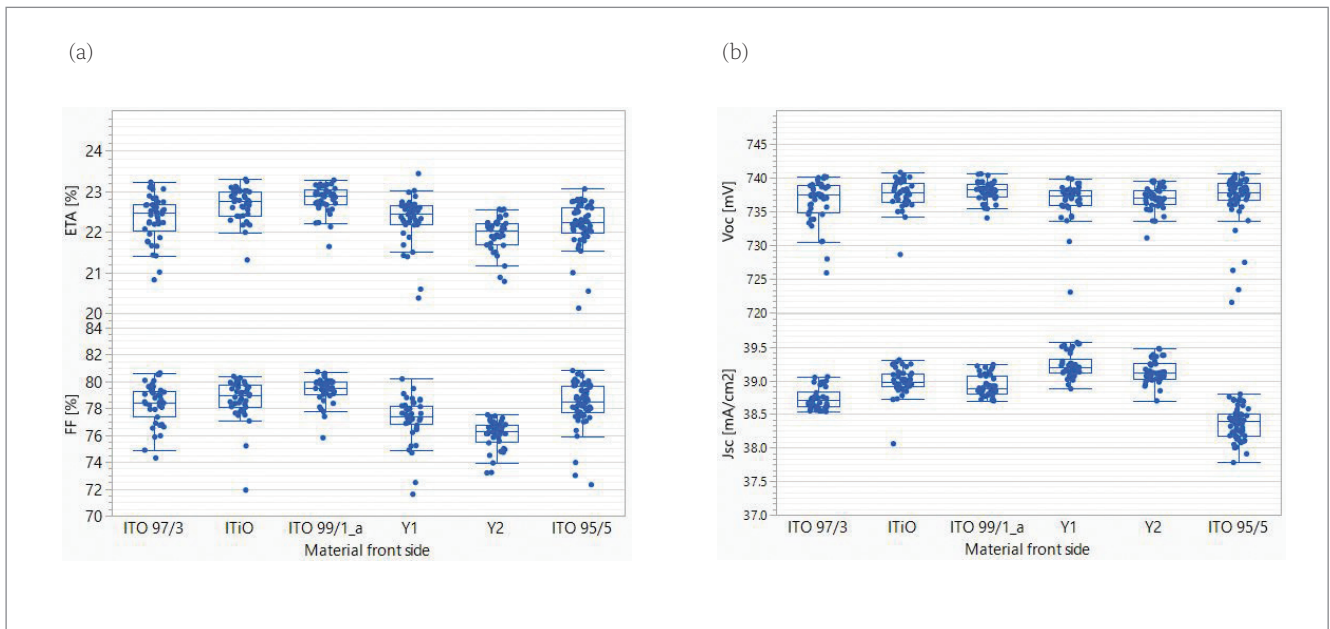
lowest parasitic absorption in the near-infrared region (see Fig. 1), which makes this material the most promising for achieving the highest  $J_{\text{sc}}$  and, possibly, the highest CE in solar cells.

The  $I$ - $V$  parameters of each of the test groups are shown in Fig. 5. All cells exhibit comparable open-circuit voltages ( $V_{\text{oc}}$ ), with medians in the narrow range of 737–738mV. This confirms that the passivation did not degrade because of different sputter damage. As expected, the solar cells with high-mobility TCOs yielded the highest  $J_{\text{sc}}$  values, with medians of 39.0 $\text{mA}/\text{cm}^2$  and 39.2 $\text{mA}/\text{cm}^2$  for ITiO and Y respectively. This is up to 0.5 $\text{mA}/\text{cm}^2$  higher than that achieved with the reference ITO97/3.

Despite the high  $J_{\text{sc}}$  and good  $V_{\text{oc}}$  values, however, the cells with a Y-front contact did not produce the highest efficiencies. The highest median CE of 22.9% was actually obtained for ITO99/1, while the highest value of CE of 23.3% was measured for a cell with ITiO. The lower CE in the case of the Y samples results from the lower median FF of only around 77%, which is due to a value of  $R_s$  that is considerably higher; in fact, the cells with a Y-front contact yield the highest median  $R_s$  values of 1.3–1.6 $\Omega\text{cm}^2$ . In contrast, the median  $R_s$  value is 0.9 $\Omega\text{cm}^2$  for the ITO99/1 cells, resulting in a significantly higher median FF of 79.5%.

### Importance of low contact resistance

The high series resistance of the cells with (low carrier density and) high-mobility TCO is in fact an aspect which needs to be tackled. More precisely, the two main components of  $R_s$  here are the contact resistance of the TCOs with the n- and p-doped silicon contact layers, which have been investigated in detail in the literature



**Figure 5. I–V parameters of 4cm<sup>2</sup>-sized bifacial SHJ solar cells with various front TCOs and ITO 97/3 on the rear side. ITO 95/5, DC sputtered from a tube target at HZB, was included as a reference.**

[37–40]. In the case of n-doped c-Si-based solar cells, the contact resistance of the TCO with the n-doped Si layers can be characterized by various, relatively simple, techniques, such as the Cox and Strack [41] or transmission-line [42] methods. The contact resistance of the TCO with the p-doped Si layer (TCO/p), in contrast, is more difficult to access, because a junction is formed. As shown by Basset et al. [21] and Wang et al. [24], for example, a simple method for extracting the value of the  $R_s$  component is to derive all the accessible components of  $R_s$ , and the remaining value is then concluded to be the TCO/p contact resistance.

The contact resistivity  $\rho_c$  depends on the detailed band alignment and band bending, as well as on the interface defect states; hence, several parameters are important, specifically the activation energy of the doped Si layer and the charge-carrier density, but also the work function difference between both materials. Procel et al. [38] showed that  $\rho_c$  is minimal when the doped layers exhibit low activation energy values, such as those obtained with nanocrystalline silicon layers instead of amorphous layers. Moreover, the charge-carrier density of the TCO should be well above  $1 \times 10^{20} \text{ cm}^{-3}$ ; this is particularly important for the TCO/p contact, for which efficient recombination of hole and electrons at the contact is essential. With regard to the selection and optimization of TCO layers, this entails finding an optimum for  $n_c$ , which must be high enough to achieve sufficiently low  $\rho_c$  values, but, at the same time, must be as low as possible in order to limit parasitic absorption (FCA).

In a more recent experiment, a Y layer with a higher carrier density was selected; Fig. 8 shows the properties available by tuning the process. Indeed, for the adapted TCO, the cell FF recovered, but at the cost of a small decrease in  $J_{sc}$  because of the

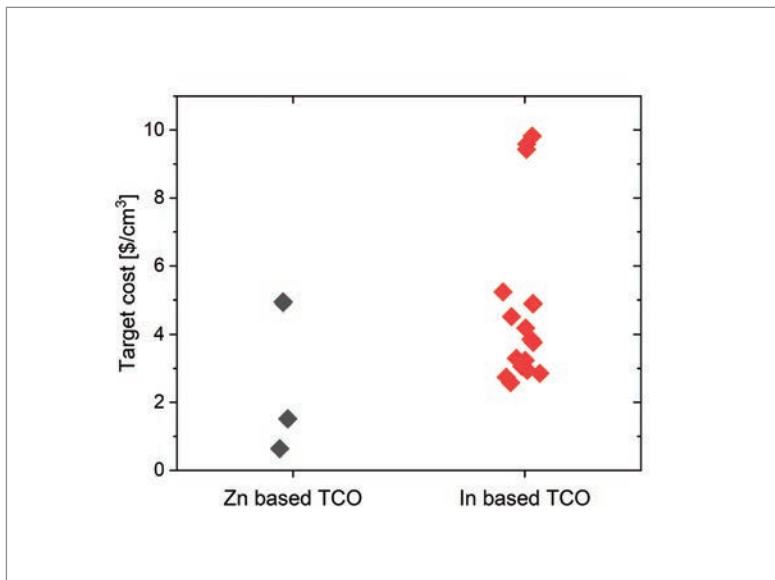
additional FCA. Overall, CE still increased up to a similar level to that found for the best groups in Fig. 5, which demonstrates the importance of careful tuning of the layer and interface properties.

### Industrial aspects: target costs

The common types of TCO target used in the crystalline silicon PV industry are *rotatable targets*, which are cylindrical shells of the TCO material bonded on a backing tube made of metal. The longer the tube, the more shells must be used for the tube target. The reason why the industry prefers this type of target for sputtering of TCOs is the much higher utilization rate of the TCO target material than that for planar types of TCO target. The utilization rate of the target material achievable with a rotatable target is usually  $\geq 80\%$ ; this is of particular interest in the case where TCO materials are expensive, such as indium-based TCOs. As regards TCOs in the crystalline silicon PV industry, indium-based TCOs are dominant owing to their excellent layer properties (as was also shown earlier). Nevertheless, some market players are also offering zinc-based TCOs for the same purpose. Indeed, there are advantages and disadvantages for using zinc-based TCOs. One advantage is the lower cost of a zinc-based tube target of dimensions identical to those of an indium-based target, whereas the lower conductivity of zinc presents some constraints in solar cell design, as discussed earlier and visualized in Fig. 3.

Fig. 6 shows the specific target cost per cm<sup>3</sup> of tube targets for zinc-based TCOs and indium-based TCOs; note that the cost of the backing tube is

**“The high series resistance of the cells with (low carrier density and) high-mobility TCO is an aspect which needs to be tackled.”**



**Figure 6. Specific target cost per cm<sup>3</sup> of target material for indium-based and zinc-based TCOs.**

## “Zn-based TCOs can be around a quarter the price of In-based TCOs.”

excluded from the target cost. The data points were collected from target suppliers all around the world. The smaller number of data points for zinc-based TCOs can be attributed to the lack of interest for that material shown by the crystalline silicon PV industry so far.

Some scattering in target cost exists because of the different materials within the zinc group and within the indium group, or because of different suppliers. The data points denoting higher target cost in both groups can be explained by less common compositions and/or costly manufacturing processes and/or high margins. The lower-cost data points observed in both groups

should be representative cost values for solar cell producers with several hundreds of yearly tube targets demand.

A comparison of the lowest value in both groups reveals that Zn-based TCOs (target cost ~\$0.6/cm<sup>3</sup>) can be around a quarter the price of In-based TCOs (target cost ~\$2.6/cm<sup>3</sup>). It should be pointed out, however, that these data points are a snapshot of the present situation and will soon probably become obsolete, depending on the volatility of the stock market with regard to feedstock material, in particular indium.

### Industrial aspects: TCO mass production

Besides the desire to implement indium-free TCOs with the aim of improving operational expenditure (OPEX), it is in the best interest to have a high-volume manufacturing sputtering tool which can produce a high-quality TCO coating at a low cost. Fig. 7 shows the highly productive XEA|nova L sputtering system from VON ARDENNE, which can deposit TCO layers at a throughput of 8,000 M6 wafers per hour in the basic version, and at an even higher throughput by using upgrade packages.

During 2019 the XEA|nova equipment became part of an industrial manufacturing line reaching top cell efficiencies of above 24% using TCO films similar to the ones investigated here.

In order to achieve a high throughput, the deposition rate of the TCO layers must be high, which can be realized by applying a high DC power to the tube target. However, the TCO properties still have to be maintained when TCO is prepared at higher power densities. Fig. 8 shows the electron mobilities and charge-carrier densities of TCO films, sputtered at 4kW and 8kW from ceramic tube targets of TCO type ‘Y’. High mobilities of around 80cm<sup>2</sup>/Vs could be achieved at a power level of 4kW after



**Figure 7. Example of TCO mass-production equipment: VON ARDENNE's XEA|nova L.**

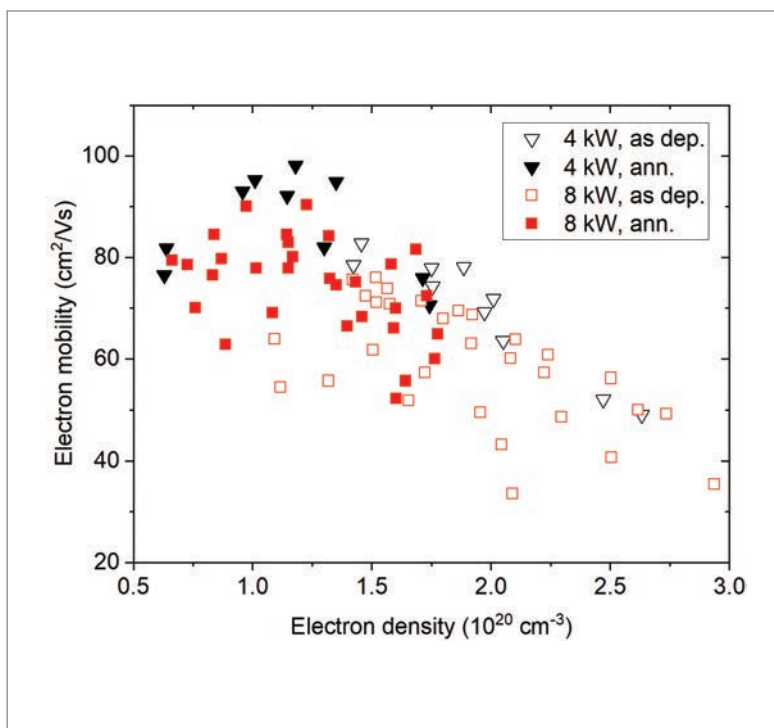
deposition. An increase of the sputtering power to 8kW reduces the maximum mobility by a maximum of 10%. It is interesting that the mobilities could be further increased, up to 100cm<sup>2</sup>/Vs, by annealing the films for 30 min at 200°C, as shown in Fig. 8.

### Conclusions

SHJ solar cell technology has demonstrated to be an important player on the way to increasing its share in large-scale production. This is because of the very high conversion efficiencies achieved and the lean production process.

Regarding the role of TCOs, three aspects still need to be addressed to boost SHJ technology's prospects of making additional inroads into the solar cell industry:

1. **Further improve cell performance.** This can be achieved by the implementation of high-mobility TCOs which are suitable for mass production. It was shown that high-mobility TCOs can be sputtered at high throughputs, and these TCOs were tested in SHJ solar cells. Although the CE of such SHJ cells is high, it still lags behind that of reference cells with the best ITO front TCO, despite a lower absorption and higher mobility. This is attributed to an increased contact resistivity of the TCOs with the n- and/or p-doped silicon contacts. Fine-tuning of the TCO and the implementation of contacting layers and/or interface optimization will need to be addressed in order to further reduce resistive losses at these interfaces and, thereby, reap the full benefits of the superior TCO properties.
2. **Reduce usage of scarce (and expensive) materials, particularly indium.** An attractive option for realizing a saving in material cost is to decrease the TCO thickness; this is even more attractive with costly high-conductivity (high-mobility) TCOs. However, another process step is needed to deposit a second, anti-reflective (capping), layer (ARC) on top of the TCO in order to reduce reflection losses. Alternatively, as shown in this paper, lower-conductivity TCOs (AZO in the example given) can be implemented in rear-junction solar cells without compromising on CE. This gains relevance where cost is concerned: in the analysis presented, ZnO-based targets demonstrate lower cost at \$0.6/cm<sup>3</sup> for target material, compared with \$2.6/cm<sup>3</sup> for In-based targets. The limited stability of AZO can be dealt with by, for example, capping it with a dielectric layer (a-SiO<sub>2</sub> or a-SiN<sub>x</sub>).
3. **Reduce PVD equipment costs.** Scaling and increasing the throughput of TCO production lines is the way to go, with DC sputtering being ready for high-throughput production of high-performance TCOs.



**Figure 8. Electrical properties of TCO layers sputtered at 4kW and 8kW from ceramic tube targets of TCO type 'Y', in the as-deposited state and after annealing for 30 min at 200°C in ambient conditions.**

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**“Scaling and increasing the throughput of TCO production lines is the way to go.”**



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**About the Authors**



Alexandros Cruz received his master’s in renewable energy systems from the Berlin Institute of Technology in 2013. From 2013 to 2016 he worked at SolarWorld in the Module Technology department, focusing on module processing R&D. He subsequently joined the Helmholtz-Zentrum Berlin to pursue his Ph.D., with a thesis topic on TCO implementation in SHJ solar cells.



Dr. Darja Erfurt received her Ph.D. from the Technical University of Berlin in 2019 for her work on high-mobility TCOs in chalcopyrite thin-film solar cells. She is currently a postdoctoral researcher at HZB, where she focuses on SHJ solar cells.

René Köhler has 10 years’ experience in the crystalline silicon PV industry, and began his career at SolarWorld Innovations, working on PERC and TOPCon/POLO. He then worked in the area of SHJ solar cells at the Helmholtz-Zentrum Berlin, before joining VON ARDENNE in 2018. He holds a Diploma degree in technical physics from the Technical University of Ilmenau.



Dr.-Ing. Martin Dimer received his Ph.D. from the Technical University of Braunschweig. Since 1996 he has been working at VON ARDENNE in various positions, including project manager, group leader and expert in the field of thin-film coatings based on PVD and PECVD technologies. Today, his main focus of activity is thin-film technology for PV.



Dr. Eric Schneiderlöchner began his career in PV in 2000 at Fraunhofer ISE, where he also worked on his Ph.D. He then gained 12 years’ experience in various engineering and management roles in solar cell manufacturing and process engineering at the former Germany-based solar company SolarWorld. He is currently the director of Crystalline Photovoltaics Technology at the German vacuum equipment provider VON ARDENNE GmbH.



Prof. Dr. Bernd Stannowski received his Ph.D. in 2002 from Utrecht University in the Netherlands. From 2003 to 2010 he worked in the PV industry and was involved in R&D on thin-film silicon solar cells, as well as in PV module production. Since 2010 he has been with the PVcomB at Helmholtz-Zentrum Berlin, where he leads the Silicon Solar Cells group.

**Enquiries**

Bernd Stannowski  
Helmholtz-Zentrum Berlin, PVcomB  
Schwarzschildstr. 3  
12489 Berlin, Germany

Tel: +49-30-8062-15491  
Email: bernd.stannowski@helmholtz-berlin.de  
Website: www.helmholtz-berlin.de, www.pvcomb.de

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## Solar PV capex trending at US\$9 billion annually as new GW fabs in China slash investments required

Capital expenditure (capex) for c-Si manufacturing (covering ingot/wafer and cell/module stages) is forecast at approximately US\$9 billion in 2019, consistent with levels seen during 2017 and 2018.

The largest part of this comes from cell equipment, accounting for just under half of c-Si PV capex, or about US\$4 billion per year during the period 2017-2019.

Capex operates with different drivers, compared to end-market demand within the PV industry. Various factors make capex analysis different also to those undertaken during the last major capex peak phase of 2010-2011. Capex is cyclic in nature and is also one of the best leading indicators of industry-wide downturns. One of the first things cut when cash is running out is capex, although (similar to R&D spending), some players up investments at this time.

One of the main factors keeping capex from growing today is the cost reduction seen for new capacity additions. GW levels of ingot/wafer plus cell/module capex is now running at about 15c/W, especially when dealing with the 5-10GW increments that new sites in China are being specified at.

It is now lower cost to build a new 5GW fab, than to retool five GW fabs with outdated (often p-multi) lines. This is the first time this has happened within the industry and suggests that we are in fact in a technology-buy phase, and not simply keeping old lines running at any cost.

Economy of scale from China-built capacity (using made-in-China equipment) has seen dramatic cost reduction in the past two to three years. The barrier-to-entry for Chinese players is not capex: it often depends on the technology chosen (copying p-mono PERC or trying something more challenging related to n-type) or being able to secure product sales (sometimes for cells, typically for modules).

Back in the last capex upturn of 2010-2011, a c-Si cell line was costing close to the 15c/W figure above (now covering ingots, wafers, cells and modules). Adding GW levels of integrated ingot-to-module capacity was costing about three to five times that of today. This is the main reason for overall PV capex (c-Si ingot-to-module) being lower today compared to 2010/2011 despite the huge increase in nameplate capacity being brought

online. Embedded within this of course are tool productivity improvements and line throughputs being much higher than before (not forgetting fab automation and efficiency/module-power improvements).

The low capex for p-type c-Si capacity (ingot to module) now makes n-type capacity (especially cell-based) a potential barrier-to-entry for Chinese manufacturers. This appears to be more emphasized for heterojunction, where PECVD tools alone can cost more than an entire p-type mono line.

Therefore, if the end-goal is to add 5-10GW of new capacity (which is becoming the new China standard), the extra capex for HJT quickly places constraints on spending plans. Therefore, it is no surprise that much of the argumentation from China for overlooking HJT today comes from capex, not the challenge of ramping lines with efficiency, distribution, and cost targets.

It is fairly easy for Chinese companies to justify not going for HJT today based purely on 'high capex' talk, but this is also coming from the acknowledgement that there is no low-cost China supply-chain anywhere near being in place.

Many of the initial wave of Chinese companies talking about HJT investments seemed to think that tapping into Sanyo's legacy process flow or tool supply-chain design would be a simple and effective route. Sanyo (Panasonic) designed its heterojunction production lines about 20 years ago – the world is a different place today.

In part, this is one of the issues behind the new push for the most standard n-type variant growing in popularity within China (PERT, TOPCon or other research-institute named process flows).

Therefore, the real impact of a technology buy-cycle driven by the top-10 module suppliers in China may not be seen from a production standpoint until 2021. However, just the fact that more of these leading players are moving on 500MW-to-1GW of new n-type capacity is probably the best leading indicator that n-type could be the real next-thing after p-mono PERC.

I noted in blogs on PV Tech in the past couple of years that it would be JinkoSolar's decision-making here that would be the key driver for n-type in China – this appears to be what is happening now and will certainly be on the rise during 2020/2021.





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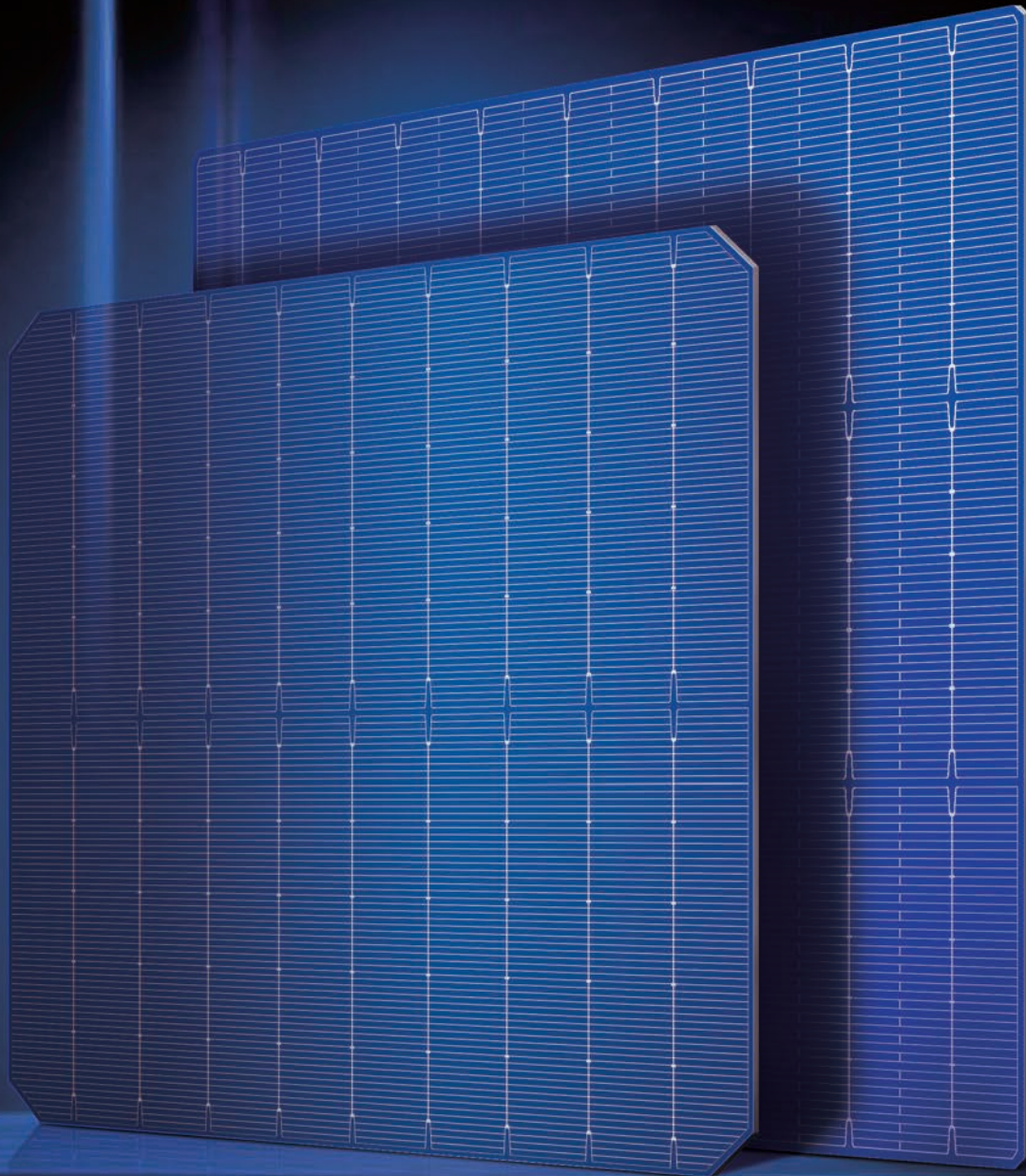


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