Ion implantation as an enabling technique for the fabrication of back-junction back-contact cells within a lean process flow

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ABSTRACT

Ion implantation offers significant process simplification potential for the fabrication of back-junction back-contact (BJBC) solar cells. First, the number of high-temperature steps can be reduced to one when applying a co-annealing process which includes an in situ growth of a silicon oxide passivation layer. Second, the implanted regions can be patterned in situ by utilizing shadow masks. ISFH's results from evaluating both aspects are reported in this paper. With fully ion-implanted, co-annealed and laser-structured small-area cells, efficiencies of up to 23.41% (20mm × 20mm designated area) have now been achieved. It is shown that the excellent recombination behaviour of 156mm × 156mm BJBC cells patterned in situ implies a potential for realizing efficiencies greater than 23%; however, back-end issues have so far limited the efficiency to 22.1% (full-area measurement). Ion implantation can also be utilized for the doping of BJBC cells with carrier-selective junctions based on polycrystalline silicon. The current status of ISFH's work in this direction is presented.

Introduction

High energy conversion efficiencies are currently becoming more and more important, since the increasing amount of balance of system (BOS) cost has to be offset [1]. Since its proposal in 1977 [2], the back-junction back-contact (BJBC) solar cell continues to be extensively investigated as a promising high-efficiency concept. The absence of optical shading from front-side metallization is considered the main advantage of BJBC solar cells, compared with double-side contacted cells. However, the recent progress achieved with more standard-type, potentially industrially feasible double-side contacted cells (e.g. > 21% efficiency for fully screen-printed p-type PERC cells [3,4]) puts pressure on the BJBC cell concept. Either the BJBC cell needs to be realized using a process flow that is as lean as that for double-side contacted cells, or additional process complexity has to be offset by additional benefits, in particular significantly higher energy conversion efficiencies. With regard to the first aspect, ion implantation can serve as an 'enabling technology', yielding a significant simplification of the BJBC front-end process. (The 'front end' of a BJBC cell process includes wafer cleaning, formation of doped regions and passivation.)

While ion implantation had already been investigated in the 1980s for PV applications [5–7], it regained significant research interest in 2010 [8] for two main reasons: first, high-current implanter tools became available, which were capable of the high throughput required in PV; and second, the capability for in situ patterning via shadow masks offered a potentially cost-effective way to form local doped regions. Although the latter aspect was first evaluated for the formation of selective emitters for double-side contacted cells [8], it was quickly applied to the fabrication of BJBC cells [9–11]. Efficiencies of up to 22.4% [9] for 5-inch industrial BJBC cells, and up to 22.1% [11] for 6-inch cells, were already demonstrated in 2012/2013; these efficiencies have very likely been limited by back-end issues. (The 'back end' of a BJBC cell process includes creation of contact openings and rear-side metallization.)

On a small area, industrial ion-implanted BJBC cells with 'conventional' (non-carrier-selective) junctions have demonstrated efficiencies of 23.41% [12]. BJBC cells with carrier-selective junctions have recently achieved record efficiencies of 25% and above [13–15]. In situ patterned ion implantation can also be utilized in the case of carrier-selective junctions based on polycrystalline Si, in particular.

In this paper important aspects relating to junction formation based on ion implantation for both monocrystalline and polycrystalline Si will first be presented. ISFH's current BJBC cell results will then be reported in the second part of the paper.

Junction formation

Doping of monocrystalline silicon by ion implantation

The ionized dopants are accelerated to energies of several keV and implanted into the c-Si wafer, where they transfer their energy by nuclear and electronic interactions to the Si lattice. Eventually, the dopants form an as-implanted profile, peaking at the projected range of a few tens of nanometres, while many Si atoms are driven out of their former lattice sites and thus become Si self-interstitials. This crystal damage must be annealed and the implanted dopants have to be incorporated into the silicon lattice ('dopant activation') by high-temperature treatment.

In microelectronics, it is important to activate a major part of the dopants while maintaining a shallow doping profile: thus, only 'spike' anneals of a few seconds' duration are performed. These short annealing steps typically

do not yield a complete annealing of the crystal damage.

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By contrast, shallow doping profiles are neither required nor desirable for junctions in solar cells; rather, it is of utmost importance to sufficiently anneal the crystal damage in order to minimize recombination losses. Thus, longer annealing processes are required in PV than in microelectronics.

For boron (^{11}B) implants, which do not yield an amorphization of the surface for typical doses, the annealing of the crystal damage is not trivial [16]. During the first phase of the annealing process, the Si self-interstitials agglomerate to extended defects – first {311} clusters, which later evolve to dislocation loops [17]. The dislocation loops are very stable and only dissolve at temperatures above 900°C through the emission of Si atoms towards sinks, such as the wafer surface. Nevertheless, as first demonstrated by Benick et al. [18], it is possible to achieve recombination current densities as low as those for BBr_3 diffusion, indicating an almost complete annealing of implant-induced damage.

By comparing advanced process simulations [19] and experimental results, the thermal budget required for a sufficient annealing of boron implants was evaluated [20]. It was found that for an annealing temperature of 1050°C, durations of ~20min are required. For even higher annealing temperatures, which might be achievable with halogen-lamp-based rapid thermal processing (RTP), the annealing time can be significantly reduced (e.g. to 1min at 1200°C [20]). The good news regarding this rather high thermal budget is that the resulting doping profiles are completely determined by boron diffusion rather than by the shape of the as-implanted profile (Fig. 1(a)). Therefore, it is not necessary to precisely control the implant energy, which offers the possibility of simplifying and reducing the cost of PV implant tools.

There are several promising approaches to reducing the required temperature budget of the annealing process. For example, BF_2 instead of elementary boron can be utilized as the implant species: in this case, the wafer surface is amorphized, and the subsequent solid phase epitaxy supports the annealing process [21]. Alternatively, crystal defects can be restricted very close to the wafer surface by using low implant energies of down to 1keV [22]. After an incomplete annealing, e.g. at 950°C, the remaining defects can be removed by an etch-back of several tens of nanometres of Si [22]. The disadvantage of this approach is that it is not compatible with an in situ growth of a silicon oxide passivation layer during the annealing process. With this passivation scheme, emitter recombination current densities J_{0e} almost as low as with Al_2O_3 passivation were achieved (Fig. 1(b)). The fact that the J_{0e} values obtained with boron implants and subsequent annealing are comparable to the best reported in the literature for BBr_3-diffused boron emitters [23,24] shows the excellent annealing quality (Fig. 1(b)).

Phosphorus implants typically yield an amorphization of the wafer surface for doses above $10^{15}cm^{-2}$ [25]. Solid phase epitaxy takes place during the annealing process and removes a major part of the crystal damage. Thus, the annealing of phosphorus implants does not require temperatures as high as those in the case of boron implants. Annealing temperatures of around ~850°C are sufficient, which are comparable to those for a $POCl_3$ diffusion.

For BJBC fabrication, however, it

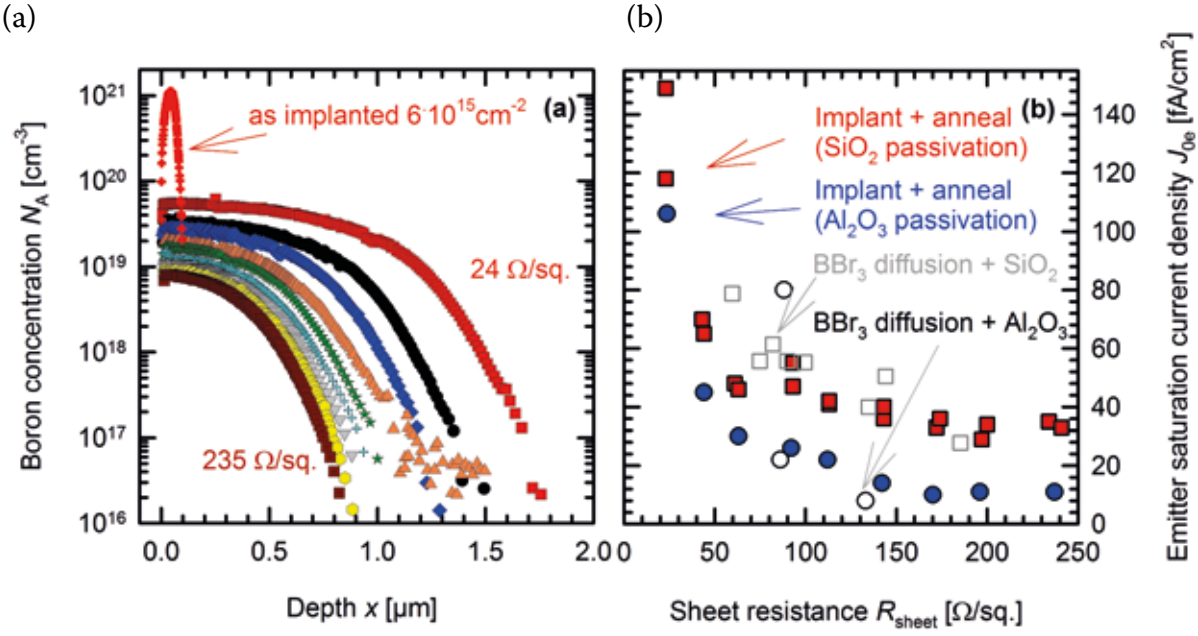

Figure 1. (a) Electrochemical capacitance-voltage (ECV) profiles of different boron emitters after implant and annealing. The implant dose is varied from $4·10^{14}cm^{-2}$ to $6·10^{15}cm^{-2}$, while the implant energy is kept constant at 10keV. For the highest dose, the as-implanted profile according to TRIM (transport of ions in matter) process simulation is shown. (b) Emitter saturation current densities for the emitters shown in (a). Different passivation schemes are compared – in situ grown SiO_2 and ALD-Al_2O_3. (Solid symbols refer to the authors' data for implanted and annealed samples, whereas open symbols refer to literature data for BBr_3-diffused emitters, according to Slade et al. [23] and Richter et al. [24].)

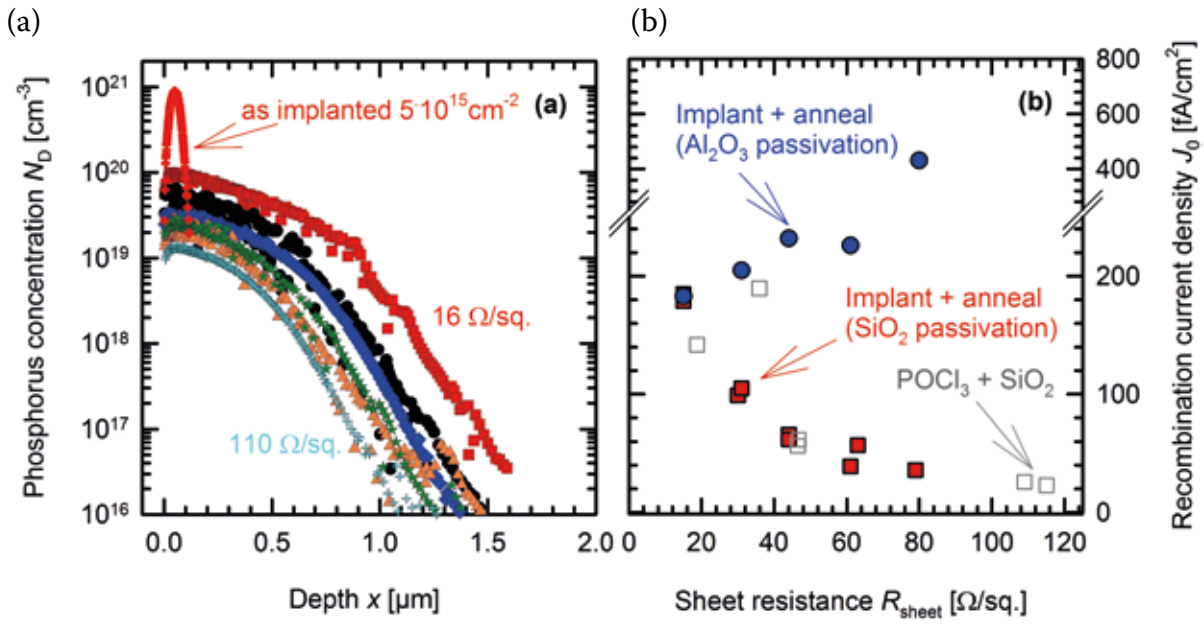

Figure 2. (a) ECV profiles of different phosphorus BSFs after implant and annealing. The implant dose is varied from 5·10^{14}cm^{-2} to 5·10^{15}cm^{-2}, while the implant energy is kept constant at 35keV. For the highest dose, the as-implanted profile according to a TRIM process simulation is shown. (b) Recombination current densities for the BSFs shown in (a). Different passivation schemes are compared – in situ grown SiO_2 and ALD-Al_2O_3. (Solid symbols refer to the authors' data for implanted and annealed samples, whereas open symbols refer to literature data for $POCl_3$ diffused and oxidized n$^+$ regions, according to Cuevas et al. [27].)

is desirable to anneal both implants in one co-annealing step. Obviously, the co-annealing temperature is determined by the requirements of the boron implant anneal, for example >20min at 1050°C (see above); thus, the resulting shape of the phosphorus-doping profiles is quite different from that of the $POCl_3$-diffused n$^+$ region (Fig. 2 (a)). As for boron, the as-implanted profile shape has almost no impact on the final doping profile.

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For screen-print metallization, the surface doping concentrations – ranging from 1·10^{19}cm^{-3} to 1·10^{20}cm^{-3} for sheet resistances from 109Ω/sq. down to 16Ω/sq. – seem quite low. With state-of-the-art Ag pastes, however, low specific contact resistances could possibly be achieved for these phosphorus profiles. In the case of metallization based on physical vapour deposition (PVD), specific contact resistances well below 1mΩcm^2 are achievable for these surface doping concentrations [26]. For silicon oxide passivation grown in situ during the annealing process, the J_0 values are comparable to the best reported in the literature [27] for $POCl_3$ diffusion and subsequent thermal oxidation (Fig. 2(b)). On the other hand, for Al_2O_3 passivation deposited by ALD (atomic layer deposition), the passivation achieved on the implanted back-surface field (BSF) regions (Fig. 2(b)) is rather poor. For increasing sheet resistance, the recombination current density also increases, a behaviour that is reminiscent of unpassivated doped surfaces.

Doping of polycrystalline silicon by ion implantation

An emerging candidate for carrier-selective junctions, which provides excellent passivation in metallized regions ('passivated contacts') as well, is a stack consisting of the monocrystalline (c-) Si wafer, a thin interfacial silicon oxide, and a highly doped polycrystalline (poly-) Si layer [28–31]. Fig. 3 shows a transmission electron microscopy (TEM) cross-section image of such a poly-Si/c-Si junction in high resolution. Ion implantation is well suited to doping of the poly-Si top layer [32–35]. Recombination current densities of down to 1fA/cm^2 after phosphorus implantation were recently achieved, and of down to 4.4fA/cm^2 after boron implantation in poly-Si [35]. The compatibility with local doping methods, such as ion implantation, might be the main advantage of poly-Si/c-Si junctions [14,15] for BJBC solar cell fabrication. However, it is fair to say that the current world record efficiency of 25.6% was achieved for a BJBC cell with carrier-selective junctions based on a-Si/c-Si heterojunctions [14].

A high-temperature anneal is required after implantation in the case of poly-Si/c-Si junctions as well. In contrast to implantation in monocrystalline Si, this annealing step is not necessary for the removal of implant-induced crystal defects. The poly-Si is anyway inherently highly defective. Since minority carriers are already blocked at the interface between the c-Si wafer and the interfacial oxide, recombination in the poly-Si is suppressed. Besides an electrical activation of the implanted dopants in the poly-Si, the high-temperature treatment also improves the passivation quality of the interfacial oxide and decreases the junction resistance [36]. The physical mechanism responsible for this improvement, however, is still under debate. One possible hypothesis is self-organized structural changes in the interfacial oxide, which might even lead to the formation of local pinholes [37,38]. In Fig. 3, it is at least obvious that the interfacial oxide thickness spatially varies between ~2 and ~4nm

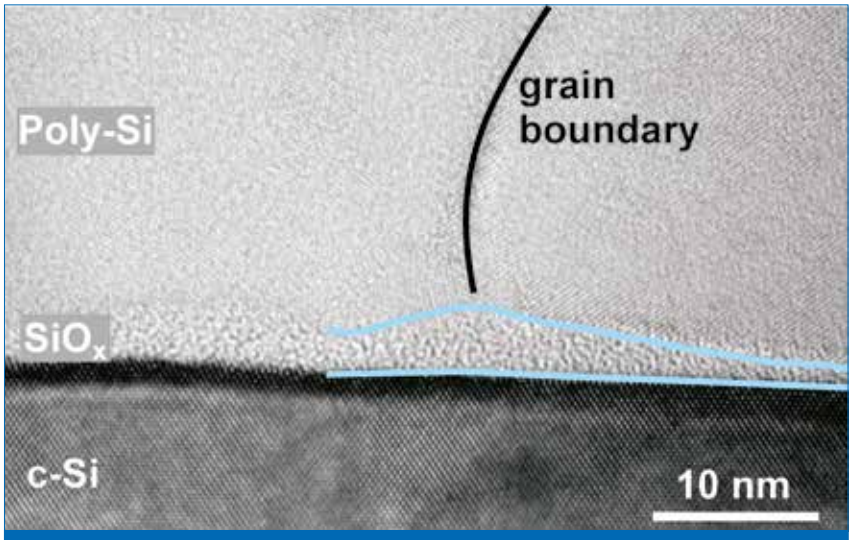

Figure 3. TEM cross-section image in high resolution, showing a poly-Si/c-Si junction with thermally grown interfacial oxide. The poly-Si was doped by phosphorus ion implantation, and received a subsequent high-temperature anneal. The variable thickness of the interfacial oxide is highlighted. The recombination current density of this sample is 1fA/cm².

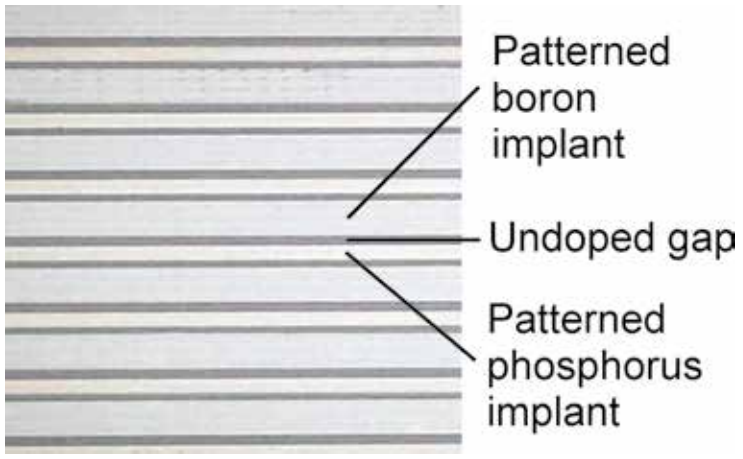

Figure 4. Optical microscope image of a wafer after two subsequent masked implant steps. The wider fingers were boron implanted using the first mask, and the narrower fingers were phosphorus implanted using the second mask. A narrow region was left intentionally undoped between both fingers. The images show the excellent implant-to-implant alignment.

after a high-temperature treatment of the complete stack, while the interfacial oxide itself was presumably grown with a uniform thickness in a short thermal oxidation. Pinholes might not be resolvable in TEM, because pinhole areal density is low. In any case, the temperature budget has to be adapted to the specific interfacial oxide [36] rather than to the implant conditions. Therefore, the optimum temperatures are typically lower than those required for the annealing of implant damage in c-Si: for wet-chemically grown oxides, temperatures of ~800–900°C are sufficient [36,39]. Temperatures that are too high certainly result in a perforation of the interfacial oxide and a significant increase in recombination current densities [36].

Depending on the poly-Si thickness, it might be challenging to accommodate the entire as-implanted profile in the poly-Si without damaging the interfacial oxide [32]; low implant energies are therefore required. Furthermore, it may be beneficial to utilize fairly heavy implant species with a low projected range – for example BF_2 instead of elementary boron, and arsenic instead of phosphorus.

The implant dose also affects the quality of the poly-Si/c-Si junction [32,35]. Interestingly, this is not only because of a different band bending (a different field effect passivation), but also because the passivation quality of the interfacial oxide is affected. For higher doses, a significant diffusion of dopants from the poly-Si into the c-Si occurs [32,35]. The optimum implant dose is different for boron and phosphorus, and depends on the thickness of the poly-Si.

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In situ patterning

One of the main advantages of ion implantation for BJBC solar cell fabrication is its capability of in situ patterning. Two approaches are possible:

1. One implant, for example the boron implant for emitter formation, could be performed all over the entire cell rear side. Only the second implant, for example the phosphorus implant for BSF formation, needs to be masked. The choice of appropriate implant parameters yields a local overcompensation of boron by phosphorus in the BSF regions ('counter-doping') [39].

2. Both implants could be masked. An undoped gap region can be maintained between emitter and BSF regions.

Although the first concept does not require implant-to-implant alignment, and therefore appears to be the simplest approach, implant-to-implant alignment is nevertheless feasible using state-of-the-art PV implanters, such as the SOLION XP tool from Applied Materials. Fig. 4 shows an optical microscope image of an implanted BJBC cell precursor. The wider finger was implanted with a first mask, and the narrower finger was implanted in a second step with another mask.

For implantation in monocrystalline Si, the first (counter-doping) concept works very well [39]. Although implanted n^+ and p^+ regions are in direct contact, the excellent annealing quality prevents a poor recombination behaviour due to trap-assisted tunnelling or to generation–recombination processes in the space charge region.

For implantation in poly-Si, the situation is different as a result of the inherently high defect density in the

poly-Si [35]. Thus, it is beneficial to leave an undoped region between the emitter and BSF fingers; this is possible with implant-to-implant alignment, corresponding to the second concept mentioned above.

Cell results

To achieve high energy conversion efficiencies in BJBC solar cells, it is important to form excellent p-n (high–low) junctions between the emitter (BSF) and the base, and to apply a rear-side passivation scheme which adequately passivates both polarities – emitter and BSF – as well as the p-n junction meander between these regions. The latter aspect is of particular importance for small BSF indices, which are necessary in order to minimize lateral transport losses of majority carriers in the Si bulk. In this case, the p-n junction meander length is fairly large. For these reasons, in situ grown silicon oxide passivation seems to perform better than ALD Al_2O_3 rear-side passivation [12], although the latter provides slightly better passivation quality on the emitter regions.

Fig. 5 shows the recombination behaviour (measured by photoconductance decay) of a 156mm × 156mm BJBC cell precursor after implantation, annealing and passivation. For this cell precursor, patterning is performed in situ via shadow masks in accordance with the counter-doping concept (see previous section). All three implants – phosphorus implant over the entire cell front side for front-surface field formation, boron implant over the entire cell rear side for emitter formation, and masked phosphorus implant on the cell rear side for BSF formation – are annealed within one co-annealing step that includes an in situ growth of a silicon oxide passivation. The high implied open-circuit voltage of 696mV and the high implied pseudo fill factor of 84.35% demonstrate the excellent quality of the ion-implantation-based front-end processing.

To estimate the efficiency potential, the following assumptions are made: a recombination current density in the metallized regions, $J_{0,met}$, of 1000fA/cm² for both polarities; a total metallized area fraction of 3.5% (PVD-based metallization); and an 'internal' series resistance (including the contributions from the base, emitter, FSF and BSF, as well as the specific contact resistance) of 0.3Ωcm². (The last of these values originates from numerical device simulations.) Accordingly, V_{oc} will decrease by 10mV upon contact opening and metallization, and the fill factor will

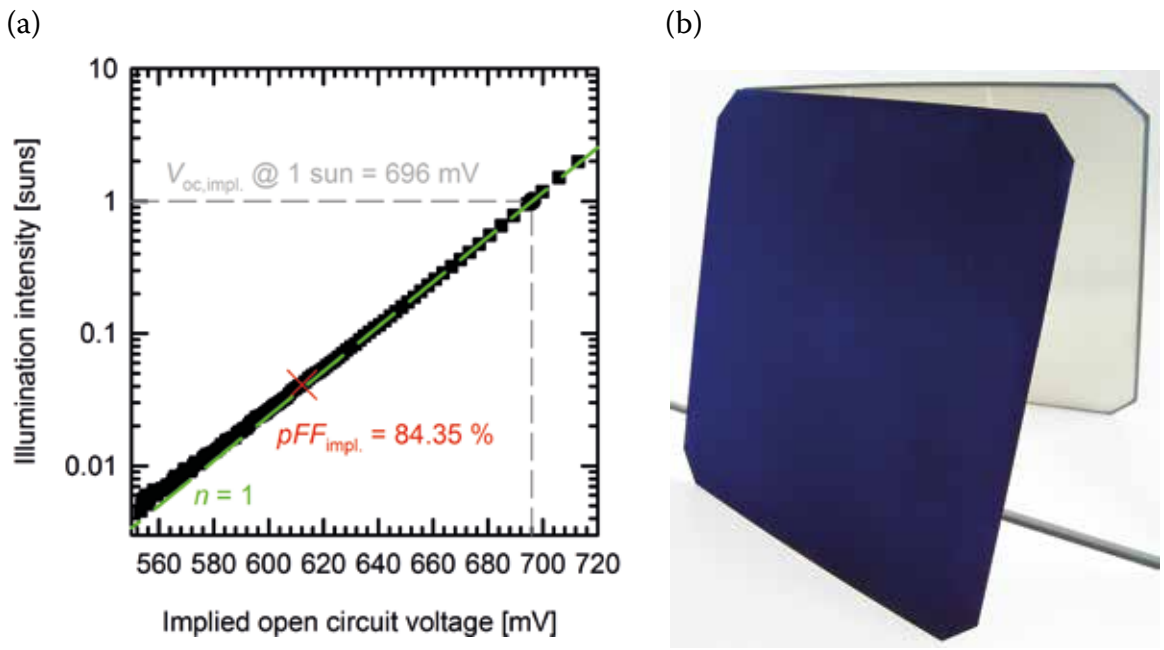

Figure 5. (a) Recombination behaviour of a 156mm × 156mm BJBC cell precursor after front-end (implantation, annealing, passivation) processing, as determined by photoconductance decay measurements. The high implied open-circuit voltage of 696mV and the high implied pseudo fill factor of 84.35% are indicated. The slope of the green dashed line corresponds to an ideality factor of one. (b) Photograph of a finished BJBC cell.

	Measurement	A [cm²]	η [%]	J_{sc} [mA/cm²]	V_{oc} [mV]	FF [%]
Large-area industrial BJBC conventional junctions	Full area	241*	22.1*	41.6*	676.2*	78.8*
Small-area industrial BJBC conventional junctions	Designated area	3.97**	23.41 ±0.47**	41.26 ±0.78**	692.8 ±2.4**	81.91 ±0.53**
Small-area industrial BJBC hybrid – conventional p⁺ emitter, n⁺ poly-Si BSF	Designated area	3.97*	22.2*	40.7*	690.6*	78.8*

*In-house measurement, **Independently confirmed by F-ISE CalLab

Table 1. ISFH's current record ion-implanted BJBC cells.

be 82.8%. For a short-circuit current density of 41.6mA/cm^2, the efficiency potential of this cell precursor is 23.6%.

ISFH's best cell result achieved so far on an industrial 156mm × 156mm BJBC cell, however, is 22.1%, as seen in Table 1. ('Industrial' denotes the absence of any pure laboratory techniques, such as photolithography: for example, besides in situ patterned ion implantation and co-annealing including in situ growth of silicon oxide passivation, contact openings are laser ablated, and metallization is performed using a high-throughput inline Al evaporation tool.) The main difference from the estimate of potential performance given earlier is the rather low fill factor of 78.5%. The fill factor loss is caused by resistive losses and an inhomogeneous potential distribution implied by the non-optimized rear-side metallization [40]. This back-end issue is independent of the junction formation method.

In order to screen out the back-end issue, small-area BJBC cells were also fabricated, which were measured on the designated area [12]. Here, co-annealing was also applied, including an in situ growth of oxide passivation, as well as laser ablation for contact opening formation. To allow a flexible evaluation of different device geometries, the doped regions were patterned by laser structuring rather than by shadow-masking the implant. The current record efficiency of 23.41% corresponds (to the authors' knowledge) to the highest value reported so far for a fully ion-implanted cell. This efficiency level can be transferred to large-area cells by utilizing an optimized, busbar-less rear-side metallization scheme, such as a simplified two-layer metallization [41].

For BJBC cells with poly-Si/c-Si junctions, significantly higher efficiencies are expected [33]: according to numerical device simulations, efficiencies above 25% are feasible. However, it will be necessary to adapt many process steps, such as the local laser ablation of a dielectric rear-side reflector on the rather thin poly-Si layer [42]. Because of these challenges, the best in-house measured efficiency for a small-area BJBC cell with n^+ poly-Si BSF regions and a conventional boron emitter is only 22.2% (Table 1). Nevertheless, a significant improvement is expected once the emitter has also been realized via a poly-Si/c-Si junction, and all related process issues have been resolved.

> "For ion-implanted BJBC cells with poly-Si/c-Si junctions, efficiencies of the order of 25% appear to be feasible."

Conclusions

Ion implantation can be utilized for the formation of excellent junctions in monocrystalline Si, as well for the doping of polycrystalline Si for emerging carrier-selective poly-Si/c-Si junctions. For boron and phosphorus implantation in monocrystalline Si and subsequent co-annealing, recombination current densities as low as the best reported in the literature for diffusion-based junctions were achieved.

In the case of BJBC cells with conventional junctions, since both polarities – the n^+ doped BSF and the p^+ doped emitter, as well as the p-n junction meander in between both regions – have to be passivated, silicon dioxide seems to be the best rear-side passivation scheme. This passivation layer can be grown in situ during the annealing process. The capability for in situ patterning is the main advantage of ion implantation for BJBC cell fabrication, resulting in significant process simplification potential. It is possible to mask just the second implant for a local overcompensation of the first implant, or to mask both implant steps, with an excellent implant-to-implant alignment.

For BJBC cells with conventional junctions in monocrystalline Si, the excellent recombination behaviour after the implant-based front-end processing indicates an efficiency potential well above 23%. With small-area BJBC cells, this potential is almost fully exploited, with a current record efficiency of 23.4%. For large-area cells, however, the back-end issues have been limiting up to the present moment: the highest efficiency obtained so far for an industrial 156mm × 156mm BJBC cell is therefore 22.1%, but further optimization of the rear-side metallization could greatly improve this result. For ion-implanted BJBC cells with poly-Si/c-Si junctions, efficiencies of the order of 25% appear to be feasible.

Acknowledgements

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