On the fabrication of high-efficiency mc-Si PERC-based solar cells on diamond wire-sawn surfaces using industrially viable etching technologies

Bishal Kafle[1], Pierre Saint-Cast[1], Ahmed Ismail Ridoy[1], Sebastian Nold[1], Jonas Schön[1,2], Marc Hofmann[1], Jochen Rentsch[1],Laurent Clochard[3], Edward Duffy[3], Klaus Duncker[4], Kai Petter[4], Stefan Peters[4]
[1]Fraunhofer Institute for Solar Energy Systems ISE, Heidenhofstraße 2, 79110 Freiburg, Germany; [2]University of Freiburg, Department of Sustainable Systems Engineering, Emmy-Noether-Straße 2, 79110 Freiburg, Germany; [3]Nines Photovoltaics, IT Tallaght, Dublin 24, Ireland; [4]Hanwha Q Cells GmbH, Sonnenallee 17-21, 06766 Bitterfeld-Wolfen OT Thalheim, Germany

Abstract

Improving the texturing approach for diamond wire-sawn (DWS) multicrystalline silicon (mc-Si) wafers is one of the key steps to decrease its efficiency gap with monocrystalline silicon-based solar cells. In this regard, black silicon texturing has increasingly caught attention of both academia and industries as a potential approach towards mass production of high-efficiency mc-Si solar cells. In this paper, the challenges of implementing such a texture, with unique feature sizes, in mass production are discussed in detail, and the latest results are reviewed. Finally, results of the first trials at high volume manufacturer applying an alternative plasma-less dry-chemical etching (ADE) method are presented.

Introduction

A significant cost reduction in wafering is possible through the adoption of diamond wire (DW) sawing for monocrystalline (mono-Si) and multicrystalline (mc-Si)-based solar cells. The major advantages of using the DW-sawing method are its low Si kerf loss during sawing, and lower operational costs by avoiding the use and management of a complex slurry mixture [1]. However, in spite of the above mentioned benefits, the switch from standard multi wire slurry sawing to DW-sawing is slower for mc-Si wafers in comparison to mono-Si wafers. The reason for this slower transition for mc-Si is mainly because of the problem associated with the incompatibility of the conventional wet-chemical texturing process. Consequently, an easy adoption of diamond wire sawing aided with a gradually easing out supply constraint of the mono-Si wafer has significantly decreased its price gap with the mc-Si wafer.

Lately with the advent of additives, which can be added in the HNO_3/HF bath during the wet-chemical texturing process to form similar surface texture as in slurry-type wafers, conventional texturing processes can continue to be used for DW mc-Si. The cost increment in texturing by including additives has been reported to be non-significant by some industrial players. During the ongoing paradigm shift towards gigawatt deployment of photovoltaics (PV), however, the final cost per watt-peak of the module or system and eventually the levelized cost of electricity (LCOE) are becoming more important than just the price of a cell or module. This implies that increasing the conversion efficiency (η) and power output of mc-Si based cell technologies to reduce the efficiency gap with mono-Si based cell technologies is essential to keep its current market dominance.

The influence of the mono- and mc-Si based cell efficiency on watt-peak costs of the solar module and the system is summarized in Figure 1. In both cases, current capital and operational costs (CAPEX/OPEX) for a green-field investment were calculated for standard processing steps used in industrial manufacturing of passivated emitter and rear cell (PERC) concepts. Current spot market prices for DW-sawn wafers [2] are used for the calculation.

In Figure 1, cell efficiency-driven cost benefits are obvious for both mono- and mc-Si based PERC modules and systems. On the module level, a difference in cell conversion efficiency $\Delta\eta <$ 1.5% absolute is required for mc-Si PERC against mono-Si PERC in order to benefit through lower costs per watt-peak. On a system level, area-related costs per watt peak decrease with an increase in conversion efficiency, which means that the maximum allowed difference in cell efficiency for mc-Si will reduce to $\Delta\eta$ = 1.2%. For instance, mc-Si PERC solar cells with η > 20.8% would still compete on a system level in comparison to the mono-Si PERC cells with η = 22.0%. Going to the LCOE level, the allowed differences in the conversion efficiency are influenced by many other factors such as temperature coefficient and low-light performance of the modules that are not only technologically but also location specific, and therefore are not further discussed here.

In summary, achieving higher efficiency was never more important for mc-Si than in the current scenario in order to retain its competitive edge against mono-Si. Two of the major frontiers for increasing the conversion efficiency for mc-Si are: a) increasing the inherent bulk-material quality before and/or during the cell processing, and b) increasing the light absorption in the mc-Si wafer by surface texturing to achieve better anti-reflective and light trapping properties. In the former, researchers from both academia and industry are working on: a) improving crystallization and base-doping processes to produce high-quality wafers with low dislocation density, reduced impurity concentration, narrow bulk resistivity distribution [3,4]; and b) increasing the bulk lifetime during the solar cell processing by employing bulk-passivation schemes such as advanced phosphorous gettering and hydrogenation [5,6], and can be read in detail in above cited publications. In this article, the latter would be discussed more in detail.

Using additive-based wet-chemical texturing for DW-sawn mc-Si leads to a high surface reflection, and therefore no efficiency gain to the conventionally textured slurry-type mc-Si wafers is to be expected. In this regard, the adoption of DW sawing could be used as the disrupting technology that presents an opportunity to introduce novel texturing concepts promising J_{SC} improvement in comparison to the state-of-the-art techniques in solar cell production. Some of the widely promoted novel etching methods enabling high cell efficiencies of 20% on DW-sawn mc-Si wafers [7][8,9] are reactive ion etching (RIE), metal catalysed chemical etching (MCCE) and atmospheric pressure dry chemical etching (ADE). A previous article in Photovoltaics International has summarized the principle as well as the pros and cons of these methods [10]. Apart from these technologies, recently researchers from SERIS have also reported an alternative undisclosed method of nano-scale texturing, claimed to be low-cost, metal free and allowing high efficiencies [11].

Out of these technologies, RIE is typically considered to have high capital and operational costs and therefore is still not widely applied in large-scale production despite being a fairly proven and tested process to form surface texture in mc-Si. In contrast, MCCE has quickly developed to be one of the major technologies to drive the production of nanotextured high-efficiency solar cells on DW-sawn mc-Si surfaces, although there are still challenges to overcome for this technology such as: expensive consumables, a likelihood of presence of trace metal particles, and most notably a cumbersome waste management. In the meantime, ADE has evolved as a texturing method that promises the advantages of RIE and MCCE in a more cost-effective and ecological manner. The advantages are summarized as: a) high etching rate and inline modular nature of the etching tool allowing high volume production; b) low cost of ownership (COO) due to no vacuum in the process; c) easy abatement of waste gases (SiF_x, F_2) through standard wet scrubber systems; d) use of environmental friendly F_2 gas with zero global warming potential (GWP); and e) purely chemical etching without any ion-induced damage in Si. First trials with high-volume cell manufacturers have started applying the ADE technology [12].

All of the above mentioned methods are reported to form surface structures with dimensions that are either smaller or comparable to the wavelength range of the visible light.

Depending upon the feature sizes, such structures are either able to lower the overall surface reflection in a large wavelength spectrum and/or cause higher order scattering to increase the overall path length and absorption probability of the longer wavelengths in the Si wafer. Detailed studies on optical modelling of nanostructures with different structure geometry and feature sizes can be read elsewhere [13–15]. By controlling the aspect ratio of these nano-scale structures during the texturing process, very low weighted surface reflection values have been reached on both mono-Si and mc-Si wafers by using all of the above mentioned fabrication methods. Such a wafer appears black in colour, hence called as black silicon (B-Si). Especially for DW-sawn mc-Si wafer, the final surface reflection achieved by forming black silicon is much lower than what is achievable by applying HNO_3/HF based wet-chemical method with additives. The introduction of such novel textures, however, demands successive optimization of the subsequent cell processing steps like emitter diffusion, passivation and metallization in order to fulfil the promise of an improved electrical performance. Some of the major technological challenges are briefly discussed here.

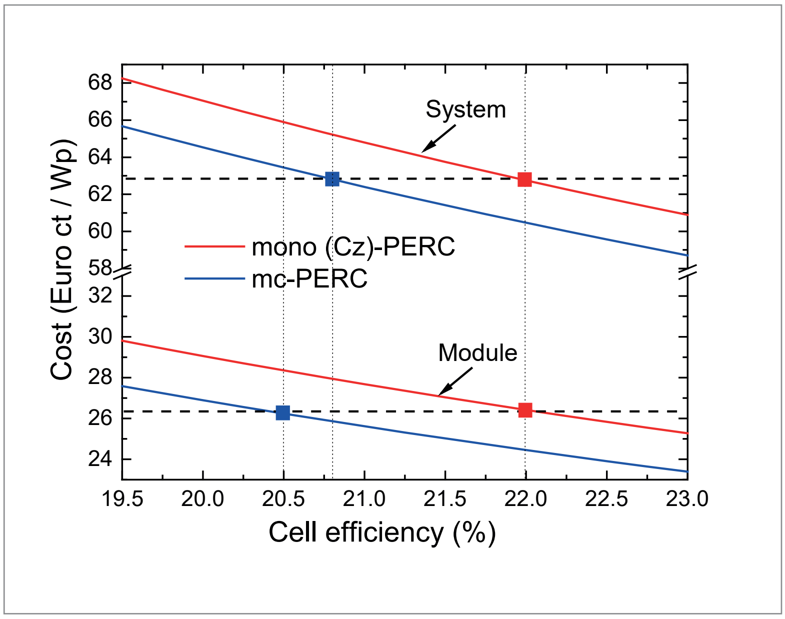


Figure 1. All-in PV module and system costs for mc PERC and Cz (mono-Si) PERC using standard PERC-process route for both types. One should note that the allowed efficiency gap $\Delta\eta$ between mc-Si and mono c-Si to reach equivalent costs decreases with increasing area-related costs. To reach a lower cost per watt-peak for mc-PERC in comparison to mono-PERC, $\Delta\eta$ <1.5% would be sufficient at the module level, whereas $\Delta\eta$ <1.2% is required on a system level.

Technological challenges of nanotexturing

The integration of such nano-scale texture in the standard cell processing sequence is not straightforward due to a significant difference in feature sizes compared to the structures that are formed by conventional wet-chemical texturing. Since texturing is one of the first steps in solar cell fabrication, each of the subsequent processes is significantly influenced by the introduction of nanotexture with unique surface features. Therefore, optimization of each of these process steps is required in order to fabricate efficient solar cells on nanotextured surfaces.

Optimal surface and emitter passivation

The application of a surface passivation layer reduces the minority carrier recombination in the surface. However, a large number of surface defects could remain un-passivated in the following conditions: i) the presence of surface structures that lead to a large surface area; ii) non conformality of the deposited dielectric layer; iii) higher stress-induced defects in the deposited passivation layer; and/or iv) crystal -orientation dependent recombination at the Si dielectric layer interface [16,17]. For such layers, the increase in recombination on nanotextured surfaces in comparison to the planar samples is accredited mostly to the difference in surface area ratio (S_f), which is experimentally calculated to be higher (S_f >2) in comparison to typical wet-chemical texture (for example $S_f \approx$ 1.5 1.7 for pyramid texture). However, an additional geometry dependent recombination component also has to be taken into consideration. Typical 'black' nanotextured surfaces show inverted conical geometry with a circular base radius in the range of 100-350 nm and depths in the range of 1 μm. In industrial facilities, plasma enhanced chemical vapour deposition (PECVD) is a preferred method of depositing dielectric passivation films, which, however, is not able to form a conformal coating on such structures. Meanwhile, excellently conformal coating of layers that are deposited by atomic layer deposition (ALD) allows reasonably low surface recombination velocities on rough surfaces like B-Si [18–20]. An example is shown in Figure 2 a) with the help of a cross sectional SEM image of ADE-formed black silicon that is deposited with a stack layer of ALD AlO_x/PECVD SiN_x.

However, industrial adoption of contemporary ALD tools is slow in PV. A quick work-around that is widely used to enhance the conformality of PECVD-layers on nanotexture is to perform a surface modification step either in alkaline or acidic solution to form modified nanotexture (M-Tex) with low S_f [21–28]. An example of such a modified nanotextured surface is shown in Figure 2 b), whereas the progression of etching and the consequent increase in weighted surface reflection (R_w) is shown in Figure 2 c). The weighted surface reflection (R_w) is calculated in the wavelength spectrum of 300-1,200 nm and a weighing function is applied using the internal quantum efficiency of a standard silicon solar cell and AM 1.5G illumination conditions [29].

Emitter diffusion process

Formation of nanotexture directly influences the emitter characteristics (total doping and emitter depth) and the homogeneity of the doping process. Insights on the nature of standard $POCl_3$-based tube diffusion on different nanotexture geometry can be obtained by performing 3-D predictive

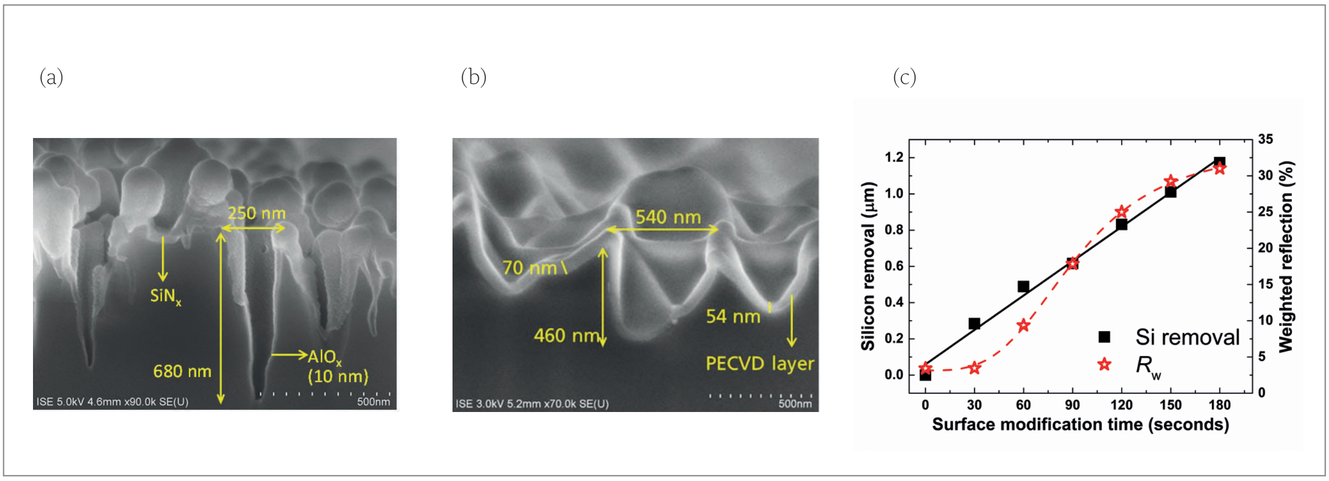


Figure 2. SEM cross sectional images of a) B Si after passivation with ALD AlO_x / PECVD SiN_x stack, and b) M Tex after passivation with PECVD SiriON/ SiN_x stack; c) plot showing increase in Si removal and surface reflection with an increasing duration of surface modification. In a) one should note that the thin ALD AlO_x forms very conformal layer in the nanostructure geometry, whereas conventional PECVD SiN_x layer is deposited mostly on the top-section of the texture and the valleys of the structures remain un passivated. In b), a conformal deposition of PECVD stack layers is achieved after surface modification.

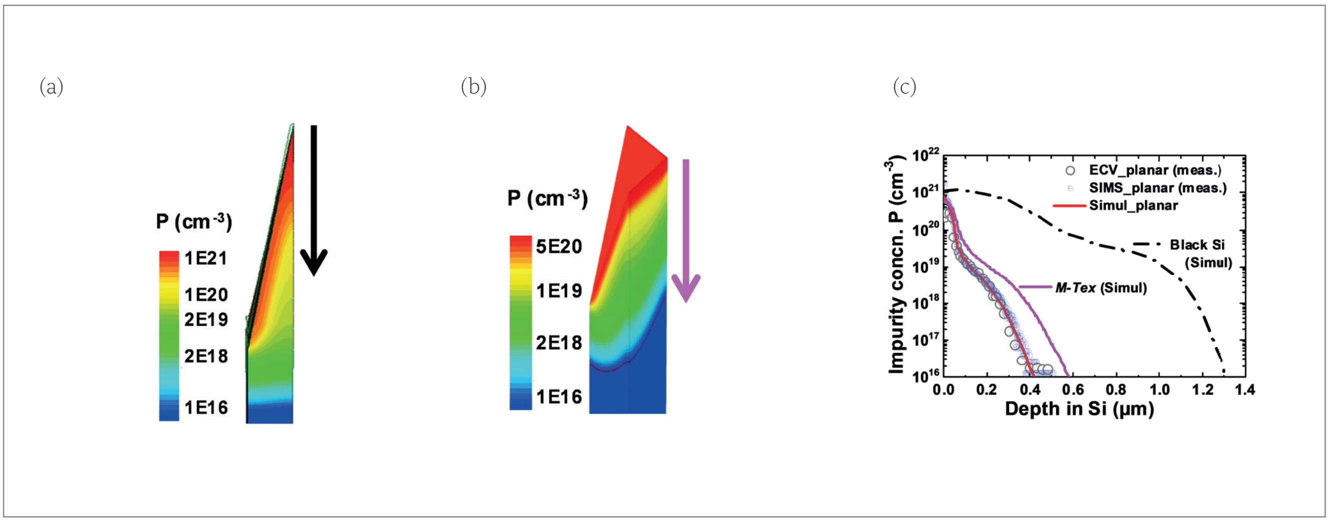


Figure 3. a) Process simulation of black silicon (B-Si) and modified texture (M Tex) showing a) cross section view of B-Si as (1/4th) nano pyramid, b) cross section view of M Tex as (1/4th) nano inverted pyramid; and c) a comparison of simulated active doping profiles of an identical emitter diffusion process on B-Si, M Tex and the planar surface. In c) 1D doping profiles are extracted for B-Si and M Tex from the 'peak' position in the direction perpendicular to the imagined planar surface, as shown by the arrows.

simulations of phosphorous in-diffusion in black-silicon (B-Si) and modified texture (M-Tex) using Sentaurus [30,31] and are presented in Figure 3. For the process simulations, M-Tex is considered to be an inverted pyramid structure with an aspect ratio of unity (width = 600 nm, depth =600 nm). Please note that B-Si has a width/height of 300 nm/1,000 nm. The dimensions are extracted from the SEM images of B-Si and M-Tex. Figure 3 a) and b) show the cross-sections of the symmetry elements of B-Si and M-Tex respectively, after the diffusion of an identical emitter. Here, different colours represent different doping regimes in the nanostructure. Figure 3 c) compares the simulated active P concentration profiles in B-Si and M-Tex surfaces that are extracted in 1 D from the peak position of nanostructures in the direction perpendicular to the imagined planar surface. For comparison, the total and active P doping profiles of the identical emitter in planar surface, which are respectively measured by using secondary ion mass spectrometry (SIMS) and electrochemical capacitance voltage (ECV) techniques, are also shown. Additionally, simulated active doping profile on planar surface is also plotted, which shows a good correlation between simulations and experiments.

In comparison to B-Si, surface modification (M-Tex surface) leads to a considerably lower active P concentration in the surface and bulk of the emitter, which means that the emitter optimization is less challenging for such surfaces. In the case of B-Si, the microscopic characterization and predictive process simulation suggest the formation of a relatively planar depletion region in comparison to the conventionally formed wet-chemical texture (acidic/pyramid) for an identical emitter diffusion. In contrast, after surface modification, the depletion region in M-Tex surface follows the nanostructure geometry very well. This indicates that an optimization of the emitter diffusion is needed for even a slight change in the surface morphology of nanostructures. In general, for all nanotextured surfaces, inclusion of an in situ oxidation process during the drive in step is found to be advantageous to avoid high doping in the emitter region. Meanwhile, the pre deposition process parameters (time, temperature, and $POCl_3$:N_2 flux) are very influential to lower the excess diffusion of both active and inactive dopants. Furthermore, it is observed that due to a large surface area, formation of nanotexture not only changes the degree of doping, but can also exacerbate the homogeneity of the emitter diffusion process. In this regard, adjustment of the pre deposition parameters is found to be crucial to improve the homogeneity of the diffusion processes.

Distribution of surface reflection on a mc-Si wafer

A mc Si wafer consists of grains of different crystal orientations. One of the challenges of the nano-scale texturing process is to maintain same etching properties in different crystal orientations. In the case of the dry etching method that uses ion-induced excitations such as in RIE, it is possible to etch all crystal orientation in the same way to leave a homogeneously etched surface with a low reflection [32,33]. The downside of such a process is the possible ion-induced damages in the crystal lattice of Si, which typically requires a defect-removal etching process before moving to further cell processing steps [33]. In other etching methods that are purely chemical in nature such as MCCE and ADE, process conditions have to be tuned to find a right balance between: a) differences in grain-grain etching, b) low surface reflection, and c) ease of integration in the subsequent cell processing steps. Especially in case of ADE, it has been observed that the starting surface before texturing plays a huge role in the grain-grain difference in reflection. An example of sister mc-Si wafers etched by applying two different ADE-based etching processes that differ mainly by process temperatures is shown in Figure 4. The corresponding weighted surface reflection measurements performed in six different grain orientations are also plotted. It can be observed that a more homogeneous texturing in different grain orientations can be achieved at a higher process temperature.

In case of MCCE, Ag nanoparticles are mostly used due to its high catalytic nature and cost-effectiveness in comparison to other noble metals such as Au and Pt [25]. However, Ag-MCCE process is also known to have crystal-orientation dependency in etching that results in some degree of etching inhomogeneity in the mc-Si wafer. In the meantime, Cu based MCCE process is shown to lack a preferential etching direction, which leads to less notable differences in morphology of nanostructures formed in different mc-Si grains [34]. Nevertheless, such a process is likely to be difficult to gain acceptance in large-scale PV manufacturing due to the likelihood of trace Cu nanoparticles in the wafer even after the cleaning process.

Meanwhile, for a less challenging integration of B-Si texture in emitter formation and PECVD deposition processes, typically the etched surfaces are further processed in an alkaline wet-chemical solution for a short duration as previously discussed (see Figure 2 b) and c)) [21,26,35,36]. In case of RIE-etched B-Si, such a post-treatment can also be used for defect-removal etching, i.e. etching of ion-induced defects and to modify the structures [33], or to remove the polymer layer formed during RIE [37]. The anisotropic etching behaviour of alkaline solution, however, leads to the formation of different surface morphologies in the grains with different orientations. Figure 5 b) shows a scan image of a typical B-Si textured mc-Si surface after post-treatment in the alkaline solution, showing a large distribution of reflection in the full-wafer area. SEM images of the darkest and the lightest grains of the mc-Si wafer, respectively in Figure 5 c) and d), show the formation of pseudo-pyramid-like structures with substantial differences in the aspect ratios, and hence the surface reflection values.

This large distribution of reflection not only directly limits the external quantum efficiency (EQE) and therefore the short circuit current density (J_{SC}) of the solar cell, but also cause concerns about the aesthetic appeal of the fabricated cell and module. Apart from optics, the optimization of emitter and PECVD deposition processes becomes challenging due to the difference in aspect ratio of nanostructures formed in different grains. The effect of such a large reflection distribution on electrical properties of the mc-Si solar cell is discussed more in detail in the later section of the article. In the meantime, applying acidic solution (HF/HNO_3) for post-treatment is being investigated to minimize the differences in morphology of nanostructures in different grains and thereby increase the J_{SC}. Apart from that, efforts on completely avoiding the post-etching steps are also being investigated for all of the above mentioned etching technologies.

Current status of high-efficiency mc-Si solar cells with nanotexture

The first step towards the application of nanotextured surfaces in high-efficiency PERC-type cells was to adapt them on conventional aluminium back-surface field (Al-BSF) architectures. The first investigations focused on understanding the challenges of integrating nano-scale structures in the subsequent cell processing steps date back as early as 2001 [38]. Extensive research into the fabrication of nanotexture on mc-Si surface and its

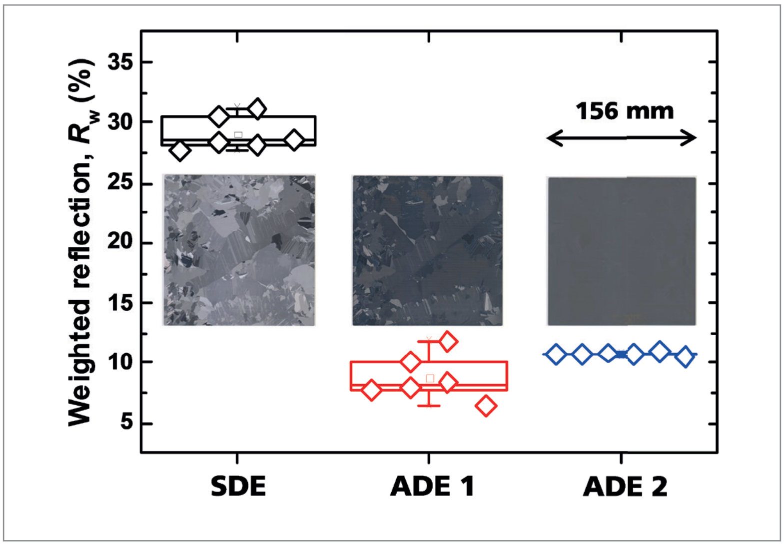
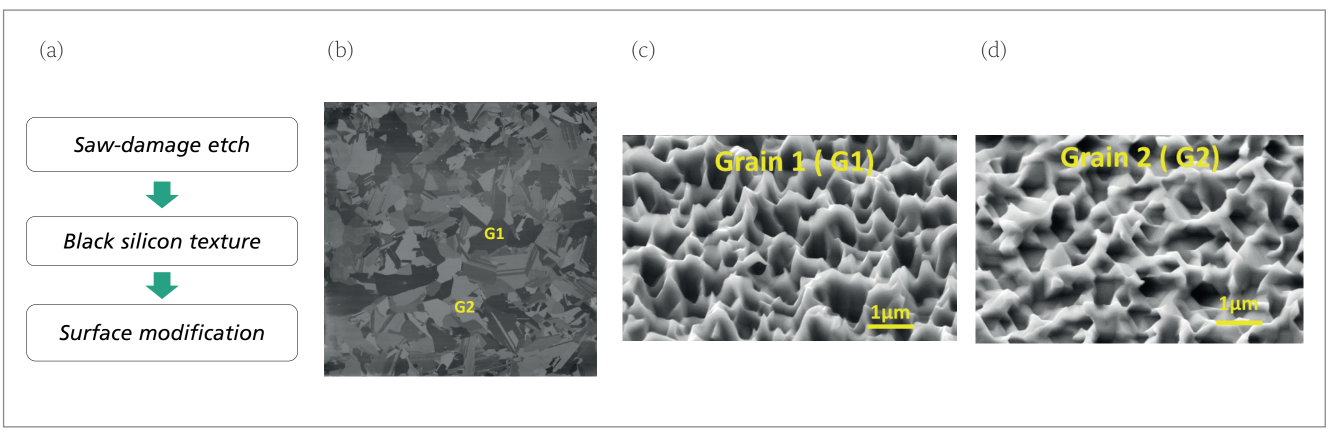


Figure 4. Plot comparing R_w measured in six different grains of the non-textured (saw-damage etched) and ADE textured mc-Si sister wafers, with inset showing scans of the wafers.

adaptation in standard solar cell process steps has since led to a steady increase in their conversion efficiencies [22,24,39][32,33,40]. Consequently, there exists a fairly large volume of literature dedicated to this topic, which cannot be covered in this article. Here, a brief review on the development towards mass production of nanotexture-based high efficiency DW-sawn mc-Si solar cells is presented.

First nanotextured mc-Si Al-BSF cells with η >18.0% and $\Delta\eta$ = 0.2-0.5% gain compared to iso textured surface were fabricated already in 2015 by employing all the above mentioned fabrication methods, namely MCCE, RIE and ADE [21,25–27,35,41]. In most of these studies, a post-etching step was applied after the black silicon texturing that is based on either alkaline or acidic solutions. Meanwhile, some studies also pointed out the possibility of avoiding this post-etching step completely and still reach comparable performances with MCCE [42] and RIE [37]. Promising results of black silicon-based Al-BSF cells paved the way to implement them in high efficiency PERC architectures and it coincided with the beginning of the phase where the PV industry needed solutions to texture diamond wire-sawn mc-Si wafers. Industrial-type high-efficiency mc-Si PERC solar cells with black silicon with efficiencies of 20% are announced by academia [8] and industry alike, culminating in the announcement of an mc-Si cell efficiency higher than 21.0% by Trina Solar with RIE [43], GCL with MCCE and RIE texture [44], and beyond 22% by JinkoSolar [45] by applying an undisclosed method of black silicon texturing. Although the details of the process steps and the associated cost-performance ratios are not disclosed, it definitely proves that mc-Si wafers would remain competitive to mono Si wafers in short and medium run. Mass production of MCCE-based mc-Si PERC cells with average efficiencies ≥ 20.5% are announced by some of the Tier 1 PV manufacturers citing a lower LCOE to that of commercially produced mono-Si-based modules [3,46]. The key towards mass production of black silicon textured cells has been the gradual adaptation of standard cell processing steps used in production facilities such as $POCl_3$ diffusion, PECVD passivation and screen-printing metallization with a strategy of making modest but continuous improvements in performance; rather than focussing only on novel disruptive technologies such as atomic layer deposition that might take some more time to become industrial standard. Two of the next steps to push the production efficiency beyond 21% are outlined as: a) lowering recombination and resistive losses in emitter and bulk, and b) use of advanced passivation schemes for texture with lower reflectivity. Recently, Fraunhofer ISE demonstrated η = 22.3% on small area using high quality n-type mc-Si material, black silicon texture and TOPCon cell concept [47] to further assert the case of mc-Si wafers to be considered with high efficiency cell architectures beyond PERC.

Figure 5: a) Typically used process flow for applying nanotextured surfaces in cell processing, b) scanned image of Gen.1 ADE-textured DW-sawn wafer and corresponding SEM images of pseudo-pyramid like structures formed in two grains – c) Grain 1 (G1) with lowest reflection and d) Grain 2 (G2) with highest reflection properties in the mc-Si wafer shown in b).

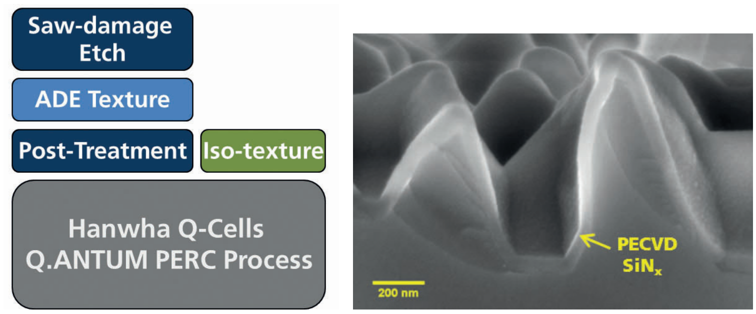


ADE-based mc-Si PERC solar cells

Formation of nano-scale structures on mc-Si surfaces by using ADE and their successful integration in Al-BSF type mc Si solar cells is already achieved and discussed in past publications [27,48]. Here, we briefly discuss the integration of different generations of ADE textured p-type mc-Si wafers in passivated emitter and rear cell (PERC)-type architectures [9]. ADE-based texturing does not distinguish between slurry and DW-sawn mc-Si surfaces and show comparable etching results. In the first generation, slurry-sawn high performance (HP) mc-Si wafers are chosen to see the potential of ADE-texture in terms of achievable V_{OC} and J_{SC} values. The process plan for first-generation mc-Si solar cells is shown in Figure 6 a).

The reference group of wafers is acidically textured in an HF/HNO_3 solution to reach typical weighted reflection values (R_w) of 26-27%. The test group of wafers is first saw-damage etched and then textured using the ADE process, during which the wafers are dynamically transported in an inline mode through the reaction chamber of the ADE tool with the process described elsewhere in detail [48]. After formation of B-Si, a short post-treatment in an alkaline solution is performed in the process described in Figure 2 c) to reach the average weighted surface reflection of 18%. The ADE-textured and the reference groups are subjected to $POCl_3$-based tube diffusion to form an n-type emitter. No significant differences in the emitter sheet resistance (R_{SH}) values are observed between the test and reference groups. Afterwards, the rear side emitter is removed. It has to be mentioned that since ADE is a single-sided process, the rear side is essentially flat. Therefore, typically used rear-sided polishing can be modified to just remove the rear-side emitter. Afterwards, the Q.ANTUM process [49] of Hanwha Q-Cells is applied to prepare PERC solar cells. Illuminated I-V measurements are performed under the standard test conditions using an in-house solar simulator that is calibrated with the Fraunhofer ISE CalLab reference. The results are presented in the table in Figure 6. The best solar cells of both test and reference groups are measured independently by Fraunhofer ISE CalLab and are also listed.

ADE-textured solar cells show an average conversion efficiency η = 20.0%, which is +0.2% absolute higher than the reference iso-textured solar cells fabricated on same material in this batch. The champion solar cell reaches 20.1%. The gain in η is solely because of a higher J_{SC} value of ADE textured solar cell pertaining to a lower surface reflection and an improved light trapping in comparison to the reference solar cell. An equivalent V_{OC} of test and reference groups suggests no significant electrical losses on test cells due to the surface and emitter recombination of the charge carriers. Furthermore, the nanotextured surface facilitates a low contact resistance between the emitter and screen-printed Ag grid [50], thus leading to an equivalent FF to the reference groups in this batch. Figure 7 shows the high resolution (200 μm) surface reflection mapping at 405 nm wavelength of an ADE textured solar cell, which is measured using a light beam-induced current (LBIC) method using a PV Tools Loana system.



(c)

Texture type	Value (# cells)	V_{oc} (mV)	J_{sc} (mA/cm²)	FF (%)	η (%)
ADE	Avg. (12)	659	38.2	79.5	20.0
ADE	Best*)	660	38.4	79.4	20.1
Reference	Avg. (15)	658	37.9	79.5	19.8
Reference	Best*)	660	37.9	79.4	19.9

Figure 6. a) Process plan for mc-Si PERC solar cells, b) SEM image showing example of a conformal deposition of PECVD SiNx on nanostructures formed in a mc-Si wafer after applying ADE etching and surface-modification step, c) table showing I-V parameters of the ADE and reference iso-textured groups with base resistivity $\rho_b \approx 1.8\ \Omega$ cm. Cell area is A_{cell} = 15.6×15.6 cm² and all cells feature solder pads, *) independently measured by Fraunhofer ISE CalLab.

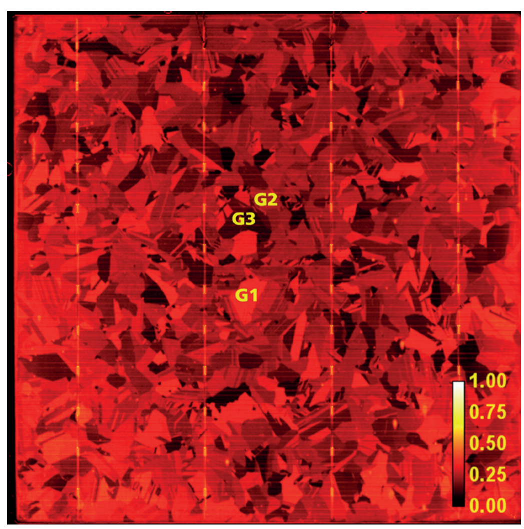


Figure 7. Reflection scan at 405 nm for ADE textured solar cell, with inset showing reflection and three different grains – G1,G2,G3; where local quantum efficiency measurements are also performed using PV-tools Loana system for the wavelength spectrum of 300-1200 nm.

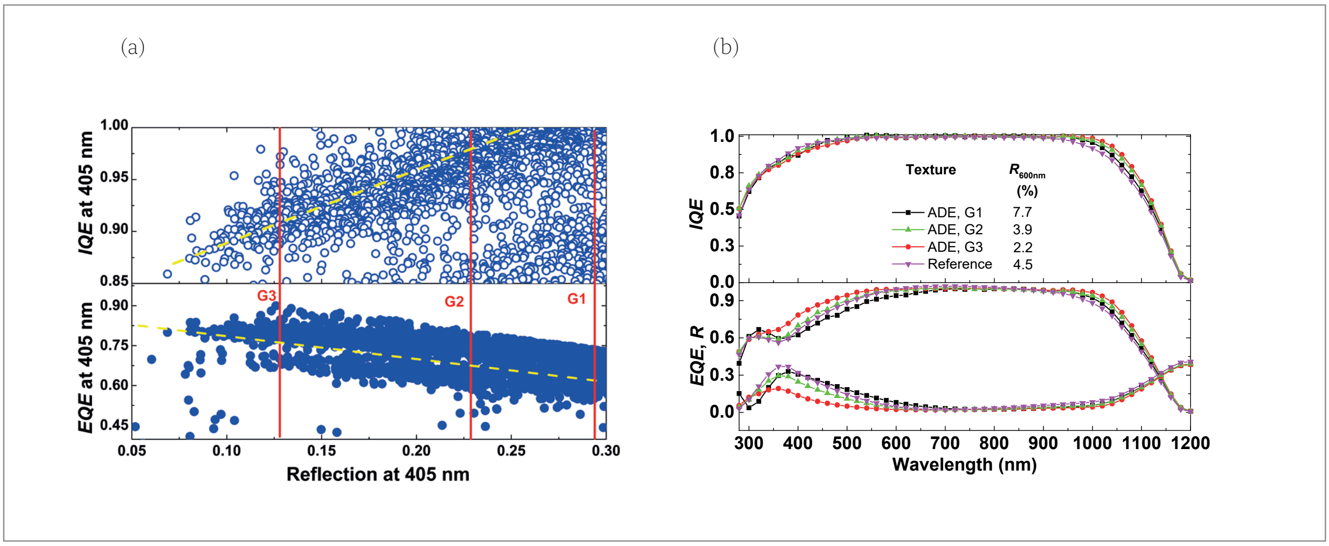
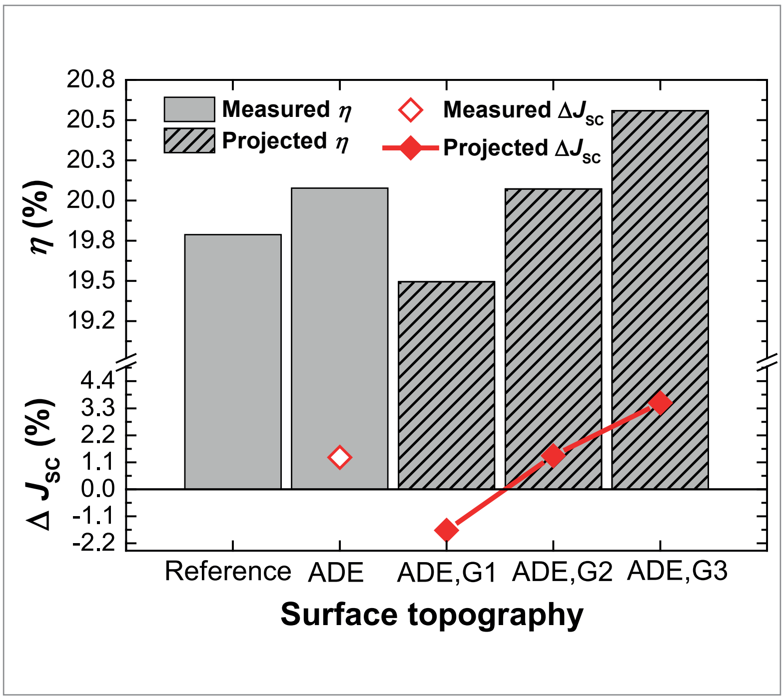


Figure 8. a) plot showing IQE and EQE of ADE-textured solar cell against corresponding reflection values at 405 nm, and b) locally measured IQE, EQE and R for three different grains G1,G2,G3 in a), showing reflection values at 600 nm. In a), the full red lines show the positions of G1, G2 and G3; whereas the dashed yellow lines serve as guides for eye.

A large distribution of reflection values can be observed in ADE textured solar cell, mainly due to the problems associated to the anisotropic nature of the post-etching process.

The influence of surface reflection on EQE and IQE of the ADE textured solar cell at 405 nm is depicted in Figure 8 a).

Here, lower reflection values correspond to higher EQE values, following a noisy but an overall linear relationship. The plot also suggests that lowering the reflection, however, still negatively impacts the IQE of the solar cell at short wavelengths until a certain value of surface reflection is reached after which the IQE saturates to its highest value. In order to have a more detailed understanding of this matter, local measurements of IQE/EQE/R are performed in three different mc-Si grains. Based on the LBIC reflection mapping in Figure 8 b), grain 1 (G1), grain 2 (G2) and grain 3 (G3) were chosen as the areas representing highest, moderate and lowest reflection values respectively in the full-area of an ADE textured solar cell with measured reflection values R_{600nm} of 7.7%, 3.9% and 2.2% respectively at 600 nm. In comparison, R_{600nm} of 4.5% is measured for the reference textured solar cell. Please note that the reflection of Ag is not subtracted during the estimation of reflection values. It can be seen that only G2 and G3 EQE values predict a gain in J_{SC} value to the reference texture in the wavelength spectrum of 300-700 nm and 900-1100 nm. Meanwhile, G1 predicts a loss in J_{SC} value due to a higher reflection than the reference texture. No significant losses in IQE are observed at short wavelengths for ADE texture of all types in comparison to the reference texture. Therefore, it can be maintained that the surface and emitter recombination are not significantly limiting the electrical parameters of the ADE textured solar cells that are fabricated in the current batch. In fact, a higher IQE for ADE-texture in comparison to the reference texture is



Caption Figure 9. Plot showing projected percentage change in J_{SC} (ΔJ_{SC}) and corresponding in comparison to the reference texture, considering a homogeneous ADE texture of either of type G1, G2 or G3 respectively along the full area of the solar cell. In addition, measured of best reference and ADE textured solar cells and measured ΔJ_{SC} (%) of best ADE-textured solar cell are also shown.

observed at longer wavelengths (λ >950 nm) possibly due to higher scattering of these wavelengths at front-texture. This phenomenon is subject to further investigations.

We estimate the relative percentage change in J_{SC} value of ADE textured solar cell in comparison to the reference, assuming a homogeneous texture G1, G2 or G3 across the whole wafer area, with the following equation:

$$J_{SC} = q \int_{\lambda=280}^{\lambda=1200} \phi(\lambda) \times EQE(\lambda)\, d\lambda,$$

where q is the elementary charge of an electron and $\phi(\lambda)$ is the incident photon flux.

Figure 9 plots the measured and projected percentage change in J_{SC} (ΔJ_{SC}) of ADE texture to that of best reference textured solar cell based on this calculation.

The measured ΔJ_{SC} for the best ADE textured surface is +1.3% higher in comparison to the best reference textured solar cell. Grain 3 (G3) is found to have the maximum difference between measured and calculated values of ΔJ_{SC} in ADE-textured wafer (ΔJ_{SC}=+3.5%). This corresponds to an absolute enhancement potential of up to +0.8% in conversion efficiency to the reference texture without any further optimizations in emitter diffusion and surface passivation.

By evaluating Gen.1 ADE-textured mc-Si PERC solar cells, it became evident that the next steps required in further increasing the J_{SC} of ADE-textured cells should focus both on lowering an overall reflection as well as to narrow the spatial distribution of reflectivity. This requires evaluating the ADE-texturing process, and most importantly the impact of the post-treatment step on different mc-Si grains. In the next generations (Gen.2 and Gen.3), collective optimization of ADE and post-etching processes is performed on DW-sawn mc-Si wafers in order to achieve best optical and electrical performances in the cell-level. Figure 10 a) shows the scan image of Gen.3 ADE-textured DW-sawn mc-Si wafer, which shows a narrow distribution of reflection in the whole wafer-area. The etching process is developed to obtain spherical cap-like structures with dimensions of 1 µm. Such characteristic dimensions are expected to cause high scattering of the middle and long wavelengths of visible light, leading to an improved light trapping in comparison to sub-micron wavelength structures. In Figure 10 b), an SEM image of a boundary region of three grains in the Gen.3 ADE-textured surface is shown. The etching process developed for Gen.3 ADE texture leads to the formation of spherical cap-like structures homogeneously in all crystal orientations of the mc-Si wafer. In this particular wafer, the weighted surface reflection measured along the full-wafer area is in the range of 14-17% after the texturing process.

Figure 11 depicts histograms comparing the distribution of reflection values at 405 nm for the full wafer area of ADE textured samples of different generations after PECVD SiN_x anti-reflective coating, which are extracted from the Loana tool. For comparison, reflection data of industrially applied additive-based texture after SiN_x coating is also included.

One should note a significantly smaller reflection distribution for Gen.3 ADE texture in comparison to previous generations. This improvement in reflection distribution is achieved in just two iterations of process optimization. In comparison to the additive-based wet-chemical texture on DW-sawn wafers, Gen.3 ADE texture shows both lower average reflection values as well as a comparable reflection distribution in the full wafer area. Using Gen. 3 texture, we expect to further increase the conversion efficiency ($\eta \approx 20.5\%$) for DW-sawn mc-Si PERC in upcoming cell batches.

Summary

DW-sawn mc-Si wafers can now be textured to a satisfying level by using additives in conventional wet-chemical processing, leading to similar reflection as the isotexturing process used for slurry-type mc-Si wafers. However, increasing the efficiency of mc-Si-based solar cells is essential to keep it competitive against the mono-Si based technologies in system and LCOE levels. Black silicon texturing has received an increased attention from academia and industries alike due to its promise to boost the current and conversion efficiency of DW-sawn mc-Si solar cell. Some technologies that are getting mature for large scale production are MCCE, RIE and ADE, although RIE method is considered to have higher capital and operational costs. Due to their unique feature sizes, nano-scale texturing poses major challenges in standard cell fabrication steps, mainly in surface passivation and emitter diffusion. These challenges are met by modifying the surface in a post-treatment step after formation of black silicon that, however, could lead to a large reflection and colour distribution in a mc-Si wafer. To mitigate this problem, strategies are being implemented in the direction of either applying a more isotropic post-etching step or to completely avoid this additional step altogether. Stepping on the massive research in this area, black silicon based mc-Si PERC solar cells with efficiencies >20.0% are beginning to be mass produced by solar cell manufacturers. ADE method of black silicon texturing is presented to be an alternative to MCCE and RIE due to its technological and ecological advantages. Already in the first trials in the industrial pilot-line of high-volume manufacturer, efficiencies of 20% are achieved on ADE-textured mc-Si PERC architecture.

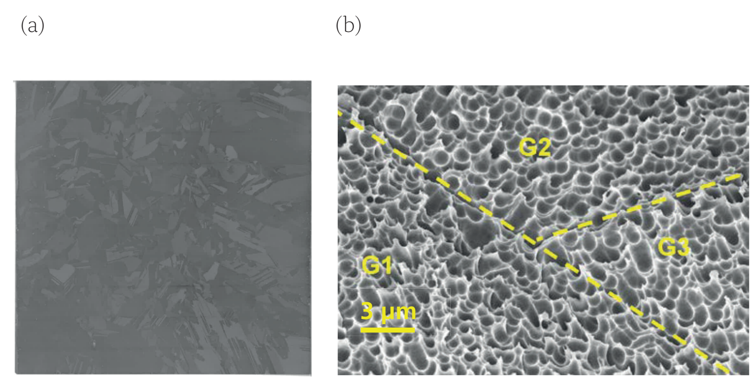


Figure 10. a) Scan image of Gen.3 ADE-textured DW-sawn wafer, b) SEM image showing tilted cross-section view of the boundary region of three grains (G1,G2,G3) in a).

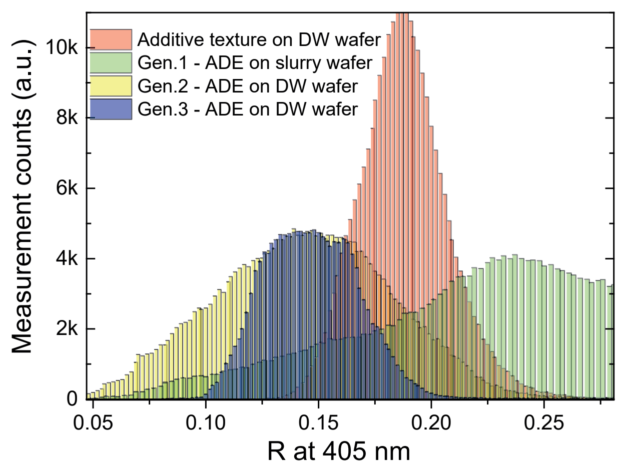


Figure 11. Histograms showing distribution of reflection at 405 nm in the full wafer area for different generations of ADE texture, in comparison to the additive-based acidic texture on DW-sawn wafer. Please note that, for all samples, reflection measurements are performed after applying PECVD SiN_x ARC layer on textured surfaces.

Acknowledgements

This work is partly funded by the federal ministry for economic affairs and energy (BMWi) of Germany within the project APPI under the contract number 0325895A. Project APPI is supported under the umbrella of SOLAR-ERA.NET Cofund by Agence de l'Environnement et de la Maîtrise de l'Energie, Project management Jülich, Technology Strategy Board and Centro para el desarollo tecnológico. SOLAR-ERA.NET is supported by the European Commission within the EU Framework Programme for Research and Innovation HORIZON 2020 (Cofund ERA-NET Action, N° 691664). The authors would like to thank all co-workers at photovoltaics department of Fraunhofer ISE, especially Elisabeth Schaeffer and Felix Martin for their help in solar cell characterization.

References

[1] B. Meinel, T. Koschwitz, C. Blocks, J. Acker, Comparison of diamond wire cut and silicon carbide slurry processed silicon wafer surfaces after acidic texturisation, Materials Science in Semiconductor Processing 26 (2014) 93–100.

[2] http://pvinsights.com/ (accessed on August 3, 2018).

[3] Yuepeng Wan, Differentiated High Performance Silicon Materials for High Efficiency Solar Cell and Modules, in 12th SNEC PV Power Expo (2018).

[4] C.W. Lan et al., in International PVSEC-25, Busan, South Korea (2015).

[5] H.C. Sio, S.P. Phang, P. Zheng, Q. Wang, W. Chen, H. Jin, D. Macdonald, Recombination sources in p-type high performance multicrystalline silicon, Jpn. J. Appl. Phys. 56 (8S2) (2017) 08MB16.

[6] B. Hallam, D. Chen, M. Kim, B. Stefani, B. Hoex, M. Abbott, S. Wenham, The role of hydrogenation and gettering in enhancing the efficiency of next-generation Si solar cells: An industrial perspective, Phys. Status Solidi A 214 (7) (2017) 1700305.

[7] Shu Zhang, Yang Yang, Daming Chen, Weiwei Deng, Hongwei Huang, Pietro P. Altermatt, Jianmei Xu, Zhiqiang Feng and Pierre J. Verlinden, 19.86% Aperture Efficient World Record P-type Multi-crystalline Module with 20.59% Efficient PERC Solar Cells, in 44th IEEE Photovoltaic Specialists Con-ference, Wahington D.C., United States (2017).
[8] J. Jin, H. Shen, P. Zheng, K.S. Chan, X. Zhang, H. Jin, >20.5% Diamond Wire Sawn Multicrystalline Sili-con Solar Cells With Maskless Inverted Pyramid Like Texturing, IEEE J. Photovoltaics 7 (5) (2017) 1264–1269.
[9] B. Kafle, A. I. Ridoy, P. Saint-Cast, L. Clochard, E. Duffy, K. Duncker, K. Petter, M. Hofmann, J. Rentsch, Atmospheric Pressure Dry Texturing Enabling 20% Conversion Efficiency on Multicrystalline Silicon PERC Solar Cells, in Silicon PV, Lausanne (2018).
[10] J. Rentsch, B. Kafle, M. Hofmann, K. Krieg, M. Zimmer, Texture etching technologies for diamond-wire-sawn mc-Si solar cells, Photovoltaics International 38 (2018).
[11] Armin Aberle, Global trends in crystalline silicon photovoltaics, in SNEC PV Power Expo (2018).
[12] Press release, Nines Photovoltaics, May 25th 2018.
[13] Hitoshi Sai, Homare Fujii, Koji Arafune, Yoshio Ohshita, Yoshiaki Kanamori, Hiroo Yugami, and Masa-fumi Yamaguchi, Wide-Angle Antireflection Effect of Subwavelength Structures for Solar Cells, Jpn. J. Appl. Phys. 46 (6A) (2007).
[14] H. Sai, Y. Kanamori, K. Arafune, Y. Ohshita, M. Yamaguchi, Light trapping effect of submicron sur-face textures in crystalline Si solar cells, Prog. Photovolt: Res. Appl. 15 (5) (2007) 415–423.
[15] A.J. Bett, J. Eisenlohr, O. Hohn, P. Repo, H. Savin, B. Blasi, J.C. Goldschmidt, Wave optical simulation of the light trapping properties of black silicon surface textures, Optics express 24 (6) (2016) A434-45.
[16] K.R. McIntosh, L.P. Johnson, Recombination at textured silicon surfaces passivated with silicon diox-ide, J. Appl. Phys. 105 (12) (2009) 124520.
[17] C. Schwab, A. Wolf, M. Graf, N. Wöhrle, S. Kühnhold, J. Greulich, G. Kästner, D. Biro, R. Preu, Re-combination and Optical Properties of Wet Chemically Polished Thermal Oxide Passivated Si Surfac-es, IEEE J. Photovoltaics 3 (2) (2013) 613–620.
[18] G. von Gastrow, R. Alcubilla, P. Ortega, M. Yli-Koski, S. Conesa-Boj, Fontcuberta i Morral, Anna, H. Savin, Analysis of the Atomic Layer Deposited Al2O3 field-effect passivation in black silicon, Solar Energy Materials and Solar Cells 142 (2015) 29–33.
[19] M. Otto, M. Kroll, T. Käsebier, R. Salzer, A. Tünnermann, R.B. Wehrspohn, Extremely low surface recombination velocities in black silicon passivated by atomic layer deposition, Appl. Phys. Lett. 100 (19) (2012) 191603.
[20] P. Repo, A. Haarahiltunen, L. Sainiemi, M. Yli-Koski, H. Talvitie, M.C. Schubert, H. Savin, Effective Passivation of Black Silicon Surfaces by Atomic Layer Deposition, IEEE J. Photovoltaics 3 (1) (2013) 90–94.
[21] F. Cao, K. Chen, J. Zhang, X. Ye, J. Li, S. Zou, X. Su, Next-generation multi-crystalline silicon solar cells: Diamond-wire sawing, nano-texture and high efficiency, Solar Energy Materials and Solar Cells 141 (2015) 132–138.
[22] D.Z. Dimitrov, C.-H. Lin, C.-H. Du, C.-W. Lan, Nanotextured crystalline silicon solar cells, Phys. Status Solidi A 208 (12) (2011) 2926–2933.
[23] X.X. Lin, Y. Zeng, S.H. Zhong, Z.G. Huang, H.Q. Qian, J. Ling, J.B. Zhu, W.Z. Shen, Realization of im-proved efficiency on nanostructured multicrystalline silicon solar cells for mass production, Nano-technology 26 (12) (2015) 125401.
[24] J. Oh, H.-C. Yuan, H.M. Branz, An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures, Nat Nano 7 (11) (2012) 743–748.
[25] X. Ye, S. Zou, K. Chen, J. Li, J. Huang, F. Cao, X. Wang, L. Zhang, X.-F. Wang, M. Shen, X. Su, 18.45%-Efficient Multi-Crystalline Silicon Solar Cells with Novel Nanoscale Pseudo-Pyramid Texture, Adv. Funct. Mater. 24 (42) (2014) 6708–6716.
[26] Z. Yue, H. Shen, Y. Jiang, W. Chen, Q. Tang, J. Jin, T. Pu, J. Luo, F. Kong, C. Rui, J. Cai, Large-scale black multi-crystalline silicon solar cell with conversion efficiency over 18 %, Appl. Phys. A 116 (2) (2014) 683–688.
[27] B. Kafle, A. Mannan, T. Freund, L. Clochard, E. Duffy, M. Hofmann, J. Rentsch, and R. Preu, Nanotex-tured multicrystalline Al-BSF solar cells reaching 18% conversion efficiency using industrially viable solar cell processes, Phys. Status Solidi RRL 9 (8) (2015) 448–452.
[28] B. Kafle, T. Freund, A. Mannan, L. Clochard, E. Duffy, S. Werner, P. Saint-Cast, M. Hofmann, J. Rentsch, and R. Preu, Plasma-free dry-chemical texturing process for high-efficiency multicrystalline silicon solar cells, Energy Procedia 92 (2016) 359–368.
[29] J. Zhao, M.A. Green, Optimized antireflection coatings for high-efficiency silicon solar cells, IEEE Trans. Electron Devices 38 (8) (1991) 1925–1934.
[30] B. Kafle, J. Schön, C. Fleischmann, S. Werner, A. Wolf, L. Clochard, E. Duffy, M. Hofmann, J. Rentsch, On the emitter formation in nanotextured silicon solar cells to achieve improved electrical perfor-mances, Solar Energy Materials and Solar Cells 152 (2016) 94–102.
[31] J. Schön, A. Abdollahinia, R. Müller, J. Benick, M. Hermle, W. Warta, M.C. Schubert, Predictive Simu-lation of Doping Processes for Silicon Solar Cells, Energy Procedia 38 (2013) 312–320.
[32] J. Yoo, J.-S. Cho, S. Ahn, J. Gwak, A. Cho, Y.-J. Eo, J.-H. Yun, K. Yoon, J. Yi, Random reactive ion etching texturing techniques for application of multicrystalline silicon solar cells, Thin Solid Films

546 (2013) 275–278.
[33] G. Xiao, B. Liu, J. Liu, Z. Xu, The study of defect removal etching of black silicon for solar cells, Mate-rials Science in Semiconductor Processing 22 (2014) 64–68.
[34]J. Zha, T. Wang, C. Pan, K. Chen, F. Hu, X. Pi, X. Su, Constructing submicron textures on mc-Si solar cells via copper-catalyzed chemical etching, Appl. Phys. Lett. 110 (9) (2017) 93901.
[35] Y.F. Zhuang, S.H. Zhong, Z.G. Huang, W.Z. Shen, Versatile strategies for improving the performance of diamond wire sawn mc-Si solar cells, Solar Energy Materials and Solar Cells 153 (2016) 18–24.
[36]B. Kafle, T. Freund, A. Mannan, L. Clochard, E. Duffy, S. Werner, P. Saint-Cast, M. Hofmann, J. Rentsch, R. Preu, Plasma-free Dry-chemical Texturing Process for High-efficiency Multicrystalline Silicon Solar Cells, Energy Procedia 92 (2016) 359–368.
[37] S. Liu, X. Niu, W. Shan, W. Lu, J. Zheng, Y. Li, H. Duan, W. Quan, W. Han, C.R. Wronski, D. Yang, Im-provement of conversion efficiency of multicrystalline silicon solar cells by incorporating reactive ion etching texturing, Solar Energy Materials and Solar Cells 127 (2014) 21–26.
[38]S.H. Zaidi, D.S. Ruby, J.M. Gee, Characterization of random reactive ion etched-textured silicon solar cells, IEEE Trans. Electron Devices 48 (6) (2001) 1200–1206.
[39]B.T. Chan, E. Kunnen, M. Uhlig, J.-F.d. Marneffe, K. Xu, W. Boullart, B. Rau, J. Poortmans, Study of SF6/N2O Microwave Plasma for Surface Texturing of Multicrystalline (150 mu m) Solar Substrates, Jpn. J. Appl. Phys. 51 (2012) 10.
[40] Y. Liu, T. Lai, H. Li, Y. Wang, Z. Mei, H. Liang, Z. Li, F. Zhang, W. Wang, A.Y. Kuznetsov, X. Du, Nanostructure Formation and Passivation of Large-Area Black Silicon for Solar Cell Applications, Small 8 (9) (2012) 1392–1397.
[41] Y. Jiang, H. Shen, T. Pu, C. Zheng, Q. Tang, K. Gao, J. Wu, C. Rui, Y. Li, Y. Liu, High efficiency multi-crystalline silicon solar cell with inverted pyramid nanostructure, Solar Energy 142 (2017) 91–96.
[42]Z. Ying, M. Liao, X. Yang, C. Han, J. Li, J. Li, Y. Li, P. Gao, J. Ye, High-Performance Black Multicrystal-line Silicon Solar Cells by a Highly Simplified Metal-Catalyzed Chemical Etching Method, IEEE J. Pho-tovoltaics 6 (4) (2016) 888–893.
[43]Trina Solar Press Release, 2015.
[44] GCL System Integration Technology Co., Ltd. Solar MBU, GCL roadmap to mass production with 21% efficient multicrystalline PERC cells and 300W+ modules, in SNEC PV Power Expo (2018).
[45]JinkoSolar Press release, 2017.
[46] Guoqiang Xing, CELL AND MODULE TECHNOLOGIES FOR MULTI C-SI TO KEEP THE WINNING EDGE, in SNEC PV Power Expo (2018).
[47]J. Benick, R. Müller, F. Schindler, A. Richter, H. Hauser, F. Feldmann, P. Krenckel, S. Riepe, M. C. Schubert, M. Hermle, S. W. Glunz, APPROACHING 22% EFFICIENCY WITH MULTICRYSTALLINE N-TYPE SILICON SOLAR CELLS, in 33rd European PV Solar Energy Conference and Exhibition, Amsterdam, The Netherlands (2017).
[48]B. Kafle, J. Seiffe, M. Hofmann, L. Clochard, E. Duffy, J. Rentsch, Nanostructuring of c-Si surface by F2 -based atmospheric pressure dry texturing process, Phys. Status Solidi A 212 (2) (2015) 307–311.
[49] P. Engelhart, D. Manger, B. Klöter, S. Hermann, A.A. Stekolnikov, S. Peters, H.-C. Ploigt, A. Eifler, C. Klenke, A. Mohr, G. Zimmermann, B. Barkenfelt, K. Suva, J. Wendt, T. Kaden, S. Rupp, D. Rychtarik, M. Fischer, J.W. Müller, P. Wawer, Q.ANTUM – Q-CELLS NEXT GENERATION HIGH-POWER SILICON CELL & MODULE CONCEPT, in 26th European PV Solar Energy Conference and Exhibition, Hamburg, Germany (2012).
[50]B. Kafle, T. Freund, S. Werner, J. Schön, A. Lorenz, A. Wolf, L. Clochard, E. Duffy, P. Saint-Cast, M. Hofmann, J. Rentsch, On the Nature of Emitter Diffusion and Screen-Printing Contact Formation on Nanostructured Silicon Surfaces, IEEE Journal of Photovoltaics 7 (1) (2017) 136–143.

About the Authors

Bishal Kafle completed his MSc and PhD degree in microsystems engineering from Albert-Ludwigs University of Freiburg, Germany in 2011 and 2017 respectively. His PhD degree was related to developing novel texture for mono-and multi-crystalline Si wafers and integrating them into the further solar cell processing steps. At Fraunhofer ISE, his current research focusses on integration of novel textures on cell and module level, and optimizing processing steps for rear passivated solar cells.

Pierre Saint-Cast received an MSc degree in micro-and nanoelectronics from Joseph Fourier University, Grenoble, France, and an engineering degree from the Polytechnic Institute of Grenoble, both in 2007. In 2012, he received his PhD from the University of Konstanz, in Germany. Since 2008 he has been with Fraunhofer Institute for Solar Energy Systems, Freiburg, Germany. His research interests include the development of passivation layers for solar cell applications, the processing, analysis and analytical modelling of PERC solar cells.

Ahmed Ismail Ridoy received his MSc degree in optics and photonics from the Karlsruhe Institute of Technology (KIT) in 2014. Currently he is conducting his doctoral research at the Fraunhofer ISE. His doctoral research focuses on the development of novel non-plasma dry texturing technique alternative to the industrially-standard texturing technique for passivated emitter and rear multicrystalline silicon solar cells.

Sebastian Nold studied industrial engineering at the University of Karlsruhe, Germany, and the University of Dunedin, New Zealand, and earned his diploma in industrial engineering at Karlsruhe in 2009. He has been working at the Fraunhofer ISE since 2008 in the field of cost calculation, technology assessment and economic evaluation of new concepts in the production of silicon solar cells. Sebastian is currently completing his doctoral thesis at the ISE on the economic assessment of silicon solar cell production along the PV value chain.

Jonas Schön received a diploma in physics from the University of Hamburg, Germany, in 2006 and a PhD degree from the University of Constance in collaboration with Fraunhofer ISE in 2011. Currently, he is a scientist in the department of sustainable systems engineering (INATECH) of the University of Freiburg and the Fraunhofer ISE. His research interests include simulation of impurities in silicon, cell processing and novel solar cells.

Marc Hofmann is Head of the Plasma Technology group at Fraunhofer ISE. In 2003, he received a diploma degree in electrical engineering from the University of Applied Sciences Koblenz, Germany, and a Ph.D. degree in physics from the University of Konstanz, Germany in 2008. His research is focussing on thin film and etching processes for high-efficiency crystalline silicon solar cells.

Jochen Rentsch is head of department production technologies – Surfaces and Interfaces at Fraunhofer ISE. He received his PhD degree in physics in 2005 from the Albert-Ludwigs University of Freiburg, Germany. He studied physics at the Technical University of Braunschweig and obtained his diploma degree in 2002. At Fraunhofer ISE, his research focuses on the development of rear passivated solar cells, new wet and dry chemical processing technologies and the coordination of cell technology transfer projects.

Laurent Clochard is the chief technical officer (CTO) at NINES PHOTOVOLTAICS since 2010, with a focus on developing a novel industrial dry etching tool and process (ADE), specifically designed for the solar industry. Prior to that, Laurent held positions in equipment companies (TEL Magnetic Solutions, Alyxan) where he was in charge of the product R&D and transition from research to industrial product, as well has CNRS. Laurent holds a B.Sc. of Thermal & Energy science from IUT Poitiers (France), an MSc in Physics from University La Rochelle (France), an MSc research in applied physics from Trinity College Dublin (Ireland), and a DEES Post-Master degree from Joseph Fourier University Grenoble (France).

Edward Duffy is the founder and CEO of NINES PHOTOVOLTAICS. He has been involved in semiconductor capital equipment business since 1996, at companies including TEL Magnetic Solutions and Applied Materials, where he held a number of senior positions both at their installed base at Intel Fab Operation (IFO) in Ireland and other facilities in Israel and the US. These positions included senior equipment engineer in the metal etch cluster and Installation and Qualification (I/Q) Lead Engineer/System Expert for HDP CVD (High Density Plasma Chemical Vapour Deposition) cluster. Edward holds a bachelors of science degree in engineering from Trinity College Dublin (TCD) and a diploma in mechanical engineering from the Dublin Institute of technology (DIT).

Klaus Duncker is senior expert in the department R&D Processes Frontend at Hanwha Q CELLS. He is responsible for the deposition processes of dielectric passivation layers on front and rear side. Klaus studied physics at the Universities of Kiel and Marburg and received a Ph.D. degree from the University of Halle in 2008.

Kai Petter is senior manager of the department R&D Silicon at Hanwha Q CELLS' headquarter for technology and innovation in Germany. He is responsible for testing new silicon wafer technologies. Kai studied physics at the University of Hamburg and received a PhD degree from the University of Marburg in 2006.

Stefan Peters is director of the department R&D Processes Frontend at Hanwha Q CELLS´ headquarter for technology and innovation in Germany. He is in charge of the development of solar cell processes for texturing, cleaning, doping and layer deposition. Stefan studied physics at the University of Bielefeld and received a PhD degree from University of Constance in 2004.

Enquiries

Bishal Kafle | Phone: +49 (0)761 4588 5499 | e-mail: bishal.kafle@ise.fraunhofer.de