Wet processing trends for silicon PV manufacturing

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ABSTRACT

Wet processing can be a very high performing and cost-effective manufacturing process. It is therefore extensively used in Si solar cell fabrication for saw damage removal, surface texturing, cleaning, etching of parasitic junctions and doped oxide glass. PV manufacturers have succeeded in bringing down the cost of ownership of batch-type and in-line tools. The trend to back-side passivated solar cells requires cost-effective single-sided processing solutions. With the future pointing to ever-thinner silicon solar cells, handling these thin wafers in wet environments is a major challenge for any wet process. This paper reviews the major wet processing steps, emphasising some new developments and unknown issues, and provides a more general outlook on trends in wet processing.

Introduction

With the aim of realising aggressive future cost targets of 0.5 €/Wp put forward in strategic roadmaps [1], every step in the process sequence is under severe cost pressure. At the same time the search for higher efficiencies is on. This dual request calls for the build-up of thorough understanding and characterization of each process step. It can be expected that based on such knowledge, critical aspects can be improved, leading to higher cell efficiencies, while process specifications for non-critical aspects can be relaxed and offer cost savings. As wet processes play an important role in solar cell manufacturing, some solutions to these issues are presented, such as single-sided wet process sequences that can alleviate some of the concerns, assuming that throughput requirements can be maintained. There is also potential for novel wet processes. For example, Cu electroplated metallization could substitute Ag screen-printed metallizations, while high-performing passivating layers that require exquisite (wet) cleaning sequences could employ process know-how from ultraclean ULSI cleaning cycles.

Standard process sequence of Si solar cells and cost reduction opportunities

Silicon feedstock material

Wet processing is used in several stages of the silicon supply chain. Some wet

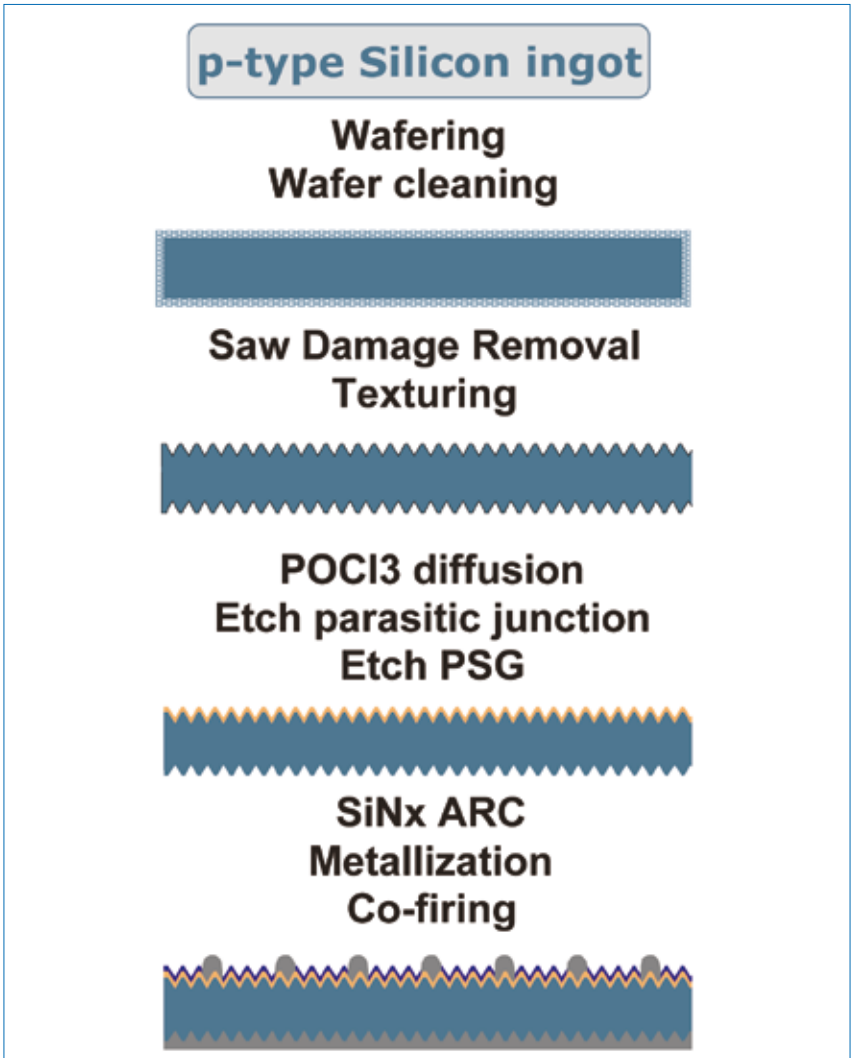

Figure 1. Standard industrial process flow for silicon solar cells.

treatments occur at the wafer producer side such as HNO_3-based cleaning of the pure silicon chunks prior to pulling or casting.

Wafering

The general manufacturing flow of a standard Si solar cell is depicted in Fig. 1. After the wire sawing process, the wafers are singulated from the silicon ingot and wet cleaning is applied. The abrasive slurry used in the sawing process can leave slurry and sawing residues, and metallic contamination left behind from the wire will eventually have to be removed from the wafers in the typically proprietary wafer cleaning process. At this stage, the wafers are shipped to the cell manufacturer.

At this point, the wafers are usually damaged to a depth of over 5 to 10µm by the mechanical wire sawing process and some metallic contaminants may also have diffused into the first few µm. This adversely affects the mechanical integrity of the wafer as well as the cell efficiency by recombination. Typically 10µm of damaged layer is removed in the saw damage removal (SDR) step by wet chemical etching (either in a alkaline or HF/HNO_3-based mixture) of the damaged layer.

Prior to applying the SDR, a wet cleaning step is performed to remove organic contaminants that may have deposited during shipping and storage and could (locally) mask or retard the SDR process. An alkaline mixture is usually used to lessen further damage to the silicon, in which case the surface should be free of all native oxides. Alternative organic removal solutions that could be more cost effective could be dilute HF/O_3-based cleans [2].

Texturing

The SDR step is immediately followed by the texturing process, which creates an intentional topography on the surface. The texturing is essential for reaching high efficiencies as it results in 'light trapping' inside the cell of the photons at the lower end of the energy spectrum, which might otherwise escape prior to being absorbed in today's thin wafers which are only 180 µm thick. The ideal topography of the textured surface is a critical trade-off between increased effectiveness of light trapping versus increased surface recombination.

With cost reduction in mind, the SDR and texturing processes are typically done in one process sequence. Two types of chemistry prevail, with best results obtained by an alkaline etch based on KOH (or NaOH) which

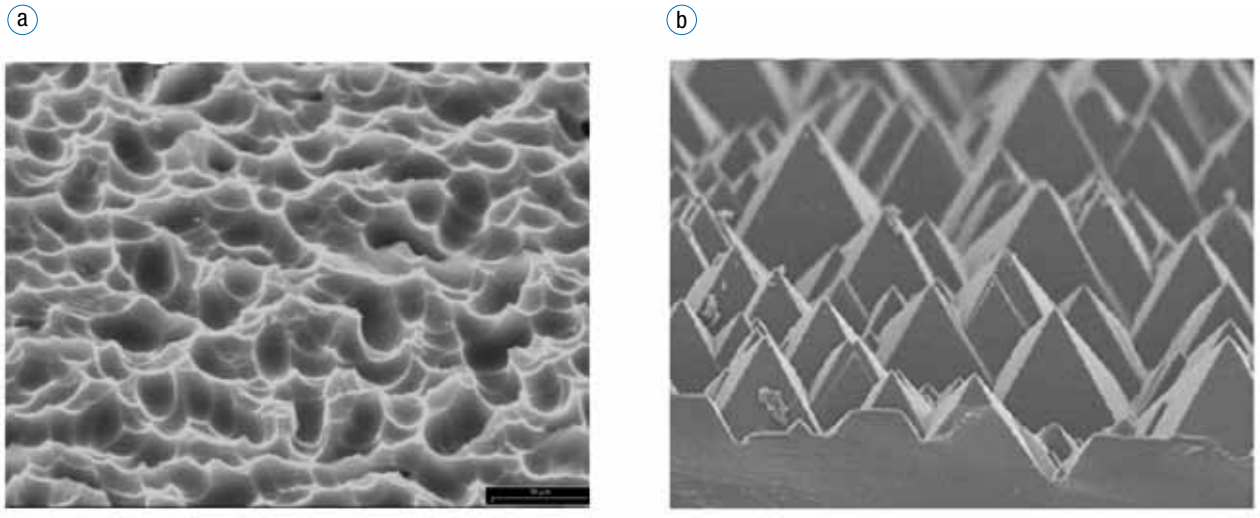

Figure 2. SEM pictures showing (a) random texture obtained after an isotropic etch in HF/HNO_3 mixtures and (b) random pyramids after an anisotropic etch in KOH solution.

etches silicon anisotropically and results in a random pyramid surface exposing only <111> planes (Fig. 2a). In practice, IPA is added to the solution at a temperature slightly above the boiling point of the IPA (which is recaptured in the solution).

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However, this process is only effective on (100) monocrystalline silicon, not on multicrystalline silicon. An infinite orientation selectivity of the texturing, cleaning and etching chemicals may not be desirable as it results in very sharp edges of the texturized surface. Subsequent processes such as amorphous silicon deposition may be affected by this. Various schemes exist to 'round off' the sharp edges, for example by means of wet chemical polishing [3, 4] or by repetitive wet chemical oxidation/etch steps.

For multicrystalline silicon, an etch mixture of HF and HNO_3 usually in combination with acetic acid is used to etch the silicon isotropically and also creates a certain topography on the wafer (Fig. 2b). This process asks for precise control as it is a very vigorous exothermic reaction, and tends to form a porous Si layer on the surface, which is subsequently removed in a cold alkaline solution [3]. While the electro-optical performance of acidic etching may not match that of random pyramids, the process is widely used since it is applicable to multicrystalline silicon and the etch time of the process is significantly lower than alkaline etches. After the alkaline treatment process, a HCl cleaning step is applied to remove the metal impurities, particularly the alkali residues.

Various manufacturers provide equipment for wet processes [5]. Batch-type tools have typical batch sizes of at least 100 wafers. In-line tools are also available, especially for the isotropic etch process.

In order to avoid wasted effort in this scheme, a close coupling should be set up between the substrate supplier and the PV cell manufacturer. Clear specifications should be given as to how clean the wafers will be when delivered by the supplier to avoid unnecessary excessive cleaning at either side. It seems logical that SDR etch should be performed by the wafer supplier as it is a process that should be matched to the actual sawing process. As texturing is already cost-effectively done in combination with the SDR etch, one could consider transferring this step to the substrate supplier. Indeed, as the texturing techniques and methods seem to converge it may be subject to standardization and could be transferred to the wafer manufacturing location as it could result in further cost reduction. For decades, wafer suppliers have used and improved damage removal and (backside) wafer texturing with caustic processes as well as with acidic processes for the ULSI wafer market. Additionally, wafer suppliers have developed excellent track records in low-cost manufacturing and delivering high standards of consistency and quality control.

It should be noted that for future high efficiency cell concepts such as i-PERC [7] and back contact cells the wafer texture should be present on the front side only (Fig. 3). Therefore, single-sided texturing processes should be developed, which will most likely fit better with in-line processing rather than with batch processing. Needless to say, the relatively long process times required for the caustic texturing are challenging to implement in an in-line production line. This is clearly an area where faster chemical processes are highly desirable.

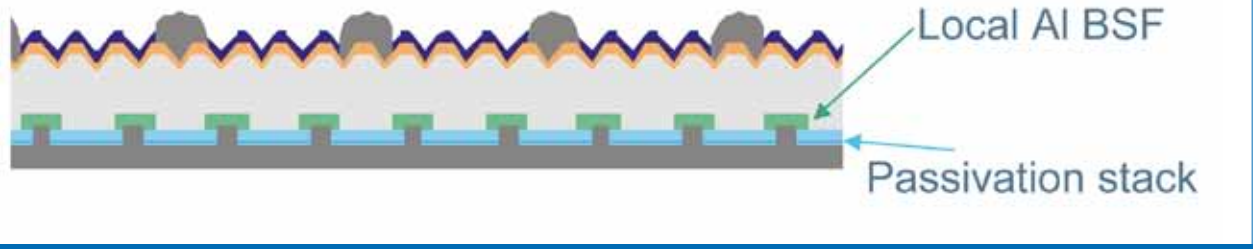

Figure 3. In the i-PERC process, an additional dielectric stack passivates the backside and therefore allows for higher cell efficiencies, especially for cells thinner than today's standard of 180µm.

Emitter

The process sequence continues with the formation of the emitter. For p-type substrates, the emitter formation itself is typically done by gaseous diffusion of $POCl_3$ in a furnace. For this process, not only is the wafer front-side doped (intentionally), but the wafer edges and back-side are also doped unintentionally, or in the case of back-to-back positioning, only partially. The $POCl_3$ diffusion also leaves a P-doped oxide glass that must also be etched. The PSG etch is often performed during a HF step. Both of these processes are offered in batch and in-line tools similar to those used in, and both processes can be combined in one tool.

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An alternative and possibly more cost-effective approach for emitter doping [8] is based on one-sided in-line deposition of H_3PO_4 liquid aerosol and subsequent drive-in in a furnace step. This approach avoids back-side parasitic doping and more importantly eliminates the need for a HF step to remove the PSG. In order for this process to be successful, good dosing and uniformity is required, which in turn requires good wetting of the substrate. An additional surface preparation step with oxidizing chemistry can be introduced. The metal decontamination HCl step could be efficiently combined with a surface preparation step such as in a $HClO_3$ process [2, 9].

Edge isolation

As any doping at the wafer back-side is eventually overcompensated by the aluminium back-surface field formation (at the end of the cell process sequence), the edge junction must still be removed as otherwise it would short-circuit the emitter to the back-side metal. The parasitic junction etch can be carried out in several ways, of which wet etching using an HF/HNO_3 mixture is one.

Passivation and antireflective coating

Subsequently, the surface is passivated and SiN is deposited to form an anti-reflective coating (ARC). Reduction of surface recombination is a key aspect for high efficiency solar cells, and therefore much effort is being put into the reduction of interface states. At the interface with the ARC, as mentioned earlier, texturing increases the surface area and consequently the number of surface defects. Passivation requirements will become even more stringent in view of the trend toward using less highly doped emitters in high efficiency solar cells. Surface recombination is also becoming increasingly important at the back-side of the cell as the industry moves towards thinner wafers. Cells like i-PERC (Fig. 3) use a dedicated dielectric stack at the backside to improve the surface passivation.

The trick is to treat atomic surface defects in such a way that they are not and will not become electrically active. Passivation by oxidation is ideally suitable for interfaces between silicon and dielectrics such as the AR coating. The growth of a clean, metal-free chemical oxide is a key process that is best achieved in an acidic regime as was described in the IMEC clean [9] and other processes. Extensive knowledge in this area is available in the CMOS community, where interfacial oxides have been studied to optimize the deposition of high-k gate dielectric materials. Recently, an improved UV response for a standard solar cell process (such as that in Fig. 1) was obtained using a HNO_3 process on n-type substrates. This improvement was attributed to the removal of excess P at the emitter surface [10]. The trend to higher cell efficiencies and thinner wafers renders improved surface passivation schemes imperative. Apart from the i-PERC passivation, very low recombination rates have been reported using ALD of Al_2O_3. Acidic surface oxidation may be applicable to PV for p-type silicon in this case. In practice, the remaining defects at the interface of oxide and Si are further passivated by hydrogen released from the SiN ARC during the firing of the metallization.

Another innovation in very high efficiency solar cell development is based on a-Si:H/c-Si heterojunctions. Passivation of defects is realized by adding a thin layer of undoped hydrogenated amorphous silicon, as is used in the heterojunction solar cells of Sanyo [11]. However, even the deposition of such i:a-Si layers requires careful surface cleaning and pre-treatment. It is well known that, in class 1 cleanroom environments, adsorption of hydrocarbons occurs within 30min after the clean [12]. This may significantly affect the deposition of subsequent layers such as amorphous silicon [13]. Therefore, after passivation the storage time and storage ambient need to be carefully controlled, possibly adding to the cost and complexity of the process.

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Metallization

A new and promising wet process in this respect is Cu electroplating, a mature and low-cost production process used for printed circuit boards, which is seen as a viable alternative for the expensive screen-printing pastes. Pastes already constitute a major part of the consumable cost in solar cell manufacturing, and the price of the Ag material used for the front-side metal grid is expected to rise as continued PV growth might exhaust the available Ag raw material. Cu metallization for the emitter contact also has a cell performance advantage when combined with shallow emitter profiles

and can lead to significant efficiency increases due to increased blue response. The main differentiator between the various processes under scrutiny is in the choice and technology for seed and barrier layers for which Ni electroless plating is one option. Some schemes allow higher aspect ratios to be reached than are possible with regular screen-printed electrodes, which leads to additional cell performance increases. Cu plating equipment for PV is being offered of late by several companies [14].

General opportunities for cost reduction and manufacturing issues

Chemical consumption: understanding the chemical processes will allow the limits to be pushed

It is felt that chemical usage, including DI water, can still be pushed down by more extensive research. The use of recycling schemes in combination with low full-lifecycle cost of ownership chemicals such as O_3-based solutions (e.g. O_3- water, or O_3– H_2SO_4) should be considered.

When using mixtures, the assay accuracy window needs to be assessed with respect to the desired processes. This has an important impact on the cost of the chemical as well as on the mixing hardware, and will eventually affect concentration monitoring and spiking. The selection of chemical mixtures and lifetime determination should also take into account potential instabilities in mixtures through chemical reactions amongst the different components as well as drift in assay through evaporation.

Today there is very little quantitative information available on the actual purity level requirements of the chemicals, with respect to metallic contaminants. Chemical mixtures are in most cases chosen based on lab or pilot line tests. Mixtures are configured based on merits in their fresh state, without significant loading, and often with little attention to the actual purity level. With particular reference to cleaning applications, the relation between the bulk concentration of contaminants in the liquid mixture versus the resulting surface concentration of contaminants deposited on the wafer surface need to be investigated [15]. This relationship should be used to set up purity specifications for starting chemicals as well as for determining bath lifetime limitations based on contamination loading. These relations can also be used to extend the lifetime of chemical mixtures based on quantitative models. Chemical processes that are less demanding on purity requirements should be favoured with respect to more 'sensitive' processes. As an example, it was demonstrated for ULSI manufacturing that trace metal specifications of DI-water used for rinsing before critical hot processes could be relaxed by acidification [16]. For etching applications (such as SDR and texturing), the loading of the mixtures with reaction products and any impact on the process need to be assessed and modelled.

Once optimal chemistries are identified, strategies should be set up to stretch the lifetime even further by bath monitoring and appropriate respiking. All of the above need to be studied in the frame of cascaded use of chemicals. This mode of operation is common in many hardware platforms, but much more systematic studies need to be made to optimize this approach. For example, the last cascade stage(s) should not contribute anything to the overall process.

Not only would these measures lower the processing cost but they would also lead to a reduction of process fluctuations that affect the cell performance, ultimately resulting in smaller variations in overall cell efficiency.

Equipment – batch versus in-line

Several aspects of wet processing hardware can play important roles such as minimizing pick and place actions, which can reduce cost. Exemplary measures which the PV industry has implemented to bring down cost of ownership are the 'merging' of processes and increasing the areal throughput of equipment to the range of 3000 wafers/hour [6].

Conceptually, in-line processing should be preferable (with respect to batch processing) as it creates a streamlined production line. In-line processing also offers better 'selective' access to one side or the edges only. In view of the high throughput, measures have to be put in place to swiftly overcome wafer breakage events without noticeable down time.

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Throughput matching of typically slower processes such as alkaline texturing are still major challenges for in-line implementations. The need for studies on required purity of the chemicals naturally extends to requirements for the materials. This in turn impacts the hardware cost. Installation of in-situ generation of chemicals (such as O_3-based chemicals) or in-situ purification should be considered with the goal of extending the lifetime of chemicals and enhancing quality while reducing waste and cost.

Impact of thinner wafers

Apart from reducing operational costs, another challenge is the expected reduction of Si wafer thickness. With silicon constituting 30% or more of the module cost, the trend to thinner wafers is foreseen to continue the next decade. For wafer thicknesses from 150 to 180µm, commercial wet process equipment is already showing high yields (0.1 % or lower breakage rate), but yield on thinner substrates has yet to be widely established. This problem will be even more pronounced once substrates become thinner than 100µm. Nevertheless, this should not be a showstopper as the wafers will most likely be supported by some sort of carrier throughout the process cycle, and the wet processes will need to be compatible with such an approach. For this reason, in-line processes in which the substrate is mounted on moving holders or chucks would seem to be most suited.

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Paul W. Mertens holds an M.Sc. and a Ph.D. degree in applied sciences from KULeuven. He joined IMEC in 1984 to work on Silicon-On-Insulator substrates and also worked on Si wafer quality, gate dielectrics, defect control, effects of contamination and cleaning processes. Currently leading the Ultra Clean Processing expertise centre at IMEC, Mertens is an organizer of the Ultra Clean Processing on Semiconductor Surfaces symposium (UCPSS).

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