Challenges in producing photovoltaic modules on thin wafers

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ABSTRACT

The principal paths to cost reduction for the photovoltaics industry are increasing the efficiency of solar cells and the power density of modules, together with the reduction of the specific consumption of silicon. Following the slowdown in the ever-increasing growth of the PV market earlier this year, and the reduction in the market cost of polysilicon, wafer producers and most cell producers moved back to the 180μm generation substrates. It may take some time for manufacturers to tackle the technological issues that need to be addressed in order to successfully decrease wafer thickness further. In this article, some of the issues related to the production of thinner and thinner cells are outlined and discussed.

Cell and module efficiency directly impact the overall €/Wp cost of a PV module and have historically been a major focus for technological development. Commercial module efficiency values (defining efficiency on the basis of the total outer dimensions) are in the range of 12-14% for screen-printed cells and 15-17.5% for the best-performing cells. Device designs capable of achieving module efficiencies of over 18% for multicrystalline silicon, and over 20% for monocrystalline silicon, are expected at a production scale in the short to medium term. Calculated efficiency limits as a function of substrate thickness indicate an optimum in the 40-100μm range on both n- and p-type wafers for resistivities >1Ωcm [1,2].

Purified silicon (polysilicon) is the basic ingredient of crystalline silicon modules and also forms an important part of the overall module cost. For the past few years, the availability of polysilicon feedstock has been a critical issue for the rapidly growing PV industry. The tight supply has caused very high polysilicon spot market prices and has limited production expansion for part of the industry. On the other hand, it has triggered rapid innovation in wafer production and cell manufacturing with a reduction of cell thickness of 45-52% from 330μm down to 160μm over a period of five years, despite increasing handling and processing problems. During the same timeframe, the typical wafer area grew by 140%. As a result, the silicon consumption per Wp of module power produced is significantly reduced. Silicon usage is currently 8-9g/Wp; a figure that was typically 13g/Wp just a few years ago. Given a feedstock cost in the range of 30-50 €/kg, this corresponds to 24-50€c/Wp – roughly half the often-cited target cost of ~1€/Wp.

As some lead cell manufacturers moved down in thickness to 160μm x 156mm x 156mm, the reduced amount of silicon used was offset by the losses in yield – both during the cell as well as the module manufacturing. Wafer producers and most cell producers moved back to the 180μm generation substrates in response to this.

Processing large-area thin cells

Achieving thinner wafers

The ratio of the amount of high quality silicon required to make a module versus its nominal power (g/Wp) is the direct related economical parameter affected by processing thinner wafers. While using advanced, highly automated wire-saw-related processing techniques should allow production of very thin wafers with high yield, it is near impossible to limit the total amount of silicon consumption to values below 100μm.

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The additional silicon loss linked to the kerf made by the wire and slurry can be avoided if the wafers are casted to thickness as is done in ribbon technologies such as Edge-defined Film Growth (EFG, Wacker-Schott); Crystallisation on Dipped Susbstrate (CDS, Sharp); String Ribbon (SR, Evergreen); Ribbon Growth on Substrate (RGS, ECN); or Ribbon on Sacrificial Template (RST, Solarforce). Such wafers are multicrystalline but can be of good quality as demonstrated by the high efficiencies reached on large areas using industrial processes by, for example, Sharp (14.8% on CDS [3]) and IMEC (16.0% on EFG [4]).

Furthermore, these technologies have a very high throughput potential, although this is mostly leveraged by losses in material quality. While in R&D environments very thin wafers (80-120μm) have been produced, the minimum thickness in the established industrial ribbon technologies is not less than 150μm.

Layer-transfer approaches form an alternate class of technologies to achieve very thin wafers. The cost of ownership of processes based on growing a thick epitaxial layer of silicon on top of a 'weakened' intermediate layer followed by detaching such as the PSI-process [5] or creating voids [6] is threatened by the additional cost linked to preparing the weak layer and the epitaxy process. Alternatives such as the PolyMax technology developed by Silicon Genesis, or the Stress-induced LIft-off Method (SLIM-Cut) developed at IMEC [7] (see Figure 1) aim at repeatedly releasing a very thin layer of silicon from a carrier with minimal losses. This is performed either by creating a sub-surface weak layer by implantation or by inducing stresses beyond the shear stress of silicon, exploiting the difference in thermal expansion between the carrier wafer and a deposited stress-inducing layer.

The most decisive advantage of the latter technique is that the crack depth (and therefore the final thickness of the silicon film) is governed by the mechanical properties of the materials used and does not rely on pre-processing of a weak layer. Another advantage of this method is that it was developed using only industrial tools (screen-printers, belt furnaces). The potential for low cost is therefore present from the beginning of the development. In addition, the first results obtained (10cm^2 free-standing films; cell efficiency of 10% obtained on a 1cm^2 cell) are extremely promising given that no tool was designed to tackle the specific issues related to the method. An advantage inherent to the layer transfer approaches is that the thin silicon films can be monocrystalline as well as multicrystalline, allowing for higher efficiencies on higher quality samples.

Figure 1. 'Stress-induced lift-off method' (SLIM-Cut) process. A high thermal stress is induced by a metallization layer, resulting in the release of a 50µm Si foil. The top row shows the remaining substrate and the bottom row, the thin lifted-off silicon layer.

Reaching high efficiencies

The thinner the substrates are manufactured, the higher the relevance of the recombination at the rear surface and optical enhancement on the performance of the solar cell. Whereas the bending of thin substrates under the influence of a traditional full aluminium back surface field (BSF) could be remedied by a dedicated cooling treatment after firing, the limited electrical surface passivation offered by such alloyed BSF will require giving up this established technology and a move to a dielectric passivated and locally-contacted rear surface, as was introduced in the Passivated Emitter and Rear Cell (PERC) structure. Usually, such dielectric passivation of the rear of the cell can be offered through deposition of commonly used dielectrics in photovoltaics such as SiN_x or SiO_x, or combinations of these.

Alternatively, technologies new to the photovoltaic industry such as Atomic Layer Deposition (ALD) of negatively charged dielectrics (e.g. AlO_x) are being explored. The local contacting can be done either by first locally opening the dielectric, depositing the base contact (typically aluminium) on the rear and firing (iPERC, IMEC [4]), or by depositing the base contact on the dielectric and locally firing it through by means of laser (Laser-Fired Contacts, LFC, FhG-ISE, [8]).

Using the iPERC technology, large-area cell efficiencies of 17.6% were demonstrated on 130µm-thin monocrystalline substrates and 16.8% on 120µm-thin multicrystalline. An additional benefit of such dielectric passivation is the excellent mirror extending over the vast majority of the rear surface increasing the light-trapping properties within the solar cells.

As the iPERC and LFC processes are finding their way to the market, R&D efforts are shifting to the next generation in order to further push up the efficiencies. The structural difference between a PERC cell with self-aligned but high recombinative rear contacts and a Local Back Surface Field (LBSF) or Passivated Emitter and Rear Locally diffused (PERL) cell is marginal. However, achieving the reduced recombination at the rear contacts due to a diffused high-low junction beneath the contacts requires significant process changes. With such PERL structures, the 20% barrier for thin large-area industrial cells will be overcome.

Although major efforts are ongoing in reducing the metallization coverage for double-side-contacted cells, part of the surface will be covered by fingers while ~2% of the surface will be covered by the cupper ribbon that provides the series interconnection with the neighbouring cell. Part of this loss can be avoided by having the solder pads to the contact grids of both polarities available at the rear surface [9]. This potential for performance increase has triggered the early developments of back-contacted cells. On the other hand, the drawback of the technology is that an adapted module manufacturing is required. To date, the most successful market penetration of back-contact cell technologies is by companies that sell the integrated product (cell & module).

In such very thin double-side- as well as single-side-contacted cells, the other challenge is to maintain strong absorption of IR photons. This requires ever-better light-trapping schemes. The prevailing approaches based on front-side texturing in combination with some sort of highly reflective back surface may be extended to reach efficiencies over 20%, but eventually more complex concepts such as multilayer interferometric reflectors, or the embedding of metal particles to introduce plasmonic effects, may be necessary.

Maintaining process yield

Added to this problem of fragility, thin wafers also become increasingly flexible. As a result, the combination of thin, large-area and square wafers is posing processing problems in terms of handling, batch-type wet chemical processing, and processing at elevated temperatures. The thin wafers are delicate and notoriously difficult to handle without inducing damage in the form of chipping and cracking. Handling issues begin when the wafers need to be separated at the entrance of the production line. Once wafers start moving through the production process, the emphasis is on transporting them smoothly with no jarring or shaking.

The high production volumes in photovoltaic manufacturing demand gripping methods for wafers that can keep hold of wafers through the high rates of acceleration and deceleration. In batch-type wet chemical processing, the wafers stick to each other in the cassette and can rarely be released without yield losses. As such, the use of in-line wet processing tools or switching to dry processing is recommended.

These methods provide further benefits via their property of addressing only a single surface of the cell, thus allowing easier decoupling of surface treatments between the front and rear surface. In processes where wafers are (even moderately) heated, such as diffusion, Chemical Vapour Deposition (CVD) processes or Physical Vapour Deposition (PVD), the wafers curl from the corners up under the influence of the thermal gradients induced by shape. As a result, an increased level of automation will be required.

This increased automation will also be required in R&D environments where

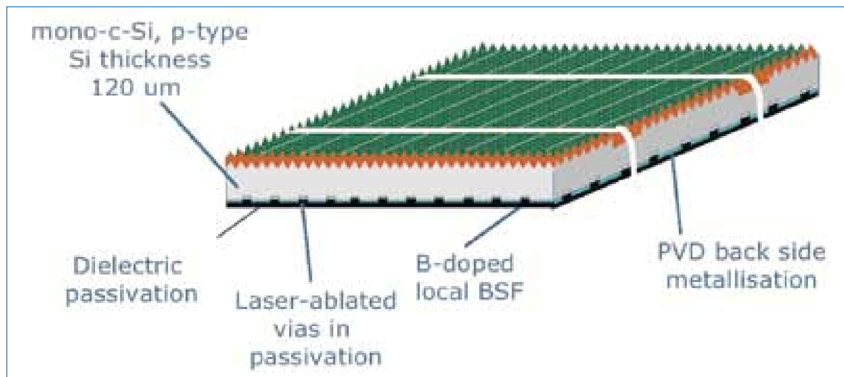

Figure 2. PERL cell with back-side passivation improved by a B-doped Back Surface Field.

handling has often been performed manually. This will significantly increase the cost of R&D operations. Additionally, the importance of in-line processing, supporting the wafers over one of the surfaces and incorporating soft clamping mechanisms near the edges is expected to grow.

Module manufacturing

Pursuant to cell production in the value chain is the manufacturing of the laminate or module, which will be sold under a 20-25 year warranty liability that tends to freeze any developments. The enthusiasm on the part of module manufacturers to change to the proven technology of interconnecting the cells by soldering and handling of full strings or even cell meshes in building up the laminate is low and major changes are not expected as long as they are not needed.

The acceptance of future thin cell offerings by module producers will need to go hand-in-hand with significant cost savings to offset the increased risk in introducing new technologies. These cells are expected to be very thin and fragile, highly efficient and capable of delivering high currents, dictating the use of higher cross-sections of the applied interconnectors. The cell thickness will eventually be less than the thickness of the cupper ribbons soldered to the front and the rear of the device, which will induce tremendous stresses in the interconnected cells.

As for cell processing, high levels of automation with minimal impact on the wafers will be required. Additionally, reducing the effective overall soldering temperature by using advanced soldering methods such as local laser soldering, low temperature solders, or eventually using conductive adhesives will become more common. Another alternative to soldering front to rear is the use of back-contacted cells where, through well-considered co-development of cell and module technologies, much wider and thus thinner interconnects could be used, helping in reducing the mechanical stress induced by the interconnection process.

Conclusions

The speedy reduction of wafer and cell thickness has currently been slowed down by a combination of reduced need as the silicon feedstock became cheaper as a result of increasing processing issues. The need to further significantly reduce the cost of photovoltaic modules in order to achieve grid parity, combined with the potential for higher efficiencies in thinner cells, will eventually lead to further reduction of the cell thickness.

The present calm on the market offers wafer, cell and module producers the time to address the upcoming technical challenges in producing thin wafers and achieving high cell efficiencies on these wafers while maintaining production yield in processing both the cells and the modules, which will give them a strategic lead to tackle the pressure on price. In order to exploit the full potential of the introduction of thin and eventually back-contacted cells, integrated companies or strategic partnerships (cell & module) where concerns from both parties can openly be discussed will have a definitive advantage.

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