State-of-the-art c-Si cell manufacturing: Trends in materials, processes and products identified in the 5th edition of the ITRPV roadmap

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ABSTRACT

The crystalline silicon (c-Si) module price has been fluctuating slightly around the US$0.72/Wp level for the last 18 months. This pricing, at an estimated cumulative PV module shipment volume of 149GWp, indicates a trend change for the PV industry. C-Si module pricing appears to be currently above the production cost and should therefore yield a profit margin. However, there is still a mismatch between manufacturing capacity and future market demand. A closer look at the pricing figures reveals that there is no indication to give the all-clear during the ongoing consolidation process in the PV industry. C-Si module pricing is not reflecting the increase in polysilicon and wafer prices, and therefore the pressure to reduce the cell and module conversion costs remains a looming fact. This paper describes state-of-the-art c-Si cell manufacturing solutions that are in line with identified trends in materials, processes and products recently published in the 5th edition of the International Technology Roadmap for Photovoltaic (ITRPV). Currently available c-Si cell technologies offering higher efficiencies as well as materials savings will be discussed. The need for implementing these technologies in mass production without significantly increasing the cost per piece and in the face of more-complex manufacturing processes will be established. The findings of the ITRPV regarding the reduction in levelized cost of electricity (LCOE) will be discussed, leading to the conclusion that contemporary cell technology supports the long-term competitiveness of PV-based power generation.

Introduction

The evolution of the sales price of PV modules has been exhibiting a continuous learning curve on the part of the PV industry for nearly 60 years [1]. Fig. 1 shows the price learning curve of PV modules for the last 37 years, from 1976 to 2013 [2]. The log–log plot displays the average module selling price in 2011 US$ as a function of cumulative module shipments. Apart from some kinks around 100MWp, the curve appears to be almost linear up to a shipment value of around 3.1GWp, which represents the cumulated shipments at the end of 2003. The linear fit shown in Fig. 1 reveals a learning rate (LR) of 21.5%, indicating that there is an average module-price reduction of 21.5% for every doubling of the cumulative module shipment.

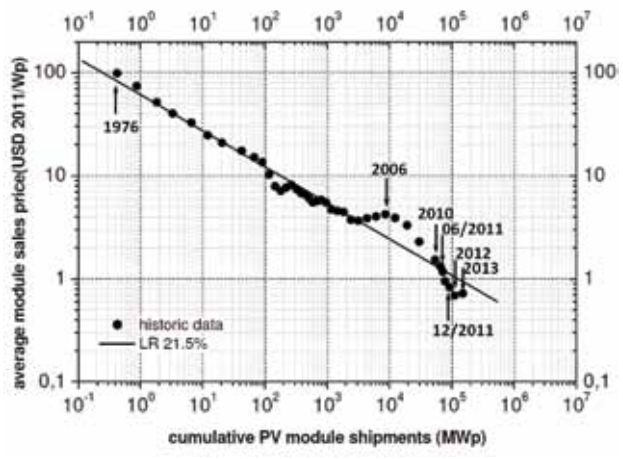

Figure 1. Historic price learning curve for PV modules from 1976 to 2013, indicating the average sales price in 2011 US$/Wp and the corresponding cumulated PV module shipments [1].

> "The evolution of the sales price of PV modules has been exhibiting a continuous learning curve on the part of the PV industry for nearly 60 years."

The deviations from this linear trend after 2003 were caused by strong market fluctuations. Following price increases until 2006 (8.5GWp), prices dropped again as the shipped volume increased significantly. The $1/Wp threshold was crossed in 2011 at a cumulative shipment of 77GWp, with a price of $0.95/Wp. The oversupply situation in 2011 and 2012 caused the big price drop to $0.69/Wp, which was well below the learning rate of 21.5%, and the 100GWp landmark was passed at the end of 2012, with a cumulative shipment of 110GWp. The recording of the data points of the average module price and worldwide shipment volume of PV modules at the end of 2013 ($0.72/Wp/149GWp) [2,3] in Fig. 1 indicates a small trend change in the historic price learning curve, with a big influence on the global situation of the PV industry.

Price and cost considerations

An examination of the price development of c-Si PV modules between 2010 and April 2014 indicates that the module price dropped steadily from 2010 until the end of 2012, with only minor changes occurring throughout 2013. A detailed price trend is plotted in Fig. 2, showing the pricing of polysilicon (poly-Si), multicrystalline silicon (mc-Si) wafers, c-Si cells and modules.

The inset in Fig. 2 outlines the shift in the percentage share of the different value chain elements for c-Si modules. While in 2010, at a module price of $1.87/Wp, cell and module conversion accounted for about 25% and 33%, respectively, of the module price, these shares changed to 22% and ~50%, respectively, in January 2013, at a price of $0.69/Wp. Since then the module price has been fluctuating around $0.70/Wp, feigning a price stabilization, but the percentage price portion, especially for module conversion, has fallen by over 10%. Module and cell suppliers have to lower their prices while poly-Si and mc-Si wafer prices are increasing. This change, and the assumption that the global PV module production capacity of 63GWp or more in 2014 will still exceed the expected market demand of about 44GWp [5], clearly shows the market pressure on module and cell manufacturers. Finding and implementing measures for driving cost reductions in consumables and materials as main non-silicon cost elements [6] therefore remain major tasks for c-Si cell and module manufacturers in order for them to be successful in the continued PV industry consolidation phase.

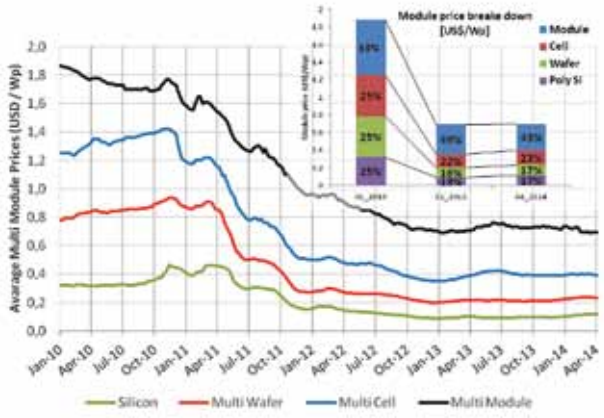

Figure 2. Price trends for poly-Si, mc-Si wafers, mc-Si cells and modules [4]. A percentage breakdown of the specified elements is shown in the inset top right. Assumptions: 44.1 wafers/kg with ~22.7g/wafer; average mc-Si cell efficiency ~17.3% (4.2Wp).

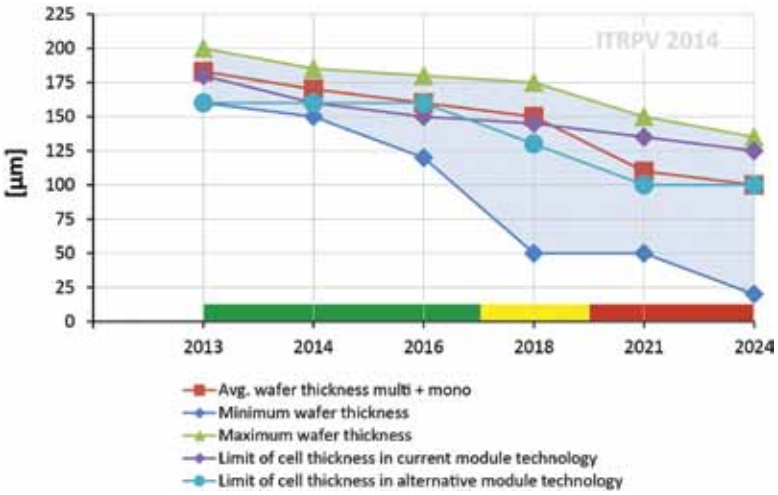

Figure 3. Predicted trends for the minimum, maximum and average as-cut wafer thicknesses in the mass production of c-Si cells and modules. (Colour coding: green = technology is available and manufacturable; yellow = technology is available but not yet in mass production; red = industrial solution not known.)

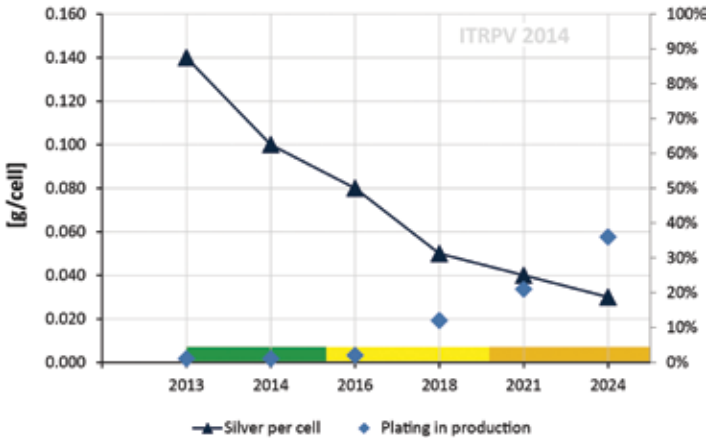

Figure 4. Trend of the reduction in silver usage per cell (156mm x 156mm) and predicted share of plating technology in production. (Colour coding: green = technology is available and manufacturable; yellow = technology is available but not yet in mass production; orange = interim solution is known but not yet suitable for mass production.)

ITRPV findings in cell manufacturing

The International Technology Roadmap for Photovoltaic (ITRPV) [7] discusses topics in three areas: materials, processes and products. Analogous to this, topics related to cell manufacturing, as well as the corresponding responses of the PV industry, will be discussed in the following sections.

Cell materials

Mc-Si wafers account for about 60% and 30% of the mc-Si cell price and c-Si module price respectively, as indicated in Fig. 2. Reducing the c-Si wafer price may be achieved by cost reductions in crystallization and wafer sawing and by a more efficient use of poly-Si, namely by a reduction in wafer thickness. Fig. 3 summarizes the expected thickness reduction trend for the conventional 156mm x 156mm wafer dimensions.

Current minimum as-cut wafer thickness in 2014 is expected to be between 150 and 180µm. This reduction is in line with cell and module trends, and thicknesses are expected to attain 100µm in 2024. High-efficiency cell concepts and modules have to deal with this reduction in wafer thickness, in addition to the improvements in wafer-sawing technology, wafer handling and module interconnection.

C-Si cell concepts for thin wafers are currently available: different passivated emitter and rear cell (PERC) approaches for p- and n- type wafers [8], or heterojunction with intrinsic thin layer (HIT) for n-type wafers in particular [9].

Metallization pastes containing silver (Ag) and aluminium (Al) are the most costly non-Si materials in c-Si cell processing. A total amount of 140mg of Ag per 156mm x 156mm c-Si solar cell was used in 2013 for the front-side grid and for the rear-side soldering interface, as shown in Fig. 4. The Ag price of $690/kg alone as part of the paste price results in a cost of around ¢2.3/Wp, accounting for around 14% of the current price for the cell conversion of c-Si back-surface field (BSF) cells. As regards processing cost, Ag accounts for approximately 50% of the metallization process cost, as reported by Schuler & Luck [10]. With the assumptions used in Fig. 2, the quantity of Ag needed for 1GWp of c-Si cells is calculated to be 33t/GWp. The reduction of Ag per cell to 100mg in 2014 results in an impressive fall in demand to 24t/GWp. Further reductions in Ag usage per cell are therefore essential, especially with respect to the significant price fluctuations in recent years.

The future trend of Ag reduction for the next ten years is shown in Fig. 4. These projected values are ahead of the predictions of the ITRPV 4th edition [11], demonstrating the progress in screen printing. Ag is still a perfect conductor but expensive. A cost-efficient alternative may be the use of copper (Cu) with the implementation of plating technologies. The introduction of such technologies into mass production, however, is not expected to take place before 2018.

Cell manufacturers put a lot of effort into reducing cost and realizing Ag savings, while ensuring acceptable cell quality and increasing the efficiency. Some approaches – such as sophisticated front-side busbar layouts, optimized finger grids and interrupted busbar structures at the cell rear side – are illustrated in Fig. 5 and compared with designs from 2010.

Cell manufacturing processes

The conventional Al-BSF cell manufacturing process comprises 1) the front-end (FE) processing, including two wet chemical processes (texturing, chemical edge isolation) and two thermal processes (phosphorus diffusion, silicon nitride (SiN) anti-reflective coating (ARC)); and 2) the back-end (BE) processing, consisting of metallization and testing/sorting. These processing steps have been the status quo in production for several years. Regular productivity optimization of the installed production equipment is essential in order to stay cost competitive.

The construction of cell fabs with

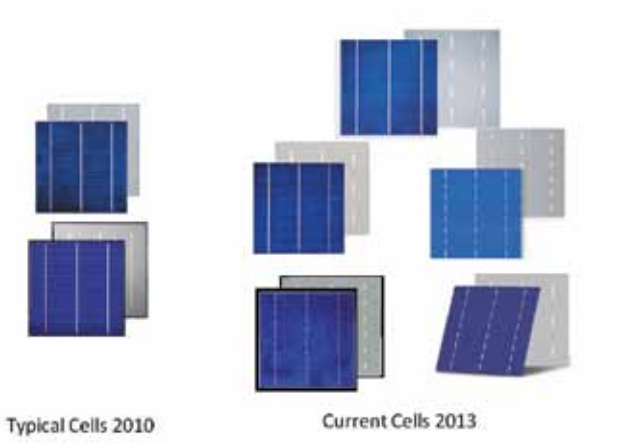

Figure 5. Comparison of c-Si cell layouts in 2010 and 2013, taken from the cell data sheets of Gintech, Hanwha Q CELLS, Hareon, JA Solar and Motech.

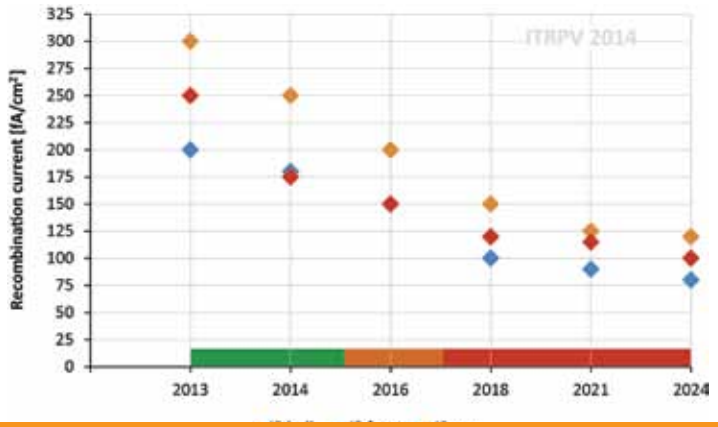

Figure 6. Trends of the recombination currents J_{0bulk}, J_{0front} and J_{0rear} in p-type cells.

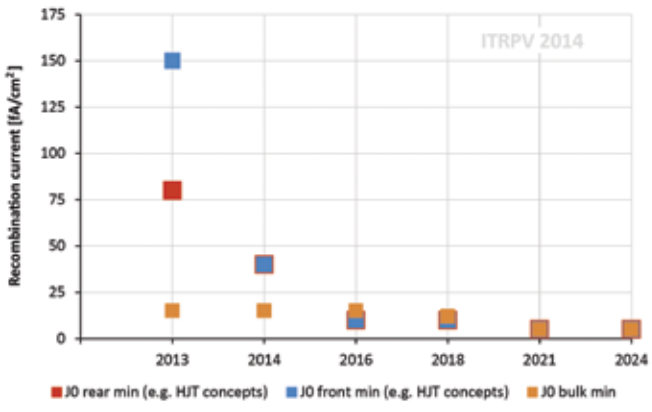

Figure 7. Trends (R&D perspective) of the recombination currents J_{0bulk}, J_{0front} and J_{0rear} for high-efficiency n-type cell concepts.

new 'high-throughput' equipment is not yet in line with today's investment cycle. The current challenge for cell manufacturers is to increase tool throughput, tool uptime and process yield, in parallel with increasing the cell efficiency of existing cell products and introducing new high-efficiency cell concepts. The ITRPV 5th edition [7] emphasizes the importance of reducing the throughput mismatch between the FE and the BE. The roadmap suggests a throughput of 7200 wafers/hour for FE and BE as the target to be met by 2024 with new, innovative equipment. Today, smart upgrades of existing cell lines are more important than replacing full lines by new equipment. Those upgrades eliminate existing bottlenecks with single high-throughput tools, selected automation solutions and improvements of the installed tool base regarding manufacturing availability and throughput. Now is also a good time to implement and test new tool concepts in order to be prepared for the next investment cycle.

> "Today, smart upgrades of existing cell lines are more important than replacing full lines by new equipment."

Cell process technology

Cell efficiency improvements are directly linked to reductions of the recombination current in the cell bulk (J_{0bulk}), at the cell front side (J_{0front}) and at the cell rear side (J_{0rear}). Fig. 6 shows the trend of the recombination losses for p-type cells. The trend from the R&D perspective for high-efficiency n-type cell concepts is shown in Fig. 7.

The reduction of J_{0bulk} is imperative, since stagnation here would hamper any improvement at the front or rear side of the cell. Mono-Si material provides low J_{0bulk} for p-type cells, and for the cheaper, casted p-type material there are industry solutions: high-performance (HP) mc-Si and mono-like Si material. While HP mc-Si material is available from several wafer manufacturers, the euphoric expectations for mono-like c-Si material as a low-cost alternative to p-type mono c-Si did not materialize and it has not become established in the market. N-type mono material, however, enables the lowest J_{0bulk} as demanded in Fig. 7, and it is mandatory for high-efficiency cell concepts, such as HIT or n-type PERC.

An inspection of the ITRPV assumptions about the market share of casted- and mono-Si materials confirms that no clear statement is possible about a long-term winner. As shown in Fig. 8, it is expected that the mono market share will increase slightly, from currently 40% to 50% by 2024, mainly driven by an increased demand for n-type mono material for more-complex high-efficiency cells. Casted material will remain strong in the market thanks to the shift from mc-Si to HP mc-Si material. Mono-like c-Si material is expected to remain a niche application.

Reducing the J_{0rear} to 100fA/cm^2 and below is a requirement for the cell rear side and a limitation for BSF cells. PERC cell concepts use dielectric passivation layers, enabling J_{0rear} values of ~60fA/cm^2. Solutions for the deposition of SiO_2, SiN_x or Al_2O_3 are available on the market and may be combined with a rear-side aluminium metallization as an IR light reflector, deposited by either screen printing or physical vapour deposition (PVD) methods. Lasers are available for contacting the rear-side metallization with the bulk, either before or after the metal deposition.

Fig. 9 shows the internal quantum efficiency (IQE) behaviour of the Hanwha Q CELLS Q.ANTUM cell, a typical PERC concept with rear-side passivation and laser-fired point contacts applying mc-Si material. The efficiency benefits are realized by the higher usage of infrared light, as illustrated in Fig. 9.

Reducing the J_{0front} to values below 100fA/cm^2 is a requirement, as indicated in Fig. 6. One condition that leads to a reduction in front-surface recombination losses is an increased emitter sheet resistance. The ITRPV trend for the sheet resistance of n-type doped emitters is shown in Fig. 10; with sheet resistances above 100Ω/sq., the trend moves towards more lightly doped emitters. Selective emitter (SE) or homogeneously doped (HD) emitter techniques have been commercially available for some years, as well as solutions with and without additional processing steps to contact these lightly doped regions. SE techniques are available with etch-back or laser-doping processes, with ion implantation or with silicon inks. Solutions for HD emitters are available with techniques that combine fine-line metallization with Ag plating as well as with screen printing techniques using advanced Ag-pastes.

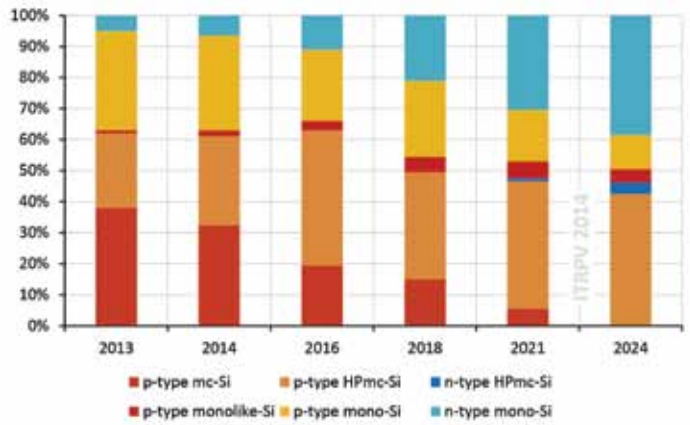

Figure 8. Expected relative market shares for casted and mono-Si materials.

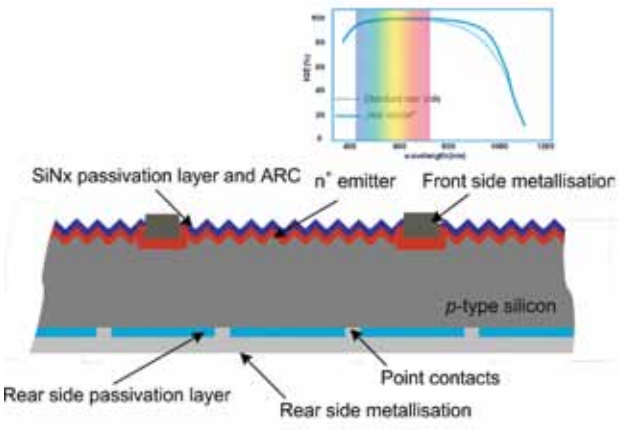

Figure 9. Schematic cross section of Hanwha Q CELLS Q.ANTUM Cell concept with passivated front and rear and laser-fired point contacts (LFC). This cell concept yields efficiencies of up to 19% on mc-Si material [12].

"A trade-off has to be made between following the roadmap for Ag reduction, good contact properties and high conductivity."

Fig. 11 shows the ITRPV requirements for finger widths and alignment precision. Finger widths of around 65µm are currently in production: this value is significantly lower than that predicted in the 4th edition of the ITRPV [11]. Reducing the finger width increases efficiency; however, a trade-off has to be made between following the roadmap for Ag reduction, good contact properties and high conductivity. There are various technologies for high-quality printing available on the market:

- Single print – the current mainstream technology.
- Double print – a technique requiring an additional printing step and precise alignment, because the fingers are printed twice.
- Dual print – also requires an additional printing step, but the printing of the fingers is separate from the printing of the busbars, enabling the use of busbar pastes with a smaller quantity of silver.

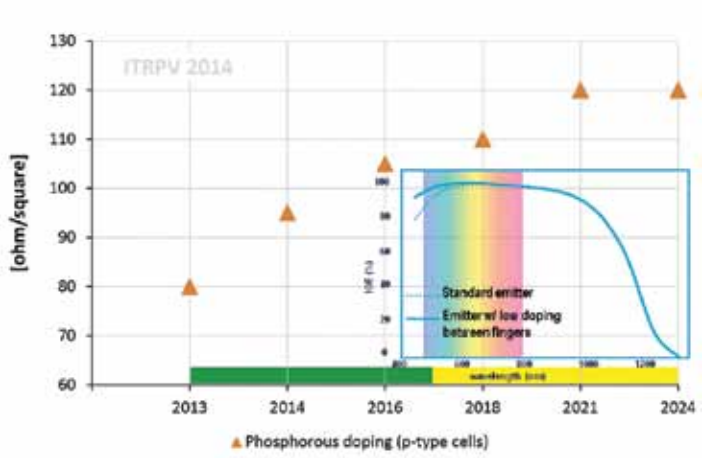

Figure 10. Expected trend for the emitter sheet resistance of n-type emitters. The inset shows the benefit in internal quantum efficiency (IQE) for cells using these improved emitters.

Figure 11. Predicted trend for finger width and alignment precision in screen printing. The inset shows the expected shares of different screen-printing technologies in production over the next years.

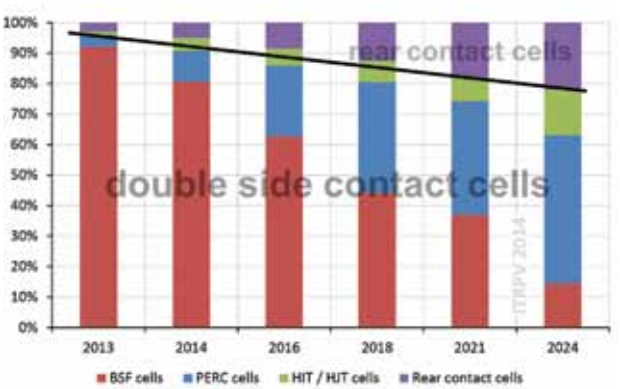

Figure 12. World market shares of different cell concepts, predicted by the ITRPV [7].

The inset in Fig. 11 shows the expected share of these printing technologies. Single print is therefore expected to stay mainstream until 2016, with the other two methods gaining market share; no clear winner during the period to 2024, however, has so far been identified. Improvements to the screens will be necessary; current screens enable finger widths down to 50µm, with acceptable screen lifetimes. Further reductions to 30µm, in line with the ITRPV roadmap, will require either more precise and robust approaches for screens or new approaches (such as stencils, which are well established in the semiconductor industry). Revolutionary new techniques for mass production are not much in evidence so far. Nevertheless, cell manufacturers have the choice of implementing the most cost-efficient solutions for their production environments.

Products

The technology trends discussed above address two requirements for c-Si solar cell products: cost reduction per cell and increase in cell efficiency. As an addendum to the materials trend of Fig. 8, Fig. 12 shows the expected market share trend to 2024 of currently available cell concepts. The clear message is that double-side-contact cell concepts will remain mainstream during the next few years. The market share of BSF cells will shrink in favour of PERC concepts for both p- and n-type materials. HIT concepts are expected to gain more share, surpassing 10% by 2024. The market share of rear-contact cells is estimated to be around 20% by 2024 – a greater reduction with respect to the assumptions of the 4th edition of the ITRPV [11].

The average efficiency of c-Si solar cells is expected to steadily increase, as illustrated in Fig. 13. Fig. 14 shows the trend of the corresponding 60-cell modules, assuming a wafer format of

156mm x 156mm (in the case of high-efficiency rear-contact cells, the values are estimated, as these cells are not yet available in this format). N-type cells will yield the highest efficiencies and respective module power classes, with an efficiency advantage of up to 4.5% over p-type cells. Despite the above-discussed progress in casted crystallization – especially the wide availability of HP mc-Si material – it is evident that the argument of the gap between mc-Si and mono-Si materials still remains valid. Acidic texturing is assumed for mc-Si and HP mc-Si cells, and alkaline texturing for mono materials. Fig. 14 clarifies the expectation that HP mc-Si cells will enable 60-cell modules to produce 300Wp.

Conclusion

A prediction of the future cost development for modules and of the LCOE can be made by considering all the available technology improvements and trends discussed above. Cell efficiency improvements, in combination with average unit cost reductions through improved manufacturing productivity and optimized materials consumption, will result in continued reductions in cost/Wp of c-Si modules.

Table 1 summarizes the predicted cost evolution if the average percentage increases in module power (deduced from Fig. 14) and the continual manufacturing cost reductions are combined. The June 2012 price value of $0.83/Wp represents the average cost from non-Chinese module manufacturers, i.e. the price was at cost level at that time [13]. The module manufacturing cost at the end of 2012 is assumed to be $0.73/Wp, which is slightly above the module price at that time. The average module production cost of $0.64/Wp is assumed for the end of 2013 [3]. The stable price development of 2013 driven by the development of the previous two years and anti-dumping initiatives in the USA, Europe, India and China provided breathing room for module production costs to catch up with prices. The industry has currently already reached a price level in 2014 that was expected with a deployment of 350–400GWp of cumulated installed capacity – a level that will most likely be reached between 2016 and 2017 [14]. The values for subsequent years are calculated on the assumption of average cost reductions between 3 and 5% per year. Module shipments in 2014 are assumed to be 50GWp [5]. For the years beyond 2014 an annual growth of between 60 and 70GWp is expected [15].

Fig. 15 shows a plot of the ITRPV cost trend together with the historic price learning curve; the calculated learning rate for this cost trend is 23.5%, slightly ahead of the historic price learning rate. The analysis emphasizes the potential of the c-Si PV industry to support further cost, and hence price, reductions. Future cost reductions for c-Si modules will further improve the cost structure of c-Si-based PV systems, lower the LCOE and increase the potential market size. Moreover, a lower LCOE will enable entire customer groups to supply themselves with low-cost electricity by the end of the decade at well below retail electricity prices – and therefore position PV as a major global source of energy in the 21st century [16].

> "The PV industry will be able to provide highly competitive power-generation products compared with conventional and other renewable sources of energy."

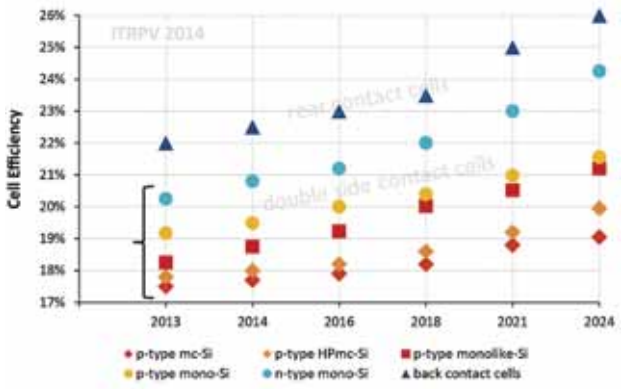

Figure 13. Stabilized cell efficiency trend curves for different c-Si cell concepts.

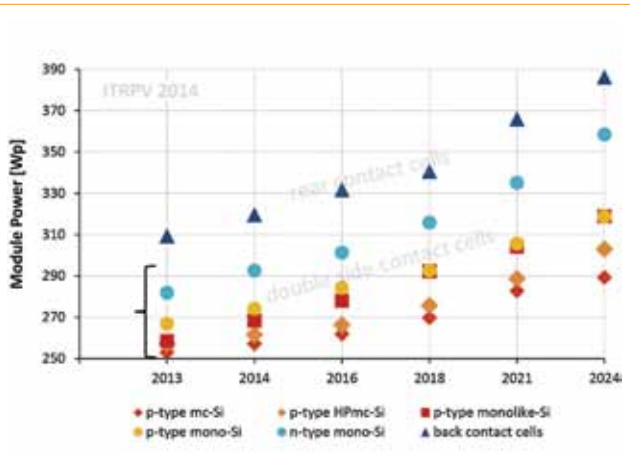

Figure 14. Module efficiency trend curves for different c-Si cell concepts.

	06/2012	12/2012	12/2013	12/2014	12/2016	12/2018	12/2021	12/2024
Cum. volume shipped [GW]	92	110	150	200	320	440	630	850
Avg. Wp increase (period to period)			3%	3%	3%	4%	5%	5%
Cost reduction (period to period)			6%	6%	8%	10%	10%	10%
ITRPV cost trend [US$/Wp]	0.83 [13]	0.73	0.64 [3]	0.58	0.52	0.45	0.38	0.33

Table 1. Module manufacturing cost trend based on the predictions of the 5th edition of the ITRPV [7].

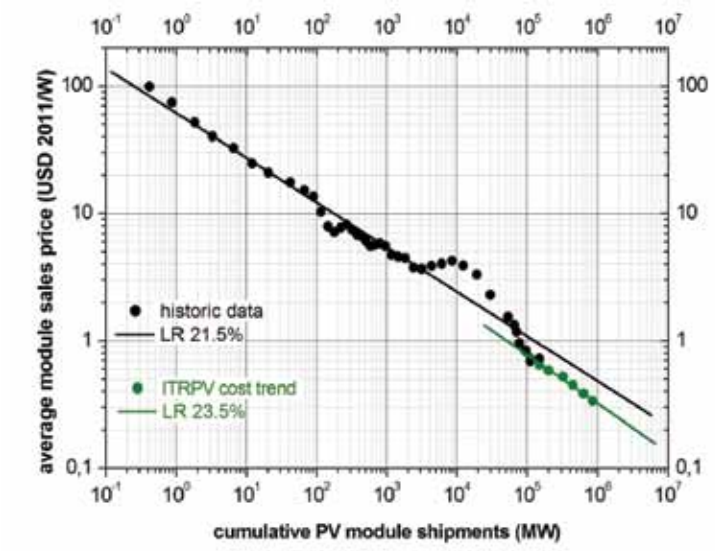

Figure 15. C-Si module cost trend of Table 1 combined with the historic sales price learning curve for PV modules.

The 5th edition of the ITRPV [7] contains an analysis of the LCOE trend at different insolation conditions, taking into account the discussed cost-reduction capabilities of c-Si PV modules. It is shown that today's LCOE of $0.05–0.10/kWh can reach a level between $0.03 and $0.07/kWh. Contemporary c-Si cell technology consequently supports the long-term progress of PV-based power solutions. The PV industry will therefore be able to provide highly competitive power-generation products compared with conventional and other renewable sources of energy.

The data for the ITRPV 5th edition [7] were collected in 2013 from leading international PV manufacturers along the c-Si value chain, PV equipment suppliers, production material providers and PV institutes. Information about how to get involved in the roadmap activities is available on the website www.itrpv.net.

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Markus Fischer studied physics at the Dresden University of Technology and received his Ph.D. in electrical engineering in 1997 from the University of Stuttgart. After working in the semiconductor industry in different engineering and management functions at Siemens, Infineon, Philips and NXP, he joined Hanwha Q CELLS in 2007. As director of R&D processes, Markus is responsible for the process development of c-Si solar cells as well as for the Hanwha Q CELLS research and module test lines. Since 2010 he has been a co-chairman of the SEMI ITRPV for c-Si technology.

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