Cell modifications for preventing potential-induced degradation in c-Si PV systems

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ABSTRACT

Potential-induced degradation (PID) in modules is a serious reliability issue for large PV systems. For commercial modules incorporating p-type cells, it has been established that local shunts in the cell are responsible for the degradation. In the case of modules with n-PERT (passivated emitter, rear totally diffused) cells, it has been predicted (and recently confirmed on a laboratory scale) that a different form of PID can occur, i.e. PID by surface polarization. The latest research at ECN has demonstrated the prerequisites for PID-stable n-PERT modules. The susceptibility to PID of n-PERT cells can be drastically reduced by modifications at the cell level, in particular to the anti-reflection coating. In this paper the mechanisms of PID in p-type and n-type cells are compared, as well as mitigation or prevention strategies, which can be either generic or specific to one of the mechanisms. In the concluding section, the implications for other cell architectures based on c-Si are also considered.

Introduction

In recent years, potential-induced degradation (PID) has been recognized as a serious reliability issue for large PV systems, potentially causing efficiency losses of more than 90%, and even failures [1–4]. Such large decreases in efficiency may require the modules in the system to be replaced after just a few years' operation. This has motivated a substantial research effort in the PV community, leading to a better understanding of the phenomenon, as well as to a range of mitigation strategies. A recent publication by Luo et al. gives a comprehensive overview of this research [5].

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PID is caused by a leakage current that is the result of a voltage difference between the frame of a module and the cells it contains. Manifestations of PID are dependent on the sign of the voltage bias, as well as on the cell architecture. The prevalent degradation mechanism for industrial cells at a negative voltage bias has been found to be the deposition of sodium (Na) atoms in the front-side emitter of the cell, resulting in local shunts and a loss in fill factor (*FF*) [6,7]; this mechanism has therefore been termed *PID-s*. Preventive measures against PID-s consist of modifications at the system, module or cell level, mostly aiming to avoid the drift of Na^+ ions into the cell [2,8].

Unlike modules incorporating conventional industrial cells, however, little attention has been paid to PID in modules containing next-generation types of c-Si cell, such as n-PERT (passivated emitter, rear totally diffused) or IBC (interdigitated back contact) cells. Nevertheless, PID in modules with n-type IBC cells at a positive voltage bias has already been reported by SunPower in 2005 [9]; in the same paper it was predicted that n-PERT cells would also be susceptible to PID. Also motivated by recent reports in the literature [10–13], ECN therefore conducted investigations of PID of its bifacial n-Pasha cells, which are mass-produced by Yingli under the Panda brand name [14].

ECN's results confirmed the findings of SunPower and others that the prevalent mechanism for PID in n-PERT cells is surface polarization, a mechanism termed *PID-p* that does not involve sodium atoms [9,10,12,15,16]. At the cell level this degradation predominantly exhibits reductions in short-circuit current density (J_{sc}) and open-circuit voltage (V_{oc}), rather than a decrease in *FF*. In the research carried out at ECN, it was found that PID-p is strongly dependent on the anti-reflection (AR) coating, consisting of non-stoichiometric SiN_x. By using a stack of SiN_x layers instead of a uniform layer, PID-p can be virtually eliminated in n-PERT cells [15,16]. Such modifications do not compromise the AR or passivation properties of the coating.

On the basis of the difference in PID mechanisms, it was also expected that PID might be easier to deal with, or more easily prevented, in systems with n-PERT cells than in systems with industrial p-type cells, including passivated emitter rear cell (PERC) devices. The following sections will first summarize some experimental findings with p-type and n-type modules in the field, as well as giving an outline of PID test methods and their relation to field observations. The mechanisms of PID in both p-type and n-type cells will then be presented and compared, and respective mitigation strategies discussed. The focus will be on modifications for preventing PID that can be made at the cell level.

PID in systems and modules

Observations of PID in the field

Swanson and co-workers from SunPower reported one of the first cases of loss of power in field-

mounted modules in Germany, after only a few months of operation [9]. Interestingly, the degradation seemed to be dependent on the location in the module string, with modules at the highest, positive voltage end of the strings exhibiting the highest degradation rates by far.

PID is observed more often, and is more severe, in locations with high temperatures and high humidity, such as Singapore and Florida, than in drier or cooler places, such as Andalusia, Spain, and Berlin, Germany. On a smaller scale, it has also been observed that PID is more likely to occur near the sea, where salt is present and the humidity is higher.

PID can affect all solar cells in a module, but in the field a distinction is made between *surface* PID and *frame* PID [17]. This distinguishes PID-affected modules on the basis of the degradation pattern: either a selection of cells is degraded in a 'random' pattern, or the degradation occurs mostly, or even solely, in those cells on the outside of the solar panel, in particular the bottom row of cells. As the name implies, frame PID occurs near the edges of the module; it is promoted by a higher conductivity near the bottom edge of the module due to dirt accumulation, which accelerates the degradation of the bottom row of cells relative to the other cells. Alternatively, PID can occur under dry conditions, but only near the four edges of the module. As a result of low humidity, leakage current pathways between the frame and the cells will only be possible close to the frame of the module.

Not only have PV modules been reported to show degradation in the field, but also their recovery has been observed. Hacke (NREL) showed that PID-susceptible p-type modules placed outdoors in Florida at –600V during the daytime exhibited a large power loss of the order of 10 to 30% between July and October; subsequently, between January and April, all of these modules demonstrated a certain amount of recovery [18]. LG reported on the recovery in n-type modules which can take place during a normal day–night sequence [11]; in that paper LG claim that under conditions of strong illumination, i.e. 1000W/m^2, the leakage current is suppressed, and that this prevents the polarization of the cell surface.

Origin and possible limitations of the voltage bias

In a PV array with string inverters the solar panels are connected in series, building up voltage along the string.

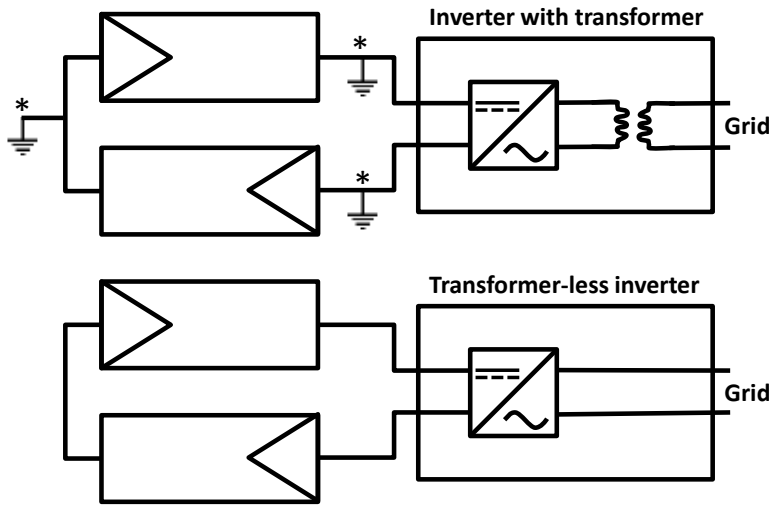

Figure 1. Schematic of a PV system incorporating an inverter with a transformer (top) and a transformer-less inverter (bottom). The locations indicated with an asterisk and a grounding symbol can be selected (one per circuit) for grounding the circuit of the PV system.

A distinction must be made between inverters with transformers and transformer-less inverters that have been coming on the market in recent years. In systems with transformers (Fig. 1, top), there is a galvanic separation between the solar panels and the electricity grid; therefore, one can ground the electric circuit of the PV system at one point, e.g. one of the two poles of the system-side of the inverter. In systems with transformer-less inverters, there is a continuous conducting path from the electricity grid via the inverter and the cabling to the solar cells (Fig. 1, bottom). Grounding a system with transformer-less inverters is no longer possible, as this would lead to a short circuit between the grid and the ground.

In the initial findings reported by SunPower with regard to degradation induced by a positive system voltage, an obvious solution was already indicated. By grounding a PV system that includes an inverter with a transformer, on the positive pole of the DC side of the inverter, the system voltage for all modules in the entire string can only be negative with respect to ground [9]. Similarly, for commercial p-type modules, where degradation occurs in modules at a negative voltage, grounding the system at the negative pole will be an effective preventative measure.

The above mitigation strategy has the disadvantage that it halves the allowed number of modules in a string, as one of the two polarities is out of bounds; it also relies on the system installer (who might install p-type modules one day and n-type modules the next) to ground the system at the appropriate pole. Furthermore, with the emergence of transformer-less inverters, because of their better DC to AC conversion efficiency, this strategy is no longer available.

PID testing and relation to real-life data

The IEC standard 62804-1 has been developed over the past few years as a qualification test for modules. The PID is accelerated at 60° and 85% relative humidity (RH) by applying the maximum intended system voltage, often 1000V, with the appropriate sign(s), for 96h. The voltage is applied between the module frame and the shorted solar cells of the panel. For frameless modules, the voltage is distributed over the front of the solar panel via an Al foil. A pass or fail of the test will be assigned on the basis of the criterion that there is a power loss of less than 5% after 96h under these conditions.

For R&D purposes it is highly desirable to know not just whether the module is susceptible to PID, but also how fast the PID progresses with time. In addition to the qualification test, the progression of PID can be monitored, for example by measuring dark I–V or R_{shunt} (in the dark) at regular intervals during PID exposure or by measuring I–V

curves under illumination at fixed time intervals, such as every 20h. Moreover, to test the PID susceptibility of the cell, single-cell modules are often used.

At the Fraunhofer Centre for Silicon Photovoltaics (CSP) a device that exposes solar cells to PID-like conditions has been developed without the need for encapsulation of the solar cells or for placing the cells in a climate chamber [7].

Data exist in the public domain for PV modules that have been degraded in accelerated PID tests and have been exposed outdoors at high voltage. This enables a connection to be made between the degradation rate indoors and the expected degradation rate outdoors. NREL has published data that show a power loss of 10–20% after around four months during spring and summer in Florida, when –1000V was applied during daytime hours. The same modules exhibited a power loss of approximately twice as much, i.e. 35%, after 60°C/85% RH/–1000V/96h when tested indoors. On the assumption of linear degradation rates, a module that would just pass the IEC standard test would have a degradation rate that is one-seventh that of this module; this corresponds to an extrapolated power loss of between 10 and 20% of its nameplate power after 28 months in Florida [18].

Mechanisms of PID in cells

Root cause of PID: the leakage current

For both PID-p and PID-s the leakage current that arises between the grounded frame and the cell under voltage bias conditions has been identified as the root cause of degradation. Fig. 2 shows several pathways of this leakage current from the frame to the biased cell. In the lateral direction, the pathway along the front glass surface ('1' in Fig. 2) will be favoured, especially in high-humidity conditions, as will the pathway between the encapsulant and the glass ('2' in Fig. 2) [19]. The backsheet usually has a very high resistivity, and the leakage current through the rear of the module will therefore be small.

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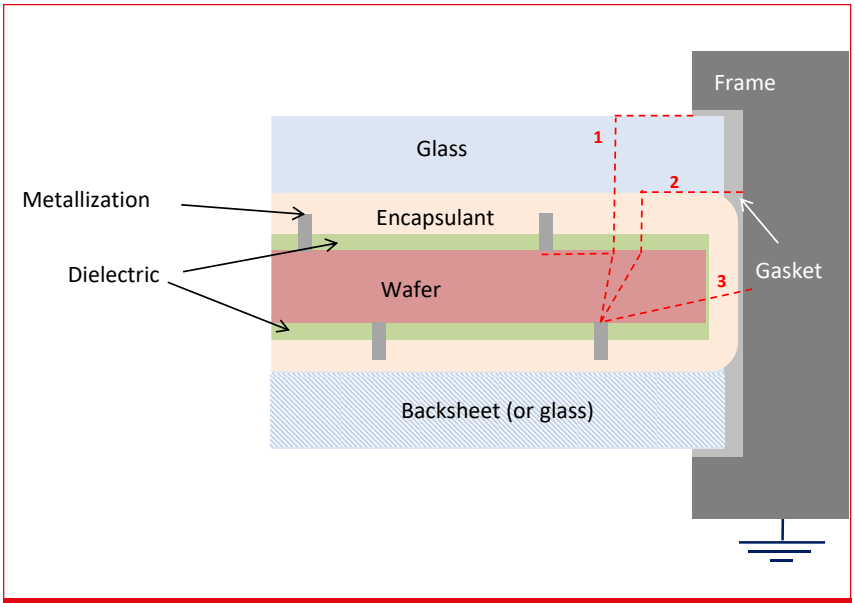

Figure 2. Schematic showing possible leakage current paths (dashed red lines) between the metallization of the cell and the grounded frame (not to scale).

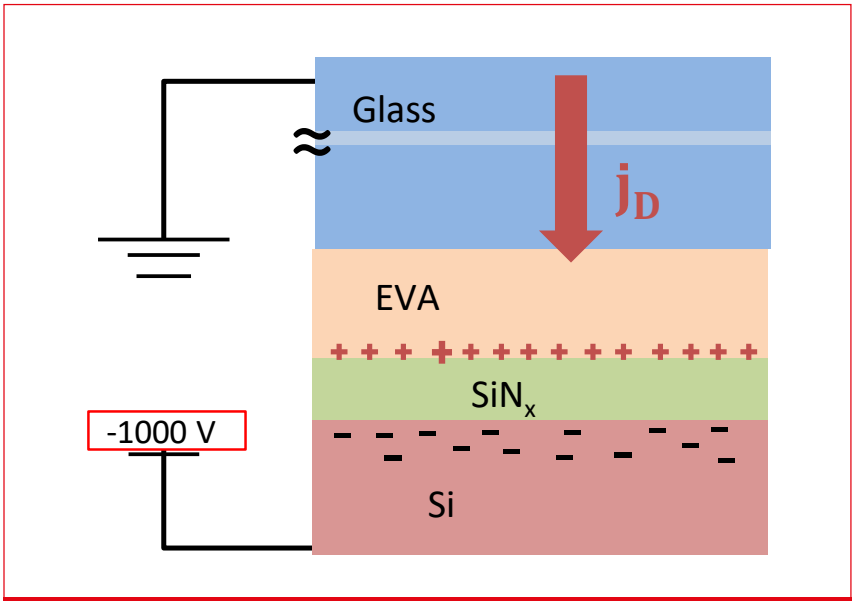

Figure 3. 1D schematic of leakage current at a negative cell bias.

To reach the metallization of the cell, which carries the voltage bias, the current also needs to have a transverse component. This transverse component will not be uniform over the cell area, but it will be present in the sections between the metallization lines, as the doped Si wafer has a high conductivity and can therefore carry current in the lateral direction ('1' in Fig. 2). The transverse leakage current is thought to be responsible for the loss of efficiency in the cells.

Often a simplified 1D scheme like the one shown in Fig. 3 is used to explain the degradation. To reach the cell, the leakage current has to pass the glass, the encapsulant (usually EVA) and a dielectric layer, the AR coating. The local leakage current j_D is the result of the total voltage bias and the resistivity and thickness of these materials. The glass (4mm) and EVA (200µm) are orders of magnitude thicker than the SiN_x coating (only 70nm); hence, the leakage current is mostly determined by the resistivity and thickness of the encapsulant and the glass. The resistivity of both glass and encapsulant strongly depends on temperature and humidity, which means that in PID test conditions the actual local leakage current density is higher than that in most outdoors conditions. Swanson reported a value of 0.6nA.cm^{-2}, while others have reported typical values during testing of up to 10nA.cm^{-2} [9,19]. The voltage drop over the dielectric is of the order of a few volts.

In order for the leakage current to pass through the highly resistive

dielectric layer, a large electric field is required. This field will be provided by the accumulation of charges at the interface of the dielectric and the encapsulant; these charges are mirrored by opposing induced charges at the surface of the silicon wafer. There has so far been no discussion of the nature of the accumulated charges or of the species forming the leakage current. In the case of a positive voltage bias, the current and the charges will be electronic in nature; however, a complication arises when the voltage bias is negative, as metal ions (Na^+ ions in particular) are also mobile in the system. The Na^+ ions can originate from the glass (often soda-lime glass is used), or from contaminations of the SiN_x surface or from out of the SiN_x bulk. Both the accumulated charges as well as the leakage current itself can consist of Na^+ ions. In the following sections it will be explained that Na plays a major role in the PID-s mechanism, whereas it is not relevant in the case of PID-p.

Shunting in industrial p-type cells

A negative voltage bias of the cell relative to the frame causes an electric field in the direction of the wafer. By using time-of-flight secondary ion mass spectrometry (TOF-SIMS), high-resolution transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDX), Naumann et al. at Fraunhofer CSP have shown that, during PID tests on industrial cells with an n^+-emitter, Na^+ ions drift through the dielectric layer [6]. In the n^+ emitter the Na^+ ions are reduced by the free electrons, and Na atoms then decorate stacking faults in the Si wafer.

The above mechanism is nicely illustrated in Fig. 4, taken from the paper by Naumann [6]. The reduction in Na^+ ions implies that they do not contribute to an opposing charge at the bottom of the dielectric layer, i.e. the drift of Na^+ ions is continued. The Na atoms can thermally diffuse further along the stacking faults, which extend through the emitter into the p-type base. One resulting effect is that a semi-metallic path between the surface of the cell and the base is created, which leads to a local shunt ('process 1' in Fig. 4). A second effect is that the Na atoms form recombination centres in the p-n junction area, leading to an increased ideality factor ('process 2' in Fig. 4). Both effects have a large negative impact on *FF*, and can result in efficiency losses exceeding 90%. The group at CSP have also confirmed, by means of electron beam induced current (EBIC) and dark lock-in thermography (DLIT), the correlation between shunted regions and regions with high Na content [6,7].

Stacking faults occur intrinsically in both monocrystalline and multicrystalline material. It has been reported that these faults are also formed during $POCl_3$ diffusion (extrinsic stacking faults) [6]. It seems not to be entirely clear whether both play a role in PID; moreover, according to recent reports, stacking faults are also induced, or grow, during PID [20]. Naumann et al. attribute a special role to the thin silicon oxide (SiO_x) layer at the SiN_x/Si interface; this thin layer is supposed to facilitate thermal diffusion of Na^+ in the lateral direction, so that the Na can reach the stacking faults [6].

PID in standard PV modules is

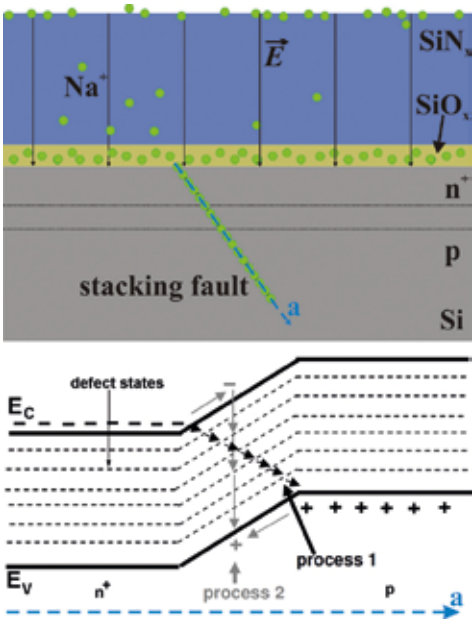

Figure 4. Schematic of a solar cell cross section. Na^+ ions drift, as a result of the dielectric field, towards the Si interface, where diffusion into stacking faults takes place. The bottom graph shows the proposed band structure along a decorated stacking fault. (Reprinted from Naumann et al. [6] with permission from Elsevier.)

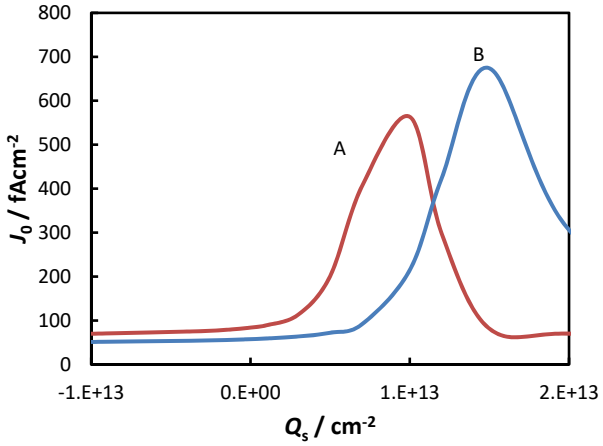

Figure 5. Calculated J_0 values of emitters A and emitter B as a function of an applied external charge Q_s. The recombination velocity S at the surface, for holes and electrons, was set to 2000cm.s^{-1}

reversible, for example by applying a reverse voltage bias, or the efficiency can be restored at elevated temperatures without a bias. [1,2,21]. Microscopy studies have shown that, after subjecting cells affected by PID-s to a reverse bias or to a thermal process at 250°C, the stacking faults become free of Na, and cell performance is restored [22]. There is still some doubt as to what may be the effect of repeated PID-s exposure/recovery sequences. There are indications that the formation of stacking faults during PID tests is not quite reversible; on the other hand, there are reports that degradation becomes less in subsequent PID tests [5].

Surface polarization of c-Si

Although PID by surface polarization has not been described in great detail in the literature, it is very relevant to next-generation cells, such as IBC and n-PERT. PID-p occurs with a positive voltage bias at n-type surfaces and with a negative bias at p-type surfaces. As pointed out in the discussion of Fig. 3, the electric field across the AR coating results in a space charge in the Si wafer; this means that, as depicted in Fig 3, at a negative voltage bias electrons are attracted to the surface, and holes are repelled from it. In the case of a p-type surface, the result is enhanced surface recombination. At a positive bias, electrons are repelled and holes are attracted, with similar detrimental surface recombination for n-type surfaces (i.e. emitter surface on p-type cells).

In the case of a dielectric with resistivity ρ and dielectric constant ε, the charge density Q seen by the Si wafer is determined by the electric field $E = Q/\varepsilon$, which is in turn determined by the leakage current according to $j_D = E/\rho$, i.e. $Q = j_D \cdot \rho \cdot \varepsilon$. After substitution of appropriate values for the resistivity and dielectric constant, it was calculated that charge density values corresponding to the observed leakage currents can become as large as 10^{12}–10^{13}cm^{-2}, and such high values will impact the surface passivation of emitters.

The effect of this surface polarization can be studied in detail by numerical simulation. Fig. 5 shows the calculations of the recombination parameter J_0 of two typical boron emitter profiles (both ~60Ω/sq.), as a function of an external charge density Q_s, i.e. producing a space charge density $-Q_s$ in the diffused region of the wafer. The total surface recombination is to a good approximation proportional to this parameter J_0. Emitters A and B were both formed in the same diffusion process; in the case of emitter B, however, the 30nm-wide boron depletion zone had been etched way, leading to a higher surface concentration. At a negative external Q_s, holes are attracted to the surface, and surface recombination is actually reduced compared with the zero-charge case. But as Q_s becomes more and more positive, J_0 increases steeply, until it reaches a maximum at the charge density for which the concentrations of holes and electrons are equal. At an even higher charge density, the situation arises that the concentration of holes at the surface is lower than that of electrons, which again leads to improved passivation conditions. Because of the higher surface concentration of emitter B, a large Q_s is required in order to obtain a similar impact on J_0. The J_0 will also depend on the fundamental electron and hole recombination velocity at the surface S, which is proportional to the density of surface states D_{it}.

Numerical device simulations can also illustrate the effect of surface charges on the I–V characteristics of n-PERT cells, which resemble the n-Pasha cells of ECN. With emitter A, assuming good surface passivation, the results in Fig. 6 are obtained. For Q_s values of the order of 10^{12}–10^{13}cm^{-2}, the simulations predict a large effect on J_{sc}, a comparatively smaller but significant effect on V_{oc}, and minor changes in FF. A maximum of 16% loss in cell efficiency is predicted.

These results are in good qualitative agreement with recent

experimental results obtained at the ECN laboratory, as well as with those reported by others for n-PERT cells [10,12,15,16]. For the purpose of these experiments, a uniform SiN_x layer with refractive index n = 1.97 was applied as the AR coating to ECN's n-Pasha cells. Fig. 7 demonstrates the significant effect on J_{sc} and V_{oc} of exposure to PID test conditions, thus corroborating the mechanism of enhanced surface recombination. Hara and Bae published external quantum efficiency (EQE) results confirming that the blue response of the cells is diminished [10,12]. The degradation is slower for the cell with emitter B; this is in agreement with Fig. 5, which predicts that higher values of Q_s are required for a similar impact on the J_0 of the emitter. It should be noted that, although the *FF* is not significantly affected by PID-p at the single-cell level, the situation may be different in modules where mismatches in J_{sc} and V_{oc} of cells at different positions along the string can result in module *FF* losses [5,9].

In the case of emitter A, the efficiency loss appears to reach a maximum value at a certain point during the test; this limitation is expected, because the maximum J_0 will be limited, but also because the leakage current j_D will limit the electric field. As j_D is non-uniform over the cell area, and its distribution may even change during testing, it is not possible to say what the limiting factor is in this case. In this respect, PID-p differs from PID-s, where for the latter there is a continuous increase in the amount of Na in the wafer.

In agreement with the PID-p mechanism, the results of PID tests with IBC cells also show mainly effects on J_{sc} and V_{oc}; these effects, however, can be larger than those for n-PERT cells, since IBC cells are more sensitive to front-surface recombination [23,24]. In p-type cells, where a negative bias induces PID-s, a positive bias may induce PID-p. Although there have been some observations suggesting this, it is also expected that, because of the very high surface concentrations of phosphorus emitters, large fields will be necessary in order to see an effect [9]. Since the polarization effect is essentially an electronic effect, it is entirely reversible by removing the bias or by applying a reverse bias [11].

A final question to be asked is: why do Na^+ ions not appear to play a significant role in the PID of n-PERT cells at a negative bias? No Na has ever been reported so far in the p^+

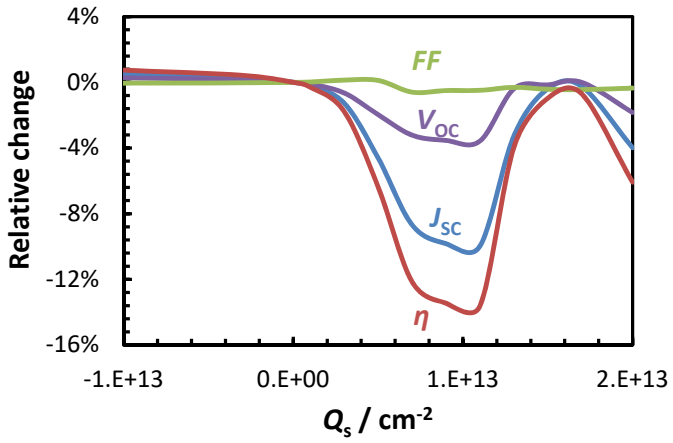

Figure 6. Relative changes in the *I–V* characteristics of an n-PERT cell with emitter A.

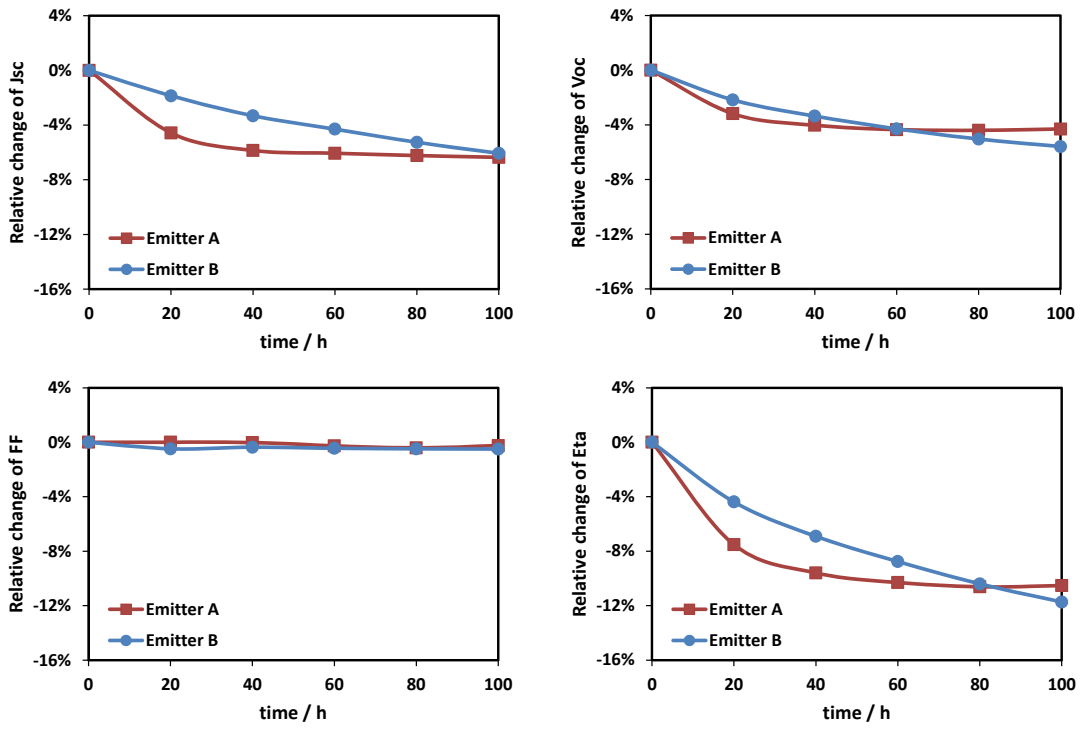

Figure 7. Time evolution of the cell parameters relative to initial values, for n-Pasha single-cell laminates (mini-modules) tested for 100h PID exposure (–1000V, 60°C, 85% RH), with a uniform n = 1.97 SiN_x layer on emitters A and B.

emitters after exposure to a negative bias. One explanation could be that at p^+ surfaces Na^+ cannot be reduced, and hence there is no sink for Na^+ ions [5]. Another hypothesis is that stacking faults in boron-doped material are not large enough to accommodate Na [12]. This does not imply that Na^+ cannot accumulate at the interfaces, but in steady-state conditions the Na^+ drift current will be compensated by a diffusion current in the opposite direction.

Corroborating this essential difference between n-type and p-type surfaces are the observations by Yamaguchi et al., who studied an n-PERT cell with a rear junction [25]. At a negative bias, they observed enhanced surface recombination, which cannot be due to polarization, since at a negative bias this would improve the surface passivation; instead, they proposed that Na atoms in the stacking faults form additional recombination centres. Note that, because the emitter is on the other side of the cell, these Na atoms do not cause a shunt or enhanced p-n junction recombination.

Solutions for PID

Generic solutions: reduction of the leakage current

In the earlier discussion of the root cause of PID, it was pointed out that the magnitude of the leakage current, and of the resulting electric field across the dielectric AR layer, is the root cause of PID. As previously discussed in the section on PID in systems and modules, adaptions at the system level to prevent this are costly or impractical. At the module level, however, several solutions have been suggested. These aim to reduce the leakage current by providing a higher electric resistance of the glass and/or encapsulant, which is an effective strategy, since the leakage current is determined by the glass and the encapsulant (see section on root cause of PID).

Alternative glass materials – such as quartz, borosilicate glass and aluminosilicate glass – are available which have volume resistivities that are greater by two to three orders of magnitude. With quartz as the front-side material, it is possible to completely avoid PID-s in conventional modules [26]. One reason for this enhanced resistivity is that glasses of this type contain little or no sodium, which also eliminates an important source of the Na causing PID-s. Nevertheless, a serious drawback of alternative glasses is that they add considerably to the module cost.

A more commonly adopted solution is the replacement of standard EVA with a high-resistivity encapsulant. Silicone, polyolefins and ionomers have volume resistivities of up to two orders of magnitude greater than the resistivity of EVA; moreover, the resistivity of these materials is less dependent on temperature and relative humidity, and their transmittance for visible light is similar to (or better than) that of EVA. Other considerations are mechanical strength, UV stability and adhesion, but these high-resistivity materials seem to be good candidates for replacing EVA; their capacity for reducing PID has been confirmed in several reports [8,26,27]. Again, as in the case of glass, these alternative materials come at a higher cost.

Specific solutions for reducing PID-s

Since it was already suspected at an early stage that Na ions could be the origin of the shunts in industrial cells, the incorporation of Na barriers into the module or the cell has been investigated as a solution, similarly to the Na-lean glass mentioned above. Hara et al. obtained improved PID resistance by inserting a TiO_2 foil between two layers of encapsulant [28]; however, this material results in less visible light reaching the cell, thus reducing the efficiency. Other attempts, including a SiO_2 layer adjacent to the glass, have proved less effective, with similar light absorption losses [26].

It has been widely reported that modifications of the dielectric stack can be effective in reducing PID-s [6,8,29–32], in particular by using a more Si-rich nitride, which is more electronically conductive. On the one hand, this may provide a lateral path for the current to the metal grid, thus by-passing the wafer (see Fig. 2); but perhaps more importantly, it would imply that the transverse degradation current in that layer would be made up more of electronic charges than of Na^+ ions. Indeed, as formulated by Luo et al., the electric field experienced by the Na^+ ions becomes smaller, and hence their flux becomes smaller [5]. The Si-rich, conductive layer, however, will also have a higher refractive index with higher light absorption. To overcome this drawback, Mishina et al. proposed a multilayer SiN_x coating, with the outer, or upper, layer having a low refractive index [31], which resulted in cells with both higher PID resistance and higher initial efficiency.

On the other hand, there have been several reports claiming that the insertion of a SiO_2 or an oxide-rich SiN_x with higher conductivity between the Si wafer and the AR coating provides an efficient Na^+ barrier or Na^+ trapping layer [8,33,34]. The role of the thickness of this layer, as well as its long-term PID resistance, is still a point of debate [5].

Specific solutions for reducing PID-p

PID-p is essentially a surface recombination phenomenon. A logical assumption would therefore be that a reduction of the surface recombination parameters S, i.e. a reduction of D_{it}, would reduce PID-p. Although this is probably true for exceptionally low values of S, according to Fig. 5 a very large J_0 can occur in depletion conditions, even if the S is as low as 2,000cm.s^{-1}, a value lower than that obtained for the 'excellently' passivated boron surfaces [35]. Hence, better surface passivation achieved either by improved S or by increased surface concentration will just slow down the PID but not limit it. A similar result was found at the ECN laboratory, with only a 5% efficiency loss in the 96h PID test after the insertion of a 6nm AlO_x layer between the wafer and the uniform AR layer [16]. While such improvements may in practice be acceptable (e.g. in field conditions where PID only occurs in the morning, which is later reversed when conditions are much drier), they will not always be deemed sufficiently robust.

> "The best prevention strategy for PID-p is the application of non-uniform AR coatings"

The best prevention strategy for PID-p, however, is the application of non-uniform AR coatings [15,16]. Fig. 8 shows the degradation of the n-Pasha cell with emitter A (also shown in Fig. 7). When the 70nm dielectric SiN_x (refractive index n = 1.97) was replaced with a stack of two layers, namely a SiN_x layer of 54nm on top (n = 1.97) and a more conductive 18nm SiN_x layer (n = 2.44) on the bottom (i.e. adjacent to the wafer), a much less pronounced and limited PID was observed. This can be explained by the reduction in the electric field over the more conductive Si-rich layer, and hence the reduction in polarization charge seen by the Si wafer, even when the total leakage current is the same. As explained earlier, the relation between polarization charge Q and leakage current j_D is $Q = j_D \cdot \rho \cdot \varepsilon$. Of course, the Si-rich layer may also result in lower

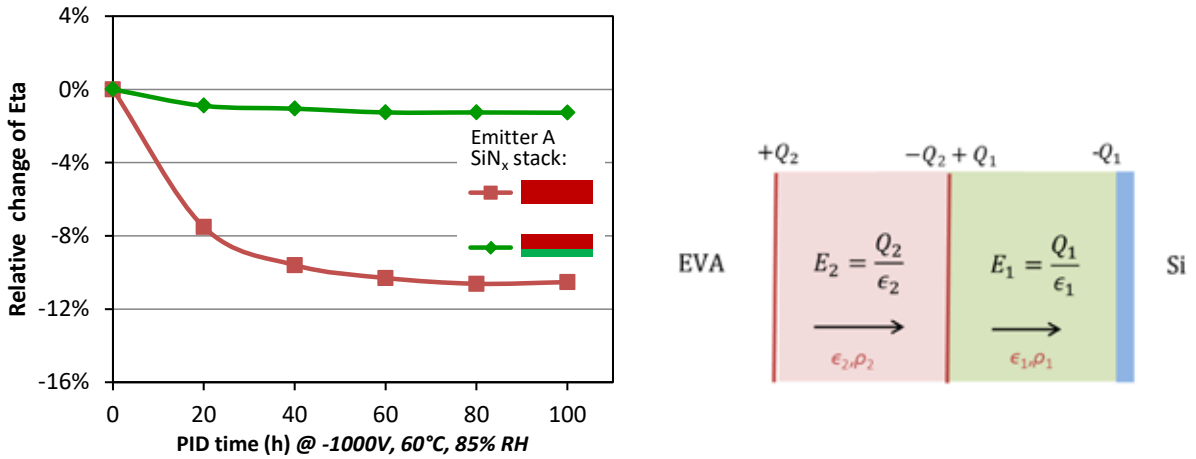

Figure 8. The graph on the left shows that an n-Pasha cell was made PID-resistant by replacing the uniform dielectric coating (red line) by a two-layer stack with a Si-rich conductive layer on the bottom (green line). The equations on the right explain how this improvement is brought about. In the uniform layer with resistivity ρ_2, the wafer would see the charge Q_2, associated with the electric field E_2. By inserting a layer with lower resistivity ρ_1 next to the wafer, a smaller field E_1 is needed to let the current j_D pass, which means that the wafer sees a smaller charge, i.e. Q_1.

D_{it} but, as already indicated in the section on surface polarization of c-Si, this will not be sufficient to limit PID.

In addition, for PID-p the order matters in which the layers with different conductivity are positioned in the dielectric stack. Fig. 9 shows a comparison, for the n-PERT cell with emitter B, of the cases where the more conductive Si-rich layer is adjacent to the wafer, on top, or in the middle of a three-layer stack. In the first case, a minimal and stable efficiency loss can again be seen; in the other two cases, however, a substantial loss is evident. There might be some mitigation in these cases because of a lateral current, but when a more resistive layer is placed adjacent to the Si wafer, then PID is clearly increased. This can be explained using the expressions on the right of the graph in Fig. 8: when the resistivity of the layer adjacent to the Si wafer is higher, the electric field over the layer is higher, and thus the charge Q_1 is now larger than Q_2, resulting in more surface recombination.

The mechanism given here is based on ohmic charge transport, which is probably not applicable for very thin oxide layers, where charge transport will take place by tunnelling or through pinholes that have a low resistivity. For charge transport through such layers, the electric field, and hence the required interfacial charge density, will be much smaller. In fact, in all ECN's n-PERT cells, a very thin (~1.5nm) passivating SiO_x layer was formed on the emitter by wet chemical oxidation (NAOS) [36]; however, as shown by the results in Figs. 8 and 9, such a layer does not induce

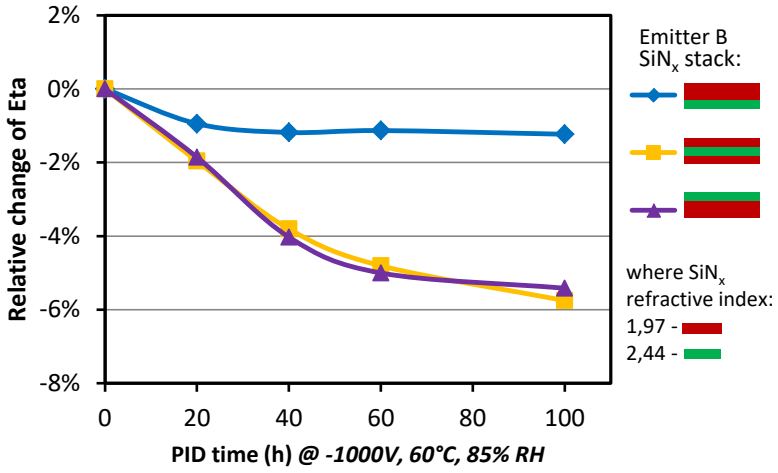

Figure 9. Layer positioning comparison, showing that a PID-resistant cell is only obtained when the Si-rich conductive layer is placed adjacent to the cell. In the other cases, significant degradation is still observed during PID testing.

PID. Similarly, PID-resistant n-PERT cells were created at the ECN laboratory using a 6nm AlO_x passivation layer between the emitter and the Si-rich conductive layer of the AR stack [16].

As also pointed out by Mishina [31], the introduction of a thin Si-rich conductive layer next to the Si wafer will not lead to more parasitic absorption when the top layer has a refractive index $n < 2$. The passivation of the cell is even improved by this layer, rather than degraded. Besides providing PID resistance already at the cell level, the described modification of the AR coating requires only minor changes to the standard plasma-enhanced chemical vapour deposition (PECVD) method of SiN_x deposition, and therefore represents a high-throughput, cost-effective solution.

Concluding remarks

As the understanding of PID in c-Si increases, it becomes clear that different mechanisms of PID can apply. In industrial p-type cells the n^+

emitter can be shunted by Na atoms (PID-s), leading to drastic reductions in *FF* and thus in output power. The Na^+ transport is driven by the electric field and Na deposits in stacking faults, thus providing a sink for Na^+ ions which facilitates a continuous Na^+ migration. It must be expected that PERC cells will be similarly affected.

In contrast, cell types based on n-type material are susceptible to PID by surface polarization (PID-p), which manifests itself at the cell level not by a loss in *FF* but by losses in J_{sc} and V_{oc}. At a positive voltage bias, n^+-type surfaces are affected by PID, whereas at a negative bias, p^+-type surfaces are affected. This mechanism does not involve Na ions but only electronic charges, and can therefore show recovery when field conditions change [11]. Moreover, the polarization effect seems to be limited, as it is the magnitude of the leakage current, rather than the accumulated leakage current, that is responsible for the efficiency loss.

The fact that PID-p can occur at both polarities has implications for cells in bifacial modules. Bifacial modules are mostly glass/glass modules, and the cells do not have a fully metallized rear; the rear side may therefore also experience a leakage current and be susceptible to PID. At a negative voltage bias, the direction of the electric field is such that it would reduce surface recombination at the rear of n-PERT cells, but this may be offset by the deposition of Na in the n^+ layer, providing additional recombination centres. At a positive bias the rear will have adverse surface polarization. For PERC+ cells at a negative bias, shunting of the emitter must be expected, as well as enhanced surface recombination at the rear. At a positive bias, the front of PERC+ cells is susceptible to surface polarization.

A better understanding of the mechanisms has promoted solutions at the cell level, in addition to the more expensive solutions that already exist at the system and module levels. Both PID-s and PID-p can be suppressed by modification of the AR coating. As demonstrated here for n-PERT cells, when a multilayer stack with a conductive layer next to the Si wafer is used the polarization effect can be effectively suppressed, resulting in only a 1% degradation over 100h of accelerated PID testing. The literature data suggest that this method is also effective in significantly reducing Na^+ transport to stacking faults in n^+-type regions. The AR and passivation properties of the stack are similar to, or better than, those of a single-layer coating. These cell modifications are easy to implement in the manufacturing process and are therefore cost-effective. Note, however, that although the proposed methods appear to be effective in a laboratory setting, they still need to be proved in field tests.

> "The PID-p effect in n-PERT cells can be slowed down by better passivation of the boron emitter."

Another finding at ECN is that the PID-p effect in n-PERT cells can be slowed down by better passivation of the boron emitter. In practice, this may be a useful consequence, since PID-p shows fast recovery, and effects such as high humidity that induce PID-p seem to occur only during part of the day. In fact, this has motivated LG to advocate a module warranty test which includes the recovery behaviour [11]. Furthermore, it must be expected that advanced cell c-Si technologies have very effectively passivated surfaces. Although heterojunction (HJ) cells have been reported to exhibit minimal PID [37], they, as well as other advanced concepts, often feature a TCO layer, which can be susceptible to electrochemical corrosion [5].

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