Achieving higher efficiencies with a low-cost etch for in-line-diffused silicon wafer cells

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ABSTRACT

Emitter formation is one of the most critical processes in the fabrication of silicon wafer solar cells. The process for standard emitter formation adopted in the photovoltaic industry is tube-based diffusion, using phosphorus oxychloride as the dopant source. A potentially low-cost alternative that typically results in lower solar cell efficiencies is in-line diffusion, using phosphoric acid as the dopant source. The Solar Energy Research Institute of Singapore (SERIS) recently developed a technique called the 'SERIS etch', a non-acidic etch-back process technology that provides a controllable, uniform and substantially conformal etch-back suitable for solar cell processing. By using the SERIS etch, efficiencies of up to 18.7% have been demonstrated for homogeneous-emitter silicon wafer cells; a 0.4%$_{abs}$ efficiency improvement has also been achieved for a unique selective-emitter approach exploiting this novel etch. All work was carried out on industrial-grade p-type Cz wafers with conventional screen-printed metallization and a full-area aluminium back-surface field (Al-BSF). With Al local BSF (LBSF) homogeneous-emitter solar cells, efficiencies of 19.0% were achieved using in-line emitter diffusion and the SERIS etch, a 0.7%$_{abs}$ efficiency increase over the baseline efficiency at the time. To the authors' knowledge, these are the highest solar cell efficiencies ever reported for in-line-diffused silicon solar cells. Moreover, the SERIS etch is a cost-effective alternative to generating pyramid-textured surfaces without using conventional metal-assisted silicon-etching processes.

Introduction

The PV industry is currently aiming for high-efficiency Si solar cells. Any gains that manufacturers can make in converting light to electricity are directly translated into better margins, provided it can be done with a minimal investment. Increasing the efficiency by 0.1%$_{abs}$ means profit margins will go up by US$200k for each 100MW of production, if no investment is required. Accordingly, an improvement from 0.4%$_{abs}$ to 0.7%$_{abs}$ in efficiency can result in a US$1 million improvement in margin. At SERIS an inexpensive way has been found for increasing the efficiency of solar cells by applying a non-acid, cheap chemical as the silicon etch after creating the emitter on a monocrystalline cell. This process has also been applied to multicrystalline cells and generates similar efficiency gains of 0.3%$_{abs}$ to 0.6%$_{abs}$.

In the PV industry a batch-based tube diffusion with a high-purity phosphorus oxychloride ($POCl_3$) liquid dopant source is the standard for the formation of the n-type emitter. Tube diffusion is a highly reliable process, which results in high-quality emitters that can be used for high-efficiency Si wafer solar cells. Complex wafer handling and automation, however, are necessary for loading the wafers into and unloading them out of the quartz carriers, and a relatively long process time per batch is required.

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In-line diffusion offers a cost-effective alternative for forming the emitter of Si wafer solar cells. In contrast to batch-based processing, in-line processing enables continuous transport of the Si wafers throughout the processing chain using belts and rollers. The employment of simple 'belt-to-belt' handovers between process steps largely eliminates complicated wafer loading and unloading; hence, large cost savings in automation can be realized by in-line processing. The use of in-line processing is well established and has demonstrated its benefits in areas such as chemical processing (texturing, etching, etc.), anti-reflection coating (ARC) deposition by plasma-enhanced chemical vapour deposition (PECVD) and screen-printed metallization. Thus, emitter formation by tube diffusion is often the only batch-based process interrupting an in-line process flow.

A multi-lane belt or roller in-line-diffusion furnace allows high throughput per tool, with an end-to-end processing time of less than 30 minutes when phosphoric acid (H_3PO_4) is applied as the phosphorus (P) dopant source. However, lower-grade chemical precursors, the short diffusion time, the open-ended design of the furnace, and the metal belt are potential disadvantages of in-line diffusion. As a result, in-line-diffused emitter Si solar cells typically achieve lower PV efficiencies compared with tube-diffused solar cells.

The short duration of the in-line-diffusion process results in a dead surface layer (due to surface contaminants and a high dopant concentration at the surface) and a very shallow junction, which limits the open-circuit voltage (V_{oc}) and the efficiency of in-line-diffused emitter solar cells. In-line-diffusion is commonly performed on both sides of the Si wafer to minimize back-surface contamination from the metallic conveyor belt and this allows additional P gettering. Nevertheless, rod-like structures of silicon phosphide precipitates are typically observed on in-line-diffused emitter surfaces, even after removal of the phosphosilicate glass (PSG) layer with a diluted hydrofluoric acid (HF) solution. Horzel et al. [1] proposed that these structures are formed during rapid cooling of the dopant solution (H_3PO_4 and solvents), involving very high P concentration above the solid solubility limit of P in Si. Thus, in order to achieve high efficiencies using in-line diffusion, a reduction or complete removal of this heavily doped dead layer and surface contaminants is necessary.

SERIS etch

Based on additional surface cleans after in-line diffusion, various cleaning or etching processes have been developed to remove the above-mentioned dead layer and surface contaminants. These processes generally provide a shallow etch-back of the anomalously doped in-line-diffused emitter surface region. Voyer et al. [2] used a mixed solution of nitric acid (HNO_3) and HF on an in-line-diffused emitter surface, as well as other processes such as the 'ECN Clean' [3], 'extended surface clean' [4], and so on. SERIS has developed its own HF-free non-acidic etch-back solution – the 'SERIS etch' [5] – which offers unique advantages compared with the current state-of-the-art techniques; these advantages are discussed in the next sections.

Uniform etching

Laterally uniform dopant diffusions, which are contactable and can result in a good blue response (e.g. because of a low recombination or the absence of a dead surface layer), are extremely important for fabricating high-efficiency Si wafer solar cells. The uniformity of the emitter is qualified by the sheet resistance (R_{sq}) as well as the diffusion depth and the surface dopant concentration. Generally, a high emitter R_{sq} is preferred with a low surface dopant concentration in order to reduce surface recombination losses. However, the formation of these so-called 'shallow emitters' is quite challenging, especially using tube diffusion, and typically these high-R_{sq} tube-diffused emitters suffer a high non-uniformity that affects the performance of the final solar cell device.

Deeper diffusions are typically much more uniform and have the additional advantage of advanced P gettering, thereby improving the bulk material quality. Thus, by using a combination of a deep diffusion with a heavy uniform etch-back, all advantages can be exploited at once, resulting in potentially higher solar cell efficiency.

A low-cost alternative to tube diffusion is in-line diffusion, which features an excellent uniformity because of the direct deposition of the dopants. However, an emitter etch-back is compulsory for in-line-diffused emitters, owing to the formation of P precipitates on the diffused surface [1]. It is essential that this etch-back does not compromise the uniformity of the initial emitter.

> "The SERIS etch enables a much deeper and uniform etch-back to be achieved, to maximize the advantages of dead layer removal and low surface concentration."

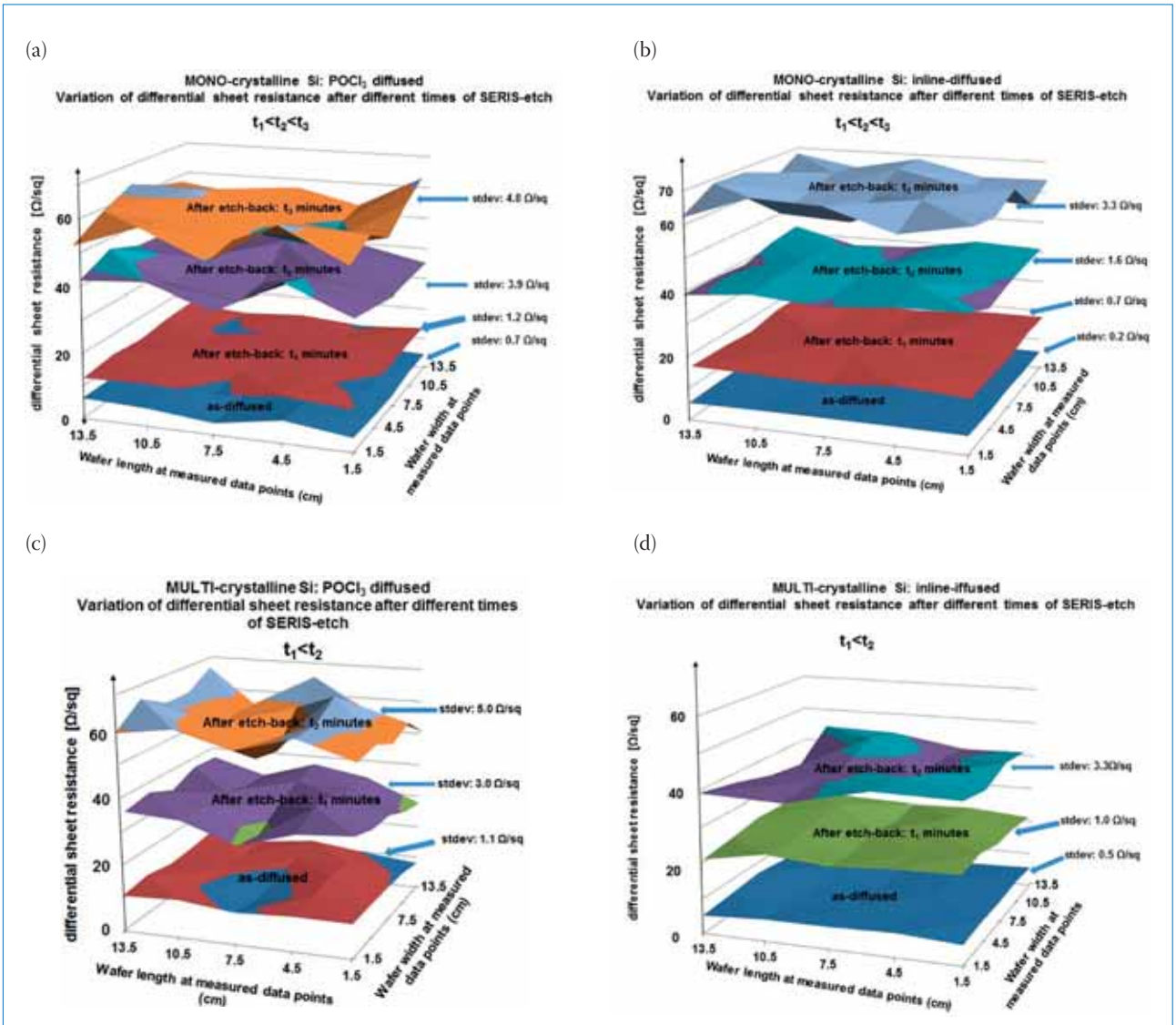

Figure 1. Variation of differential R_{sq} before and after different durations of etch-back using the SERIS etch: (a) tube-diffused ($POCl_3$) pyramid-textured mono-Si wafers (as-diffused emitter R_{sq} ~50Ω/sq); (b) in-line-diffused pyramid-textured mono-Si wafers (as-diffused emitter R_{sq} ~45Ω/sq); (c) tube-diffused multi-Si wafers (as-diffused emitter R_{sq} ~50Ω/sq); (d) in-line-diffused multi-Si wafers (as-diffused emitter R_{sq} ~45Ω/sq).

The SERIS etch enables a much deeper and uniform etch-back to be achieved, to maximize the advantages of dead layer removal and low surface concentration. The average of the variation of R_{sq} before and after the etch-back (defined here as the 'differential sheet resistance') is shown in Fig. 1 for alkaline-textured monocrystalline silicon (mono-Si) as well as acidic-textured multicrystalline silicon (multi-Si) wafers, with emitters formed using both tube (Fig. 1(a) and Fig. 1(c)) and in-line (Fig. 1(b) and Fig. 1(d)) diffusion. The sample wafers are in-line-diffused; after PSG removal in dilute HF solution, the diffused wafers are etched in the SERIS etch solution for different lengths of time. The spatially resolved R_{sq} of the emitter is measured using standard four-point probe (4PP) measurements. As can be seen, the uniformity of the etch-back on the tube-diffused and in-line-diffused emitters is comparable, with a slightly higher non-uniformity on multi-Si wafers. Typically, etch-back processes show strongly increasing non-uniformity for deeper etch-backs. In contrast to typical etch-back processes, the SERIS etch-back maintains an excellent uniformity of ≤ 5Ω/sq standard deviation (stdev) in R_{sq}, even for deep etch-backs that increase R_{sq} by more than 50Ω/sq.

Conformal etching

In any etch-back process, retaining the morphology of the original surface is an important consideration, and this is especially challenging for extended etch-backs. For the conventional etch-back process using HF-HNO_3, conformal etching is severely hampered by the non-uniform growth of a porous Si layer on the textured surface. For pyramidal Si surfaces, porous Si growth is greatest along the pyramid tips, and the pyramids are thus deformed after the etch-back process [6]. The surface reflectance therefore increases, which affects the efficiency of the final solar cell. However, as can be seen in Fig. 2, when using the SERIS etch there is no significant deformation of pyramidal structure, even after an extremely deep etch-back from R_{sq} of ~45Ω/sq to ~100Ω/sq (a typical targeted R_{sq} value for selective emitter in non-metalized cell areas). This can be explained by the chemistry of the SERIS etch: porous Si formation is not required, as the solution *directly* etches crystalline silicon. This unique etching chemistry thus allows extremely conformal etching of Si surfaces, including n-type and p-type emitters.

Surface cleaning

Tube diffusion uses high-purity $POCl_3$ as the P dopant source; during diffusion, only $POCl_3$ vapours come into close contact with the Si wafer inside the closed tube, along with high-purity oxygen and nitrogen gases. However, in-line diffusion uses a H_3PO_4-based solution as the P dopant source, which becomes physically deposited on the Si wafer in the pre-diffusion stage and then undergoes the diffusion process in the air atmosphere on a metallic conveyor belt. Hence, it is not surprising that the PSG formed during in-line diffusion contains additional surface contaminants, which are significantly more difficult to remove than the PSG formed during tube diffusion.

The residual surface contamination left on the in-line-diffused emitter surface after PSG removal can significantly compromise contacting and surface passivation. The SERIS etch process simultaneously removes these residual surface contaminants associated with in-line diffusion, along with providing an emitter etch-back. Fig. 3 shows SEM micrographs of the in-line-diffused mono-Si surface after different processing stages [7]. Even after PSG removal, a considerable amount of foreign material is visible on the surface (R_{sq} ≈ 50Ω/sq, see Fig. 3(a)). The white scaling in Fig. 3(a) represents the visible imprints of the surface contamination which will reduce the solar cell efficiency. The SERIS etch, however, effectively removes the foreign material, while maintaining the conformity of the pyramids (Fig. 3(b)). Basically the chemistry of the SERIS etch removes the deposited hard surface 'debris' arising from the in-line diffusion process. As clearly shown in Fig. 3(b), after etch-back there is an absence of surface debris, and just nanometre-size pinholes remaining in the clean Si areas.

Application of the 'SERIS etch' to in-line-diffused emitters

As discussed earlier, the SERIS etch is especially beneficial for in-line-diffused emitters and has already been successfully used to fabricate high-efficiency full-area Al-BSF homogeneous-emitter, selective-emitter (SE) and Al-LBSF Si wafer cells, with respective maximum efficiencies of 18.3% [8], 18.7% [9] and 19.0% [7]. In the case of Al-BSF and Al-LBSF solar cells, the emitter was etched back from an initial R_{sq} value of ~40–50Ω/sq to ~70Ω/sq. For SE cells, by using the SERIS etch, a unique SE process has been developed with fewer processing steps [10] compared with conventional processes [6]. In contrast with a standard in-line-diffused etch-back emitter of R_{sq} ≈ 60Ω/sq, in-line-diffused SERIS SE full-area Al-BSF cells demonstrate an efficiency gain of $0.4\%_{abs}$ [9].

> "An efficiency greater than 19% seems achievable using SE and Al-LBSF-type solar cells."

An 18.6% average cell efficiency was recently reported [11] for full-area Al-BSF homogeneous-emitter cells with an additional optimization of chemical rear-junction isolation, screen parameters and

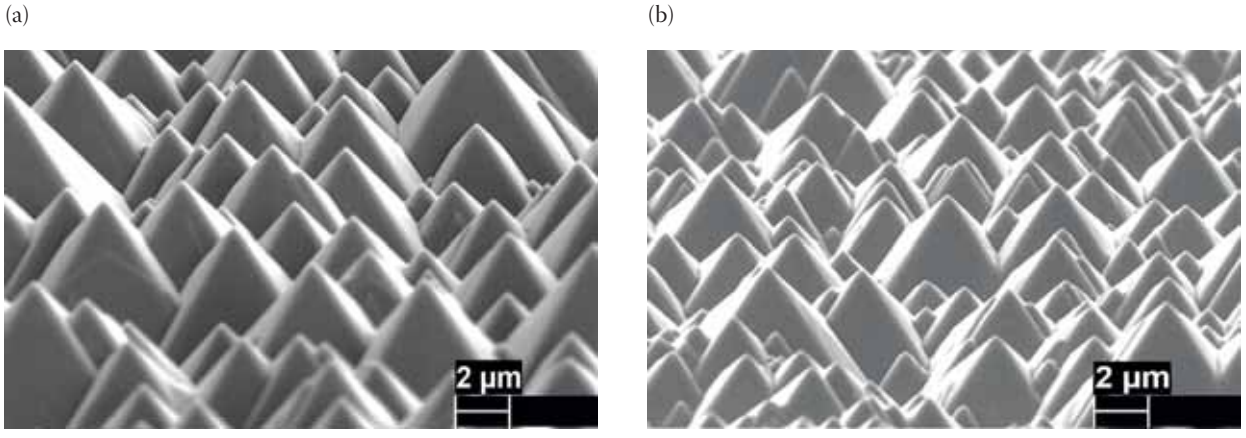

Figure 2. Scanning electron microscope (SEM) micrographs of the pyramid-textured mono-Si surface viewed at an angle of 70° (×5000 magnification): (a) textured surface (undiffused); (b) in-line-diffused surface after etch-back with the SERIS etch (R_{sq} ≈ 100Ω/sq).

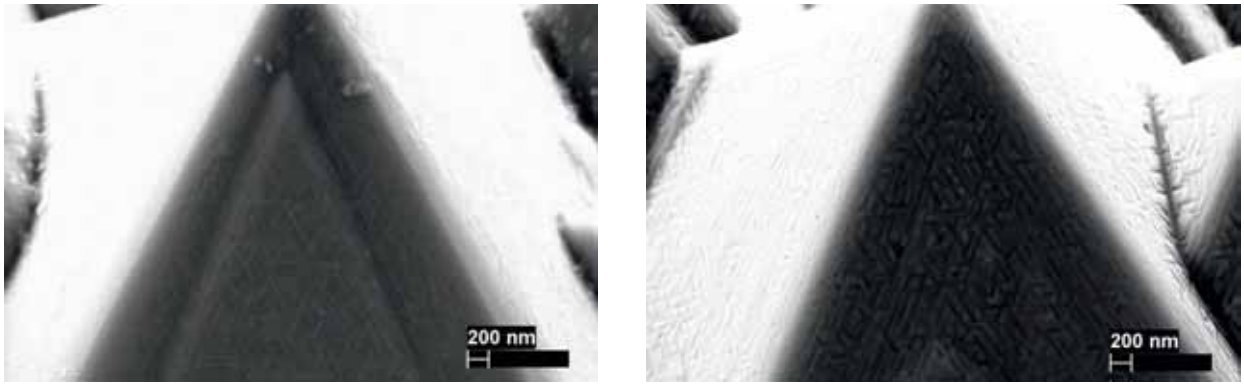

Figure 3. SEM micrographs of the in-line-diffused mono-Si surface viewed from above (×20,000 magnification): (a) after PSG removal of the 50Ω/sq diffused emitter; (b) the same surface after etch-back to R_{sq} ≈ 70Ω/sq with the SERIS etch [8].

Cells	V_{oc} [mV]	J_{sc} [mA/cm^2]	Fill factor [%]	Efficiency [%]
No etch-back	618.5	36.6	75.3	17.0
Etch-back by SERIS etch	629.6	36.7	80.2	18.6
Change (absolute)	+11.1	+0.1	+4.9	+1.6

Table 1. Summary of the average one-sun *I-V* parameters for in-line-diffused emitter mono-Si wafer solar cells without etch-back (as-diffused 70Ω/sq emitter) and with etch-back (as-diffused 40Ω/sq emitter with etch-back to 70Ω/sq).

metal co-firing processes. On the basis of this improved 'baseline' efficiency, an efficiency greater than 19% seems achievable using SE and Al-LBSF-type solar cells. To the authors' knowledge, these are the highest reported efficiencies achieved so far with in-line-diffused emitters using screen-printed contacts, which demonstrates the effectiveness of the SERIS etch.

Average values of the electrical parameters of the completed in-line-diffused solar cells (measured under standard one-Sun AM1.5G conditions) are summarized in Table 1, for both non-etch-back cells (as-diffused emitter with R_{sq} ≈ 70Ω/sq) and etch-back cells using the SERIS etch (as-diffused R_{sq} ≈ 40Ω/sq emitter and then etch-back to ~70Ω/sq). The dominant performance gain when using the SERIS etch is a result of the 11.1mV increase in V_{oc} and the 4.9% gain in fill factor, yielding an average 1.6%$_{abs}$ efficiency gain for the etch-back cells compared with the cells without etch-back.

It is assumed that the presence of sufficient residual surface contaminants obstructs the creation of ohmic contact during metallization. The removal of contaminants by the SERIS etch improves the ohmic contact, ultimately resulting in lower values of series resistance over the entire in-line-diffused emitter surface. Additionally, because of the residual surface contamination and silicon phosphide precipitates [1] with the heavily doped dead layer, cells without etch-back suffer losses in Voc and short-circuit current density (J_{sc}). The SERIS etch eliminates all these negative aspects of in-line diffusion, allowing V_{oc} and J_{sc} values to be obtained that are on a par with those of tube-diffused emitters.

Industrial application of the SERIS etch

To date, the SERIS etch has been applied in a batch process in the laboratory at SERIS. However, the authors are confident that the SERIS etch can be easily transferred to industrial in-line wet-chemistry tools. The SERIS etch process is normally performed at 80°C, and there is no significant evaporation of the chemical components, which would affect the concentration of the solution. Moreover, no hazardous HF and HNO_3 solutions are used. As a result, the SERIS etch is compatible with existing alkaline-texturing tools, which are already designed for processing with ~80°C alkali solutions. The only required modification envisaged is a shortening of the process tool because of the shorter process time (as per requirements) of the SERIS etch than that required in alkaline texturing.

> "The SERIS etch has already demonstrated world-leading solar cell efficiencies for in-line-diffused solar cells."

Conclusion

In this paper it has been shown that the low-cost HF-free non-acidic SERIS etch has unique properties that make it an ideal process for the cost-effective manufacture of high-efficiency Si wafer solar cells. The new etch technique offers uniform, conformal, deep etch-backs that also serve to remove the detrimental debris typically present after in-line diffusion. Since the SERIS etch is compatible with existing in-line industrial tools for alkaline texturing, its transfer to the PV industry is expected to be relatively straightforward. The SERIS etch has already demonstrated world-leading solar cell efficiencies for in-line-diffused solar cells, with efficiencies of up to 18.7% for standard homogeneous-emitter Al-BSF solar cells, and is also compatible with SE and LBSF solar cells.

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Bram Hoex is a director and a group Leader in SERIS' Silicon PV Cluster. He holds a Ph.D. in applied physics from Eindhoven University of Technology and has extensive experience in the areas of processing and advanced characterization of high-efficiency silicon wafer solar cells. In 2008 Dr. Hoex won the SolarWorld Junior Einstein Award and the Leverhulme Technology Transfer Award for his work in the area of high-efficiency silicon wafer solar cells.

Matt Boreland is a director of SERIS' Silicon PV Cluster. He has a Ph.D. in photovoltaics from UNSW and 20 years' solar experience in Australia (UNSW, Sydney University), Japan (TTI), the UK (Loughborough University) and Singapore (UNSWASIA, NUS). Dr. Boreland's research includes applied device and process technologies for silicon photovoltaics.

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