Cu-plated electrodes with laser contact opening on n-type crystalline silicon solar cells

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ABSTRACT

This paper presents the fabrication of front-junction n-type silicon solar cells with Cu-plated electrodes, using laser contact opening and forward-bias plating. The cells feature a back-surface field formed by a phosphorus implant, and a diffused boron emitter with aluminium oxide passivation. Laser ablation of the front-side dielectric layers is followed by a metallization based on Ni/Cu forward-bias plating, while sintered metal paste is used for the rear electrode. The results show improved line conductivity and contact resistivity for the plated electrode, leading to higher solar cell efficiency than for cells made with conventional Ag/Al paste. On 6" n-type Czochralski wafers, cell efficiencies of up to 21.3% have been demonstrated, with an open-circuit voltage of 654mV, a short-circuit current of 40.8mA/cm^2 and a fill factor of 79.8%.

Introduction

It is well recognized that n-type crystalline silicon solar cells offer higher efficiency potential than p-type cells, as n-type wafers are: 1) more tolerant of common metallic contaminations, such as iron [1]; 2) provide higher minority-carrier lifetime; and 3) do not suffer from light-induced degradation (LID), which significantly impacts the performance of p-type cells created from boron-doped Czochralski (Cz) wafers [2–4].

N-type silicon solar cells are often made with a bifacial structure, which utilizes the light incident on the rear surface to produce even more power. Motech has developed n-type bifacial cells based on a passivated emitter, rear totally diffused (PERT) structure, and has previously reported efficiencies higher than 20.6% for n-PERT cells made with screen-printed electrodes on both sides of the cell [5]. A performance ratio gain of 20% has also been demonstrated for bifacial modules using n-PERT cells in outdoor tests [5].

The conventional metallization approach, however, is relatively expensive for bifacial cells: compared with p-type cells, the usage of Ag pastes on bifacial n-type cells is roughly double. A low-cost alternative to Ag paste metallization, such as the Cu plating method studied in this work, is therefore particularly important for n-type cells. In addition to the material cost savings, the electrical performance of the solar cell also benefits from Cu plating, because the bulk conductivity of plated Cu is higher than that of Ag pastes, and the contact with Si of plated Ni/Cu is superior to that of sintered Ag. The Cu fingers defined by laser contact opening (LCO) can also be made thinner than screen-printed Ag fingers, further reducing the shading losses.

Cu-plating metallization has been used for the front electrodes of p-type cells with an Al back-surface field (BSF) and for passivated emitter and rear cells (PERCs) [6], as well as for the front electrodes of rear emitter n-PERT cells [7]. Those electrodes on the n$^+$ surface of the cells were created by the light-induced plating (LIP) method. However, LIP is not suitable for plating the boron-doped p$^+$ surface; instead, the forward-bias plating (FBP) method [8] is used, whereby the cell is placed under forward bias to enable the plating process. FBP is used to create the Ni seed layer on the p$^+$ surface of the cells, as well as the Cu conductor on top of Ni. The deposition rate is easily controlled by the applied current.

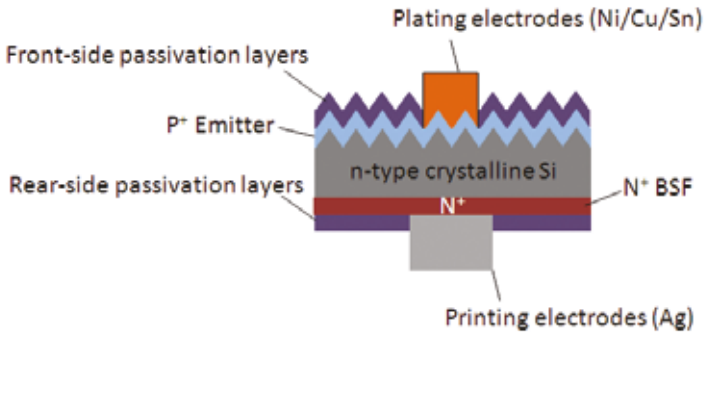

Figure 1. Schematic cross section of an n-type silicon solar cell.

Solar cell structure and process flow

A schematic diagram of the solar cell structure is shown in Fig. 1. As the starting material, 6" n-type Cz wafers were used, with a thickness of ~170µm and a resistivity of 3–5Ω·cm. The front surface was textured with random pyramids to reduce optical reflection. The p$^+$ boron emitter was established near the front surface, and homogeneous phosphorus doping on the rear side formed the BSF. Amorphous SiN_x thin film was deposited on the rear to passivate the n$^+$ doped surface, while a stack of Al_2O_3/SiN_x was deposited on the front

to passivate the boron emitter and to serve as an anti-reflection coating (ARC) at the same time. Conventional screen-printed/sintered Ag paste was used for the rear-side electrode. A Ni/Cu/Sn stack, plated on the Si surface exposed by laser ablation of the ARC, was used for the front-side electrode.

The process flow for the front-junction n-PERT cells is shown in Fig. 2. Standard alkaline etching was used to create the random pyramid texture, followed by BBr_3 diffusion for the emitter, with a sheet resistance of 75±5Ω/sq. After the removal of borosilicate glass, the wafers were subjected to a phosphorus implant and annealing process to form an n^+ BSF on the rear side. An Al_2O_3 layer for the emitter passivation was deposited using atomic layer deposition (ALD) equipment. A SiN_x coating was deposited by plasma-enhanced chemical vapour deposition (PECVD) on the front side as the ARC, and also on the rear side as a capping layer.

Commercially available Ag paste for the n^+ surface was used to create the rear-side electrode by printing and sintering. The thermal budget also helped improve the passivation. The ARC was then ablated using a 532nm green nanosecond laser to define the front-electrode pattern. Ni and Cu were then deposited by FBP, followed by Sn electroplating. Finally, a rapid thermal annealing was performed in a belt furnace to form a nickel silicide layer in order to improve the front-contact resistance.

"Laser ablation of the ARC for front-side contact opening is one of the key processes for Cu-plated n-PERT cells."

Figure 2. Process flow for front-junction n-PERT cells.

Laser ablation process

Laser ablation of the ARC for front-side contact opening is one of the key processes for Cu-plated n-PERT cells. First, it needs to completely remove the ARC in the targeted area, so that Ni can be directly plated onto Si. Second, to reduce the plated finger width and to maintain good finger conductance, the laser opening itself has to be narrow and uniform. Third, the quality of the boron emitter should be maintained after its modification by laser. Because a 532nm nanosecond laser source was used, the thermal effect of the ablation was expected to change both the emitter doping profile and the silicon surface morphology.

Various combinations of laser parameters – including peak power, scan speed, light focus and pulse frequency – were tested in the ablation of the front-side dielectric layers. Fig. 3 shows the scanning electron microscope (SEM) images of the laser contact opening in the experiments.

A good ablation process should lead to a clearly defined removal of the dielectric layer, and minimum laser damage to the Si surface. Fig. 3(a) shows the ablation with too little laser energy: the textured surface was only slightly modified, but the SiN_x film was not fully removed, as indicated by the nitrogen signal in the energy dispersive X-ray spectroscopy (EDS) for the ablated area. In contrast, the high energy case, shown in Fig. 3(c), indicates a seriously damaged surface, with melted Si splashed over the region of the laser opening. Fig. 3(b) shows an example of appropriate laser energy, with a thin line and uniform width: an average width of 15.7µm and uniformity of 1.5% (by measuring widths at different positions across the wafer) were achieved. Complete removal of the dielectric layers was confirmed in this case by the 100% Si signal in the EDS for the ablated area.

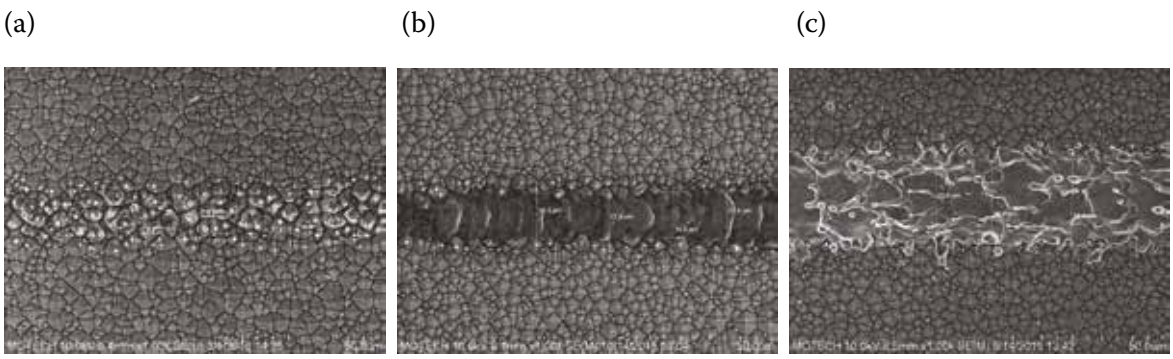

Figure 3. SEM images of front-side contact opening using different laser energies: (a) low; (b) medium; (c) high.

As regards the emitter profile, samples suitable for electrochemical capacitance–voltage (ECV) measurement were created; the results are shown in Fig. 4. The sample before the LCO process indicated a shallow emitter with a peak concentration of ~9E+19cm^{-3}; the sheet resistance was 75Ω/sq. After LCO, the emitter profile was changed in such a way that the surface concentration was reduced to less than 2E+19cm^{-3}, and the junction moved deeper, to ~0.7µm; the sheet resistance became 95Ω/sq. Although such a low surface concentration falls outside the range suitable for contact by sintered Ag paste, it is still practical for a nickel silicide contact. The deeper profile could help reduce carrier recombination in the metal contact region, and prevent a vertical shunting path when nickel silicide is formed during the annealing process.

Front-side metallization

After LCO is completed, the cell is placed in a plating tank with a bias applied via the rear-side Ag electrode in order to start the FBP process; Fig. 5 shows the SEM images of the cell at different stages of the metallization process. The metal deposition of FBP is isotropic, which means that the finger width is roughly the sum of the laser opening width and twice the metal thickness.

Because of Motech's cell design, it was decided not to push the line width to its lower limit, and so a LCO width of 20µm was used instead, as shown in Fig. 5(a). Fig. 5(b) shows the deposition of a 1µm Ni layer by FBP; the finger width was about 22µm. Subsequent Cu FBP processing increased the finger width to 46µm, with a Cu thickness of 12µm, as shown in Fig. 5(c) and (d). Finally a 1µm Sn protection layer was plated; the completed metallization is illustrated in Fig. 5(e).

A GPsolar 4-TEST four-point probe tool was used to perform line resistance R_{line} measurements, yielding the resistance per unit length of the fingers. A comparison of samples created using Ag/Al paste and Cu plating is given in Table 1. The average value of R_{line} readings at five different positions across the wafer was 0.38Ω/cm for Ag/Al paste, and 0.25Ω/cm for Cu plating. By multiplying the respective cross-sectional area of the fingers, the line resistivity of Ag/Al was estimated to be 2.7µΩ·cm, and that of a Cu finger to be 1.9µΩ·cm. This result highlights the advantages of using plated Cu fingers: with a higher finger conductivity, it is possible to implement thinner lines, thus reducing the shading on the front side of the cell.

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Emitter experiment

In the case of solar cells with screen-printed metallization, the emitter profile is significantly constrained by the contact capability of the sintered Ag or Ag/Al paste. The nickel silicide contact with the Si is expected to be superior, with a contact resistivity below 1mΩ·cm^2 at a doping level of 1E+19cm^{-3} [9]. This provides a lot of room for emitter optimization for higher cell efficiency, even though the emitter is modified in the contact area if a laser is used. In the work reported here, several emitter profiles were tested: a shallow emitter (denoted E1) with a low surface concentration (2E+19cm^{-3}), and several others

(E2–E5) with increasing junction depth and/or concentration. The results of *I–V* measurements are shown in Fig. 6.

The carrier recombination will be enhanced under heavier doping conditions, resulting in a downtrend in short-circuit current (J_{sc}). On the other hand, a heavy doping profile reduces the emitter sheet resistance and hence the series resistance. The dependence of open-circuit voltage (V_{oc}) on doping is generally characterized by an interplay between the recombination in the emitter and the field effect of the emitter. The results show that, except for the heaviest doping condition (E5), the efficiency is consistently higher than 20.6%, with an expected trade-off between fill factor (FF) and J_{sc}. The front-metal patterns were kept the same in all these experiments, and so improved electrode design is certainly a possibility for further increasing cell efficiency.

Contact resistivity was measured by the transfer length method using the GPsolar 4-TEST tool. The resistivity was found to be around 1mΩ.cm^2, even for the lowest doping condition; it should be possible to improve this by further optimizations of the Ni deposition and annealing for silicide formation.

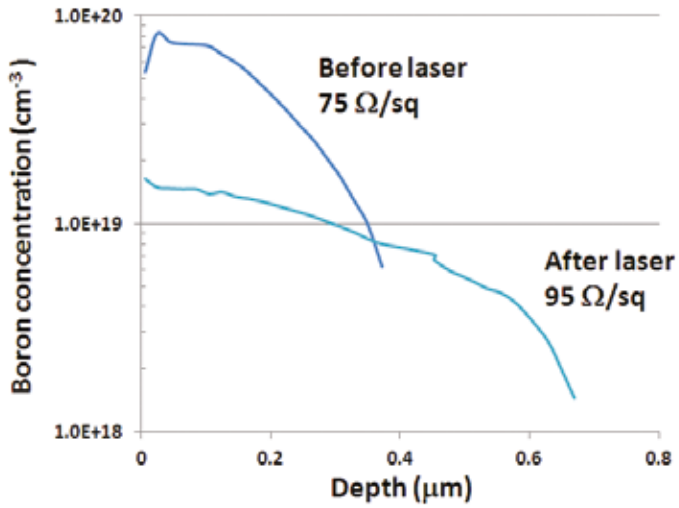

Figure 4. Emitter profile before and after the LCO process.

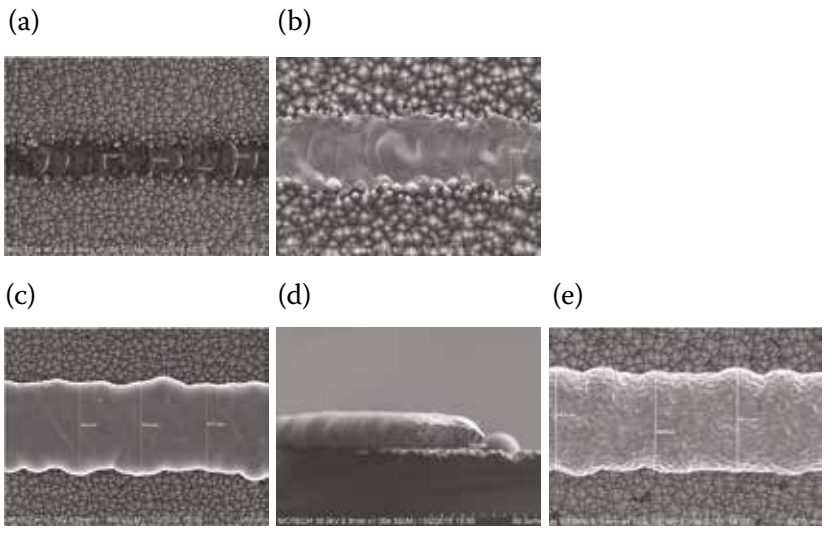

Figure 5. SEM analysis of laser opening and front-side metallization: (a) after green nanosecond LCO; (b) after Ni plating; (c) after Cu plating; (d) after Cu plating, side view; (e) after Sn plating.

Plated vs. printed

One concern about plated electrodes is that the diffusion of Cu into the active area of the solar cell could become a major source of recombination. A Ni layer with proper silicidation can be used as a diffusion barrier to Cu, but the series resistance may increase if the Ni is too thick, because of its lower conductivity. The method in Hernández, J. et al. [10] was followed, and Cu diffusion in the solar cells was checked by *I–V* and Suns-V_{oc} measurements before and after a thermal stress of 500°C for one minute. No change in either V_{oc} or pseudo-fill factor (pFF) was found after the thermal stress, indicating that there was no Cu diffusion into the p-n junction or into the bulk of the wafer.

Compared with a conventional printed Ag/Al finger, the plated Cu finger exhibits a narrow line width, a good aspect ratio, well-defined finger edges, a smooth surface and a solid bulk (Fig. 7). These characteristics indicate that plated Cu is a better conductor for Si solar cells. The fine-line capability enables a more optimal combination of the electrode pattern and the emitter profile. Furthermore, the incident light could be increased as a result of the reflection from the smooth finger edges.

It was possible to improve the efficiency of the plated n-PERT cells to over 21%; the *I–V* curve of one of the best cells is shown in Fig. 8, with a V_{oc} of 654mV, J_{sc} of 40.8mA/cm^2 and FF of 79.8%.

A comparison of the performance of n-PERT solar cells with different metallizations is given in Table 2. The Cu-plated n-PERT cells showed an efficiency improvement of 0.2%$_{abs.}$ over the printed cells. One apparent benefit of Cu fingers was the improved current density J_{sc}, which resulted mainly from the thinner line width. The V_{oc} of n-PERT cells made using the Ag/Al paste firing process usually degrades

	R_{line} [Ω/cm]						Resistivity
	Position 1	Position 2	Position 3	Position 4	Position 5	Average	[μΩ·cm]
Ag/Al paste	0.389	0.409	0.398	0.378	0.331	0.381	~2.7
Cu plating	0.253	0.255	0.259	0.258	0.223	0.250	~1.9

Table 1. Line resistance data and resistivity for sintered Ag/Al fingers and plated Cu fingers.

significantly from the implied V_{oc} value measured before metallization. Even though no Cu diffusion was observed in the plated cells, their average V_{oc} was slightly less than that of the printed cells. It is suspected that the laser used in this study introduced damage to the contact area, and that the silicidation process needs to be improved. With regard to the FF, a further increase is expected when the electrode pattern design is optimized for specific emitter profiles.

> "The Cu-plated n-PERT cells showed an efficiency improvement of 0.2%$_{abs.}$ over the printed cells."

Conclusion

A Ni/Cu/Sn metallization has been developed for the front-side electrode of an n-PERT cell, using forward-bias plating and laser contact opening. The laser parameters were tuned to completely ablate the SiN_x ARC, creating a uniform line opening with a width of less than 16µm. The FBP produced thin metal lines exhibiting excellent conductivity. Good contact resistance was obtained for a peak doping concentration below 2E+19cm^{-3}. Even though the surface morphology and the emitter profile were modified by the 532nm nanosecond laser during contact opening, the efficiency of the Cu-plated cells demonstrated a 0.2%$_{abs.}$ gain over conventional printed or sintered cells. The best efficiency achieved for 6" plated cells was 21.3%.

Many aspects of this metallization scheme can be improved. Moving to a UV laser source will significantly reduce the thermal effect of the laser and minimize damage to the silicon surface. Optimization of the silicidation process will enhance adhesion and the electrical contact between Si and metal. The vast range of emitter profiles that are possible by using a nickel silicide contact should yield a high-efficiency cell design that optimally combines the emitter, the electrode pattern, and the very fine metal lines provided by Cu plating.

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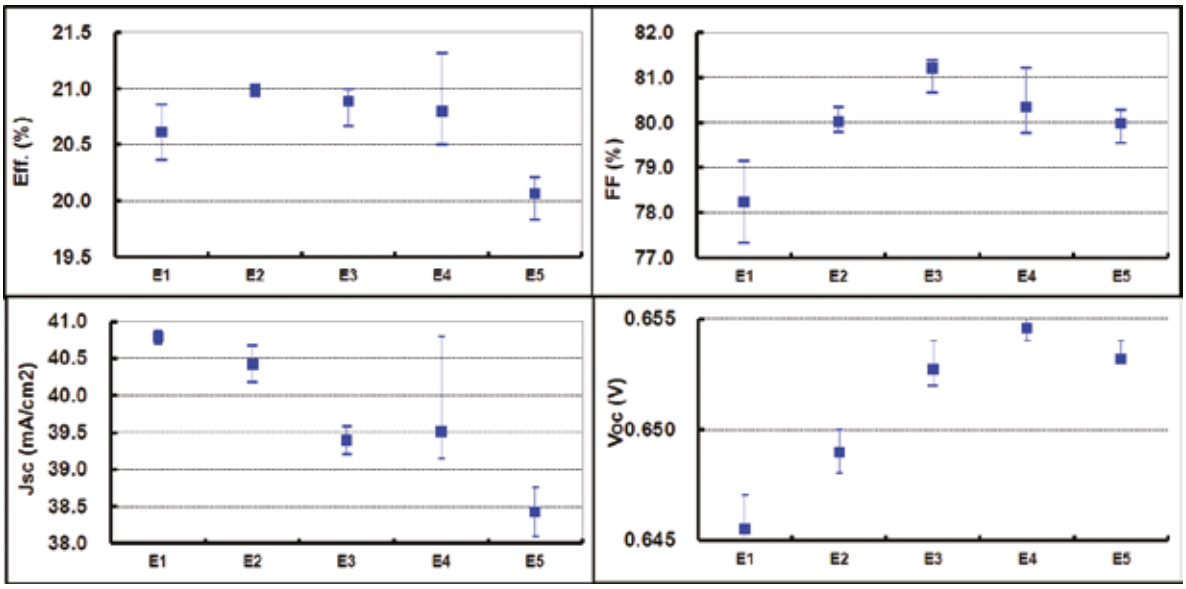

Figure 6. Cell performance for different emitter profiles.

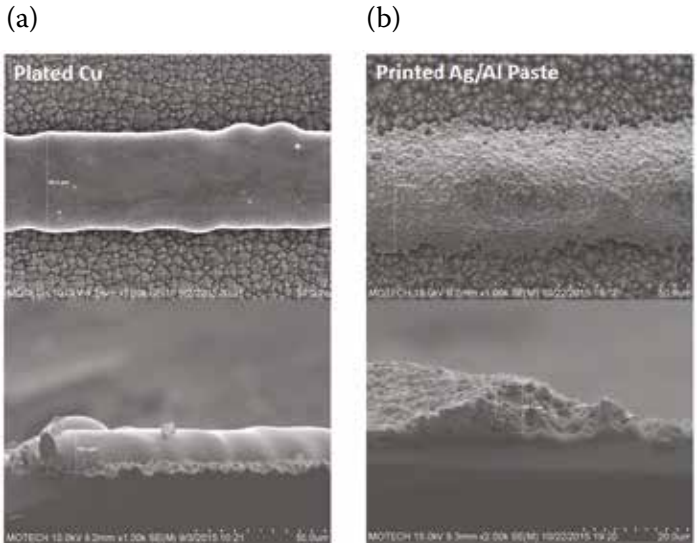

Figure 7. SEM images of (a) a plated Cu finger, and (b) a printed Ag/Al finger.

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About the Authors

Dr. Kuang-Chieh Lai received his Ph.D. in electrical engineering in 2011 from National Cheng Kung University. In 2007 he worked at NexPower Technology Corporation on developing the technology of a-Si thin-film solar cells. He joined Motech in 2011, where is involved in R&D of n-type c-Si solar cell technology.

Dr. Yueh-Lin Lee received his degree in photonics technologies and his Ph.D. from National Tsing Hua University in 2014. He then worked as a principal R&D engineer at Motech, focusing on advanced technologies of electroless plating and electroplating, and high-efficiency silicon solar cells.

Dr. Ming-Shiou Lin received his degree in materials science and engineering in 2005, followed by his Ph.D. from National Chung Hsing University in 2011, with a thesis on ZnO nanorods applied to light-emitting diodes. Since 2014 he has been working in the advanced technology section of Motech, where he is in charge of R&D of high-efficiency silicon solar cells.

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Dr. Chi-Chun Li received his Ph.D. in electrical engineering from Princeton University in 1999. From 2000 to 2008 he worked on telecommunication management systems at Alcatel-Lucent, before joining Motech in 2009 to lead the development of new solar cell designs

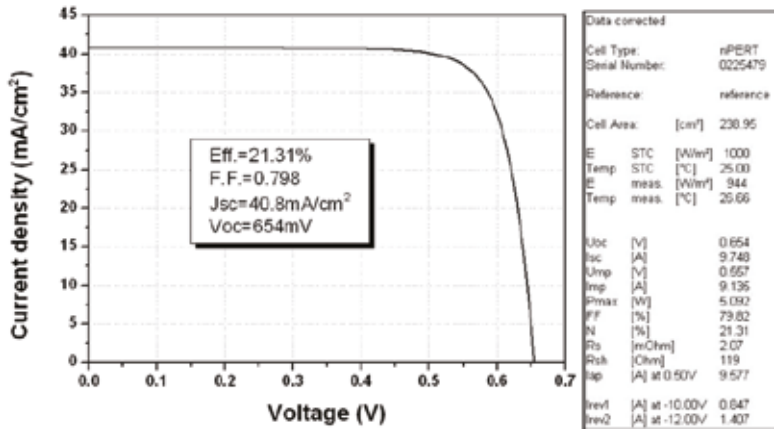

Figure 8. *I–V* curve of a Cu-plated n-PERT solar cell.

Metallization	Eff. [%]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]
Ag/Al paste	20.8	654	39.8	79.8
Ni/Cu/Sn	21.0	650	40.4	80.0

Table 2. Solar cell performance for printed and plated electrodes.

and processes. He is currently a senior manager of the Advanced Technology Development Department.

Kirin Wang is the RD senior director at Motech, and graduated from the Institute of Material Science and Engineering of National Tsing Hua University in 1991. He joined Motech in 2010 and works on advanced solar cell development (P-PERC, N-PERT, HJT, back contact cell and Cu plating), and on production process development, including double printing, screen design, advanced ingot growth and diamond wire slicing. Before joining Motech he gained 19 years' experience in technology development and mass production in the semiconductor industry.

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