Scaling single-junction a-Si thin-film photovoltaic technology to the next level

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ABSTRACT

The recent photovoltaic industry shakeout which started around Q3 2008 has faced the overcapacity, credit crunch, and economic crisis that significantly declined the average selling price by 50–65%, including the price of thin-film photovoltaic modules. The changing business environment has put significant pressure on all PV manufacturing technologies but more candidly on amorphous silicon thin-film single-junction module manufacturers to advance and scale up the device efficiency and aggressively drive cost reduction. This paper outlines the technical approach taken at Moser Baer Photovoltaic Technologies India Limited (PVTIL), including process optimization and device management strategies, to enhance the efficiency (total area) of the thin-film single-junction amorphous silicon module as manufactured using Applied Materials' SunFab line.

Introduction

Moser Baer Photovoltaic Technology India Limited (PVTIL) was formed in February 2007 with the main objective to become one of the leading thin-film module manufacturers in India with the capacity to compete in global markets. The production plant was constructed with the initial annual manufacturing capacity of 40MW using the Applied Materials Gen 8.5 SunFab Line applying a stable efficiency of ~6%. The reported efficiency is determined after applying the total module/glass area to the calculation. The Factory Acceptance Test (FAT) of the single-junction amorphous silicon (a-Si) thin-film plant was completed in December 2008. The line is capable of producing modules in three different sizes: 1.43m^2, 2.86m^2, and 5.72m^2, respectively. These modules find various applications ranging from rooftop installations to larger solar farms.

For the solar industry, 2009 was a difficult year for a variety of reasons. Financing dried up completely in all major markets. Weakening economies and job outlook increased the liquidity premium, while bankability issues coupled with an imbalance in module supply-to-demand ratio significantly decreased the module price by more than 50–65%. This has placed a severe pressure on PV module manufacturers to aggressively drive their technology improvement roadmap to lower the cost of modules.

At PVTIL, we have taken a systematic and innovative engineering approach to scale up the single-junction a-Si process

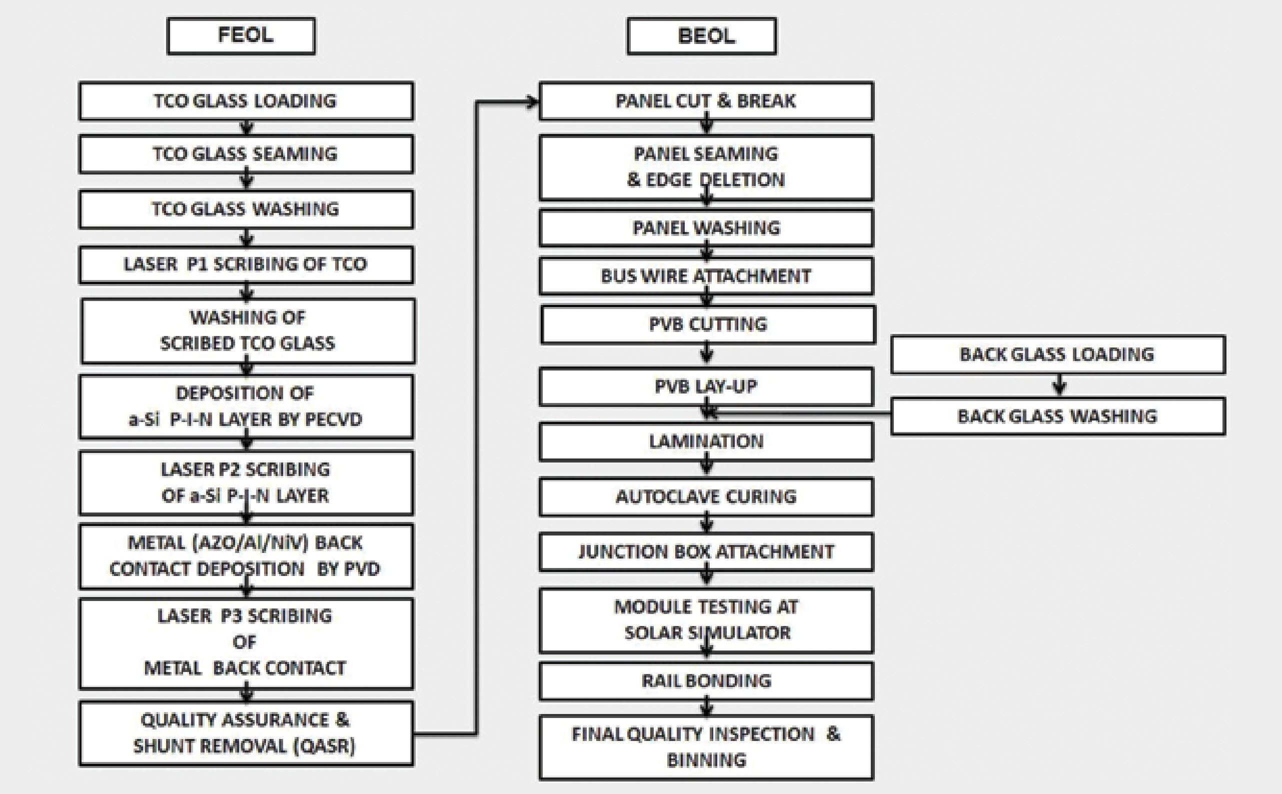


Figure 1. Flow chart of PVTIL single-junction 50MW production line, comprising both the FEOL and BEOL technologies and processes.

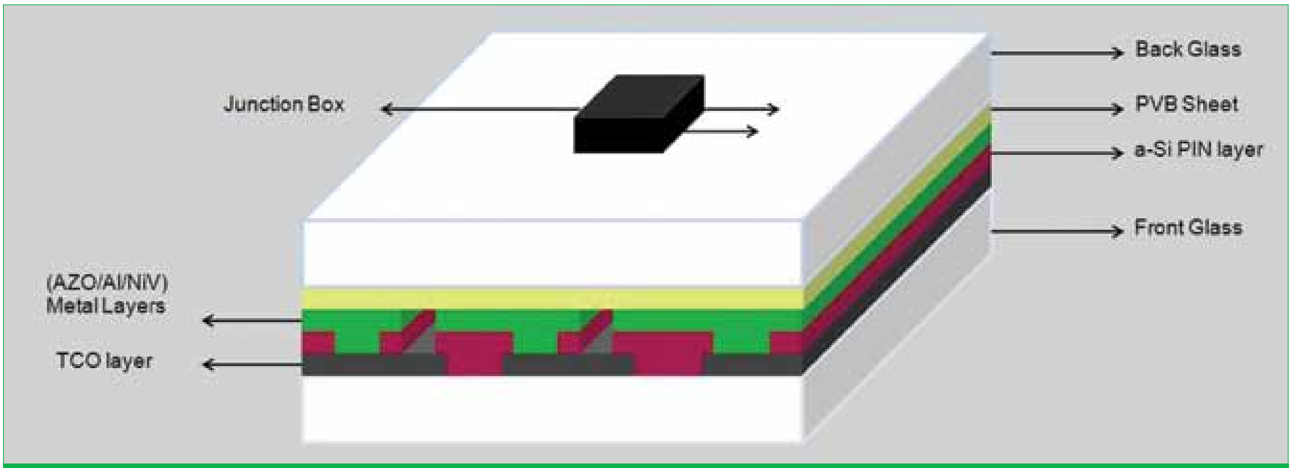


Figure 2. Cross-sectional view of the single-junction a-Si p-i-n module.

and technology from a stable efficiency of 6% to ~7%. The enhanced device and module performance has been derived by following a four-pronged strategy: better photon management/light absorption; improvement in the extraction of charge carriers; enhancement of device stability; and achievement of a stabilized daily production with consistent process control.

Enhancement of stable efficiency to ~7% and improvements in yield and equipment uptime have resulted in the readjustment of the annual manufacturing capacity of the production line to >50MW. With the scaling of a-Si single-junction technology, the old product portfolio such as MBTF85, MBTF170 and MBTF340 are now being replaced by MBTF100, MBTF200 and MBTF400, respectively, with higher wattage per module. The modules are frameless with glass-PVB-glass encapsulation and are available with and without bonded rail options.

Module production line

A general flow diagram of the fabrication steps of the production line is shown in Fig. 1. The line is divided into front end of line (FEOL) where front glass is processed as the panel and back end of line (BEOL) where a front glass-PVB-back glass encapsulant is integrated into a module. The first step of the module manufacturing involves loading of transparent conducting oxide (TCO) glass substrate in FEOL. TCO glass is manually edge-seamed before the washing and drying step. The building of the cells starts with Laser P1 scribing of TCO, which results in the formation of 216 cell isolations with ~1cm width over the glass length of 2.6m.

Next, the washing step is performed before depositing the new PVTIL proprietary a-Si p-i-n device (Fig. 2) using AMAT's Gen 8.5 plasma-enhanced chemical vapour deposition (PECVD) cluster tools. A second laser P2 is then scribed in the a-Si layer in parallel to the first scribe in the TCO, leaving a P1-P2 gap of 150–200µm to allow a monolithic interconnection of the solar cells later on in the process. A three-layer (AZO/Al/NiV) rear contact is deposited using the sputtering tool on top of the p-i-n device. Following the sputter deposition, a third laser scribe (P3) is performed. The P2-P3 scribe width is kept at 150–200µm with the P1-P2-P3 gap fixed from the 300-400µm range, respectively. In addition, an edge isolation line is scribed using P3 at a distance of ~15mm from the glass edge which defines the active area of the cell/module. The final FEOL step involves removing shunts by reverse biasing the cells and burning/curing the defects. The shunt busting is an important step to achieve P_{max} (peak module power) performance and consistency from module to module processing. This completes the processing of the solar panel.

The full-size (5.72m^2) panel is further processed through the back end of the line for manufacturing a complete integrated module, where based on laser design, the panel can be cut into quarter size (1.43m^2), half size (2.86m^2), or processed as a full-size (5.72m^2) glass. After the cut and break step from the BEOL, the panel is further processed through auto-seaming equipment for ~12mm edge deletion where all excess films are removed to achieve edge isolation on all four sides. Next, the panel goes through the final washing step. Thereafter, the side bus lines are soldered at the two end segments (cells) of the panel, at which point the cross bus bars are attached to the side bus lines which run through the centre of the module (Fig. 3).

Before the lamination step, the module is integrated in a layup room where the

Figure 3. Back-side view of the quarter-size MBTF100 module with bonded back rail.

front panel (glass), polyvinyl butyral (PVB) foil and back glass (with hole for attaching junction box) are sandwiched. The module then passes through a laminator where a combination of heated nip rollers removes the air and seals the edges. At the exit of the laminator conveyer, the modules are collected and stacked together on a rack for batch processing through the autoclave where they are subjected to an anneal/pressure cycle to remove the residual air and completely cure the PVB. Finally, a junction box is attached to the cross bus wire and sealed on top of the hole of the back glass and is filled with the pottant to achieve a complete module integrity. The fully processed module is flashed in a solar simulator (AM 1.5 Global intensity) with an NREL-calibrated c-Si reference cell covered with KG1 filter.

“Although the single-junction a-Si solar cell has limited scope in terms of efficiency improvement, it has multiple advantages.”

Strategies and new process development experiments

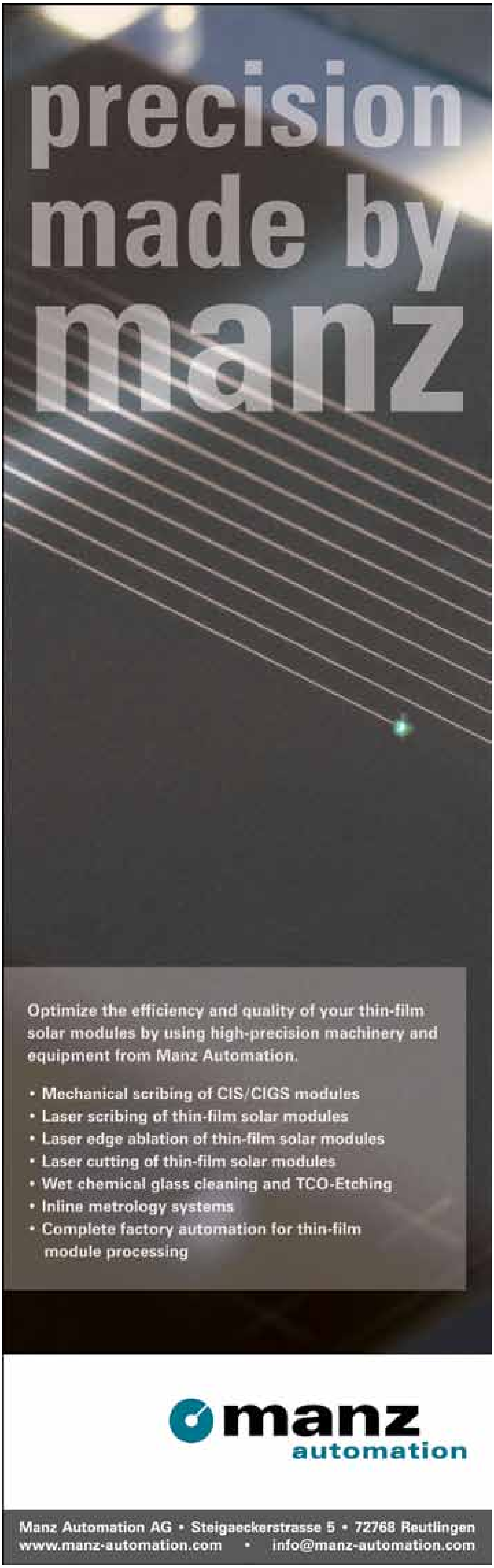
A cross-sectional view of the a-Si single-junction p-i-n device made with various layers is shown in Fig. 2. A technology transfer at an initial and stable efficiency of 7.18% and 6%, respectively, was made from AMAT to PVTIL. Although the single-junction a-Si solar cell has limited scope in terms of efficiency improvement, it has multiple advantages such as 1) it is almost independent of wafer price fluctuation; 2) it can be processed in larger glass sizes ($5.72m^2$), resulting in higher wattage modules even with low conversion efficiency; and 3) the technology can be upgraded to tandem junction (TJ). However, upgrading to TJ technology requires substantial capital investment. Therefore, we decided to look for the device and material engineering of the existing a-Si single-junction technology to improve the device efficiency from a stable value of 6% to the next level.

In order to form strategies for the enhancement of device efficiency, one must understand the basic limitations of the a-Si single-junction p-i-n diodes, which are established from thermodynamical considerations on radiative recombination and semi-empirical considerations on the classical diode equations. An upper limit for the short circuit current density Jsc can be computed by considering the normalized AM 1.5 spectrum (IEC 904-3) and assuming that all photons with $h\nu > E_g$ (h is Planck’s constant, $\nu = c/\lambda$ where c is the speed of light, λ is the wavelength, and E_g is the energy gap of the semiconductor material considered) are absorbed and converted into electron-hole pairs that can, in principle, be collected at short circuit conditions. According to this equation, for a-Si solar cells with the E_g of 1.75eV, the corresponding limitations [1–3] to J_{sc} is $\sim 21.1mA/cm^2$. For the single-junction a-Si solar cell technology that was transferred to PVTIL at a typical stable efficiency of 6%, the measured average J_{sc} was about $\approx 12.23mA/cm^2$. In order to achieve the major efficiency gain, we looked into the CVD and PVD process development and optimization strategies to increase the short circuit current density through better light trapping and absorption.

We also looked for improving both V_{oc} and FF by reducing the recombination losses in the I-layer, achieving low series resistance and high isolation resistance in between the cells, and improving the extraction of charge carriers with reduced recombination losses at various device layer interfaces. Fig. 4 describes the four-pronged strategy for device performance management.

Results and discussion

As a first step towards increasing the module efficiency, we investigated and developed the new CVD process regimes and deposition conditions which resulted in a much better film uniformity across the entire $5.72m^2$ area of the module. A detailed design of experiment (DOE) around the key deposition parameters



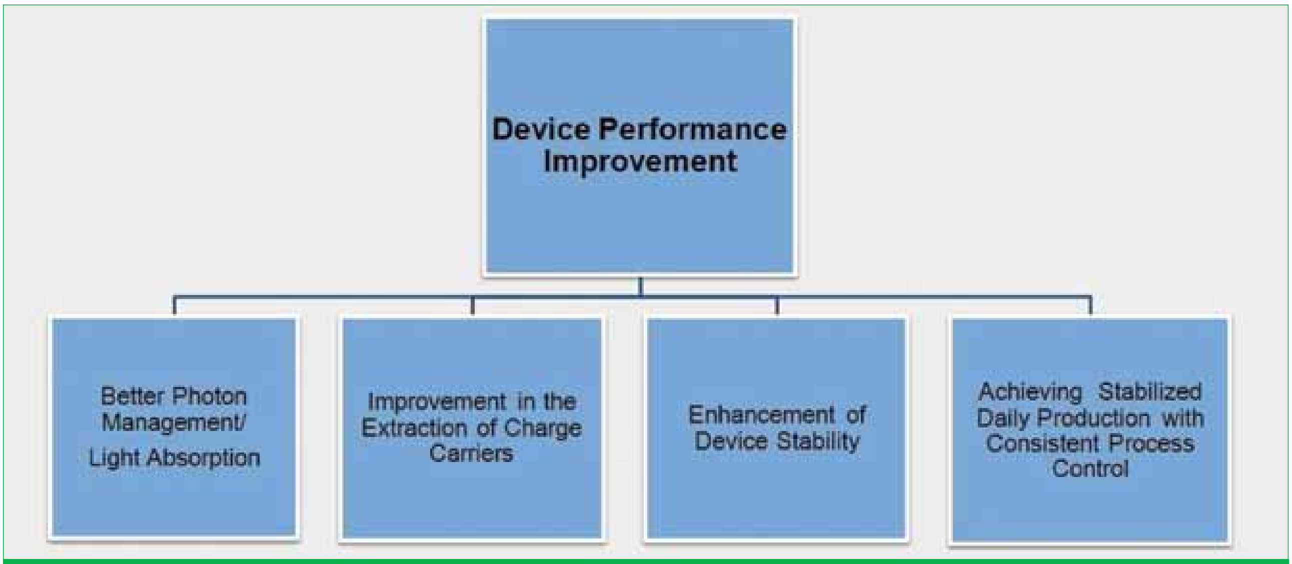


Figure 4. Description of the four-pronged strategy for device performance management.

such as gas flow ratio, power, pressure and susceptor to diffuser plate spacing conditions for all the p, i and n layers were conducted. The new optimized CVD process improved film uniformity to the ≤10% range over the entire panel area for all amorphous layers. Fig. 5 shows a typical a-Si intrinsic (i) layer thickness mapping. Good film uniformity of all deposited layers of the solar cell structure is essential to achieve a consistent and much improved module efficiency both within the entire substrate and from module to module.

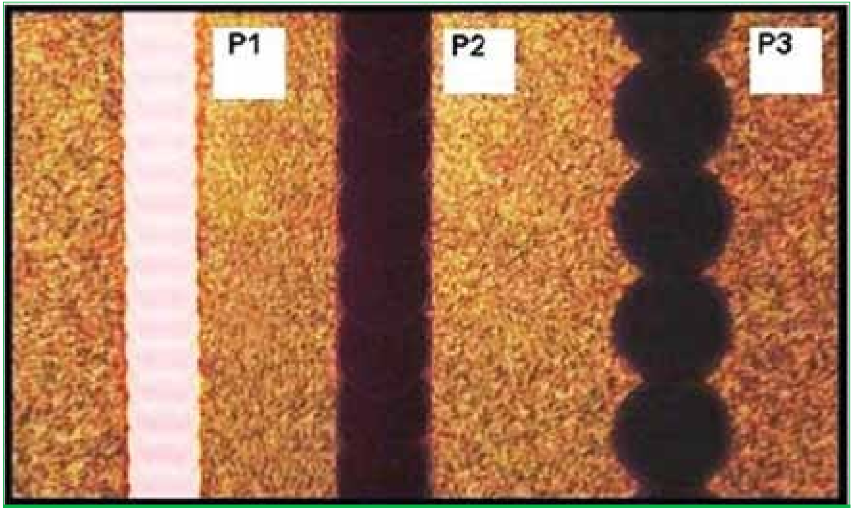


Figure 5. Typical photo by optical microscope of the laser P1-P2-P3 scribe used for panel fabrication.

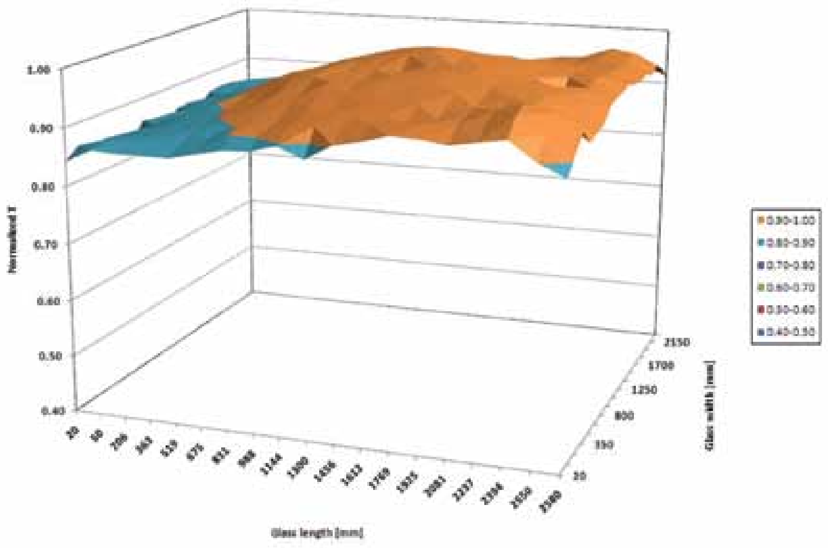


Figure 6. Typical thickness variation of the new proprietary PVTIL a-Si:H based i-Layer, with improved film uniformity of <10%.

Next, emphasis was placed on the optimization of all the laser P1, P2 and P3 processes and improvement of the scribe quality. This was done to optimize and achieve low series and contact resistance in the monolithic interconnection design and to reduce the active area losses. Fig. 6 shows the photo of the laser P1 - P2 - P3 scribe pattern taken from the module with optimized conditions. It is critical to achieve the right P2 scribe: an 'over and under' P2 scribe will yield high series resistance and low shunt resistance and hence will lower FF and device efficiency. For all three lasers, we optimized the beam frequency, energy and spot size conditions to achieve maximum gain in efficiency and overall gain in the device's electrical parameters such as V_{oc}, I_{sc} and FF. The laser design was also optimized to minimize the active area losses.

In order to improve the current density from the device, we further optimized the p layer energy gap (E_g), doping concentration and film thickness while maintaining the film uniformity at below 10% target variation. The optimization brought about substantial gains in J_{sc} and some improvements in V_{oc} and FF. A further optimization of the process conditions was achieved to minimize the recombination losses and absorption of charge carriers at the p/i interface.

Next, we focused on i-layer deposition conditions to achieve maximum gain in J_{sc} and V_{oc} without sacrificing the light-induced degradation (LID) factor. The new and optimized process showed a better LID factor, as verified by certification agency TÜV. In order to further enhance the light trapping and reduce recombination in the n layer and at the i/n interface, we further optimized the entire deposition conditions and film thickness. Similarly, we improved the quality and transmission of the AZO layer through development of the new process. The AZO layer has a special role in controlling the light transmission and light scattering back to the device to improve its absorption in the i layer to increase the J_{sc}. At PVTIL we have followed multiple designs of experiments to leverage and combine different process gains to develop a new PVTIL proprietary single-junction a-Si manufacturing process.

After the development of the new process, it was successfully validated for production worthiness on our manufacturing line. During the production trials on the stabilized manufacturing line, the new PVTIL process recipe has consistently demonstrated gains in module efficiency, hence establishing its performance.

Fig. 7 shows the illuminated current voltage curves (both initial and stabilized) of the quarter size modules made with the new PVTIL proprietary single-junction a-Si process. The measurements were conducted on the flash solar simulator calibrated using the NREL 2cm x 2cm reference cell covered with the KG1 filter. The illumination level was adjusted over the whole panel area with the calibrated 30cm x 30cm a-Si module to an illumination level of 1000W/m^2 and the module I/V measurement temperature was maintained at 25°C.

> "Optimization brought about substantial gains in J_{sc} and some improvements in V_{oc} and FF."

Table 1 gives a summary of the stabilized electrical data for the two types of quarter size (1.43m^2) modules produced using old BKM (Best Known Methodology) and new PVTIL Proprietary BKM process. It is clearly visible that the new PVTIL single-junction a-Si process gives much better and enhanced values of J_{sc}, V_{oc}, FF, η and P_{max}. A maximum increase in current density, J_{sc}, from 12.23 to 13.53mA/cm^2 is achieved using the new process. The observed stable efficiency and power on the 1.43m^2 module processed with the new process recipe is ~6.91% and 98.8W, respectively. The reported electrical values are factored with a light-induced degradation factor of ~15-20% to arrive at the stabilized values. For the full size module (5.72m^2), as a result of gain in area and reduction in process losses, which incur on quarter size modules, the estimated average stable efficiency and P_{max} are anticipated at ≥7% and ≥400W, respectively. The new recipe trials on full size substrate are in progress and we expect to establish the results in the first quarter of 2010.

Process Type	Module size	Initial efficiency	Stable efficiency	V_{oc} [V]	I_{sc} [A]	J_{sc} [mA/cm^2]	V_{mpp} [V]	I_{mpp} [A]	FF[%]	R_s[ohm]	P_{max} [W]
Old BKM	1.43m^2	7.19%	6.00%	91.7	1.47	12.23	70.4	1.29	63.3	7	85.8
New PVTIL Proprietary BKM Process	1.43m^2	8.28%	6.91%	93.3	1.63	13.53	72	1.37	64.7	7	98.8

Table 1. Comparison of the stabilized electrical data of 1.43m^2 modules deposited with the Old BKM and New PVTIL Proprietary BKM process.

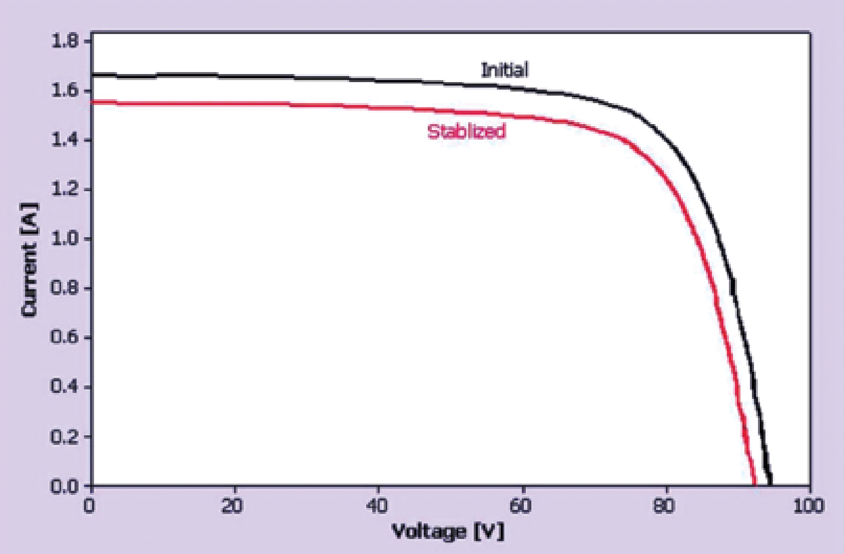


Figure 7. A typical initial & stabilized I-V curves of the ~7% efficiency quarter size MBTF100 module.

Following the modules' manufacture, application of the new proprietary process and verification at TÜV Intercert, the old module types are now being replaced with the new product types such as MBTF100, MBTF200, and MBTF400, respectively with higher wattage per module. Modules prepared with the new process steps are undergoing further evaluation and certification at TÜV Intercert.

> "The new PVTIL single-junction a-Si process gives much better and enhanced values of J_{sc}, V_{oc}, FF, η and P_{max}."

Further process development work is ongoing and new strategies are being investigated with the aim of taking the single junction a-Si technology of the $5.72m^2$ module to the ≥7.5% stable efficiency range.

Conclusions

The changing business environment has put significant pressure on all PV manufacturing technologies, but more so on amorphous silicon thin-film single-junction technology to advance and scale up the device efficiency and drive cost reduction. At PVTIL, we have developed new processes for the enhancement of stabilized efficiency of the modules. Through both device and process engineering, we have been able to increase the quarter size ($1.43m^2$) module efficiency performance from a stable 6% to ~7% with improved P_{max} ~ 99W. The superior module electrical performance has been achieved through gains in current density to $13.53mA/cm^2$ and improvements in V_{oc} and FF. For full size ($5.72m^2$) modules, the gain in active area and reduction in process losses are expected to yield a stable efficiency ≥ 7% and power ≥400W, respectively. With the enhancement of stable efficiency to ~7% and improvements in yield and equipment uptime, the annual manufacturing capacity of the production line has been readjusted to >50MW.

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The authors wish to thank the entire PVTIL team for their dedication and drive in establishing the successful operation of the plant. We are especially thankful to **Dr. Rajiv Arya**, CEO MBPV and **Mr. V. C. Agerwal**, COO MBPV Operations for their support. Finally, the technical support from the local AMAT technical team in maintaining the production line at our plant is greatly appreciated.

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Dr. Mohan Bhan is an industry veteran and brings with him over 20 years' experience from both the solar and semiconductor industries. Dr. Bhan is currently working as vice president of engineering at Moser Baer Photovoltaic India Ltd. and is managing Applied Materials' 40MW Sun Fab turnkey line. He has expertise at the intersection of technology, marketing, business and operations. Before joining Moser Baer, he worked at Applied Materials for more than 13 years in various technical, marketing and business management positions.

Dr. Rahul Kapil has more than 12 years of experience in the field of process engineering, new product development and R&D. He has a Ph.D. degree from the Indian Institute of Technology, Delhi and has extensive experience in thin-film processing and material deposition. Dr. Kapil has worked on a variety of products and technologies including a-Si thin-film solar cells, plasma display panels and blank optical Media (Blu-ray). He has published 16 research papers and filed two patents.

Vineet Jain is general manager of operations at Moser Baer India and is responsible for planning manufacturing operations and ensuring smooth functioning of the plant. His role is to ensure synchronization of production lines by line balancing and de-bottlenecking of key processes.

Dr. Sudheer Kumar is general manager of the PV solutions group at Moser Baer. He has over 16 years of experience in the fields of strategic project conceptualization and execution, value engineering, R&D, product development and management, contract management for technology transfer and material sourcing, among others. He has extensive experience in thin-film processing and material deposition for different products and technologies.

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