Improving cell efficiency and reducing costs: applying experiences in microelectronics

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This paper first appeared in the seventh print edition of *Photovoltaics International* journal.

ABSTRACT

The PV industry is expected to eventually reduce its manufacturing costs well below €1/Wp. Major technological changes lie ahead of us for manufacturing wafers, solar cells and modules if this cost target is to be met. In order to focus R&D efforts amongst the myriad options, and to speed up the learning curve, the PV industry (equipment vendors, material suppliers and PV manufacturers) may benefit from collaborative efforts guided by an ITRS-like roadmap. In this paper we present the IMEC roadmap, the target of which is to reduce drastically the amount of pure Si needed per Wp by combining efficiencies beyond 20% with aggressive reductions in wafer thicknesses.

Introduction

In 2008 the first PV systems were revealed to have reached grid parity [1]. Grid parity is now predicted to be within reach for the whole of southern Europe by 2012 [2], and may already have been reached in certain parts of Italy. Widespread introduction of PV will require a price level well below €1/Wp, bringing with it the possibility that crystalline silicon modules at this price level will look different from their current appearance. In many scenarios it has been predicted that in order for c-Si PV modules to reach costs < €1/Wp, great changes will be required [3]. Improved manufacturing practices, vertical integration, economies of scale (fabs may scale by a factor of 10 or more), increase of areal throughput, and standardization are essential to reduce costs, but will continue to require constant technological innovation.

With Si representing about 40% of the cost/Wp at module level [3], the amount of Si used per Wp has to be reduced drastically from the present 8-9g/Watt. Higher cell efficiencies are equally essential to reduce the contribution of the module fabrication costs.

ICT technology for PV: where are the opportunities?

There is a wide range of process technologies available for advanced Si-based devices and microsystems that have not yet found their way into PV production, but this is about to change. Fig. 1 suggests a classification of a number of technologies according to their potential to contribute to efficiency increases and/or reduced consumption of Si.

- Obvious gains are available by **improving emitter-doping profiles** beyond what can be offered by $POCl_3$ diffusion. The highest flexibility in this respect is offered by the use of epitaxial technology: near-ideal profiles can be grown starting with a lowly-doped emitter (enhancing the UV response) plus a highly-doped 'spike' at the very surface (acting as a Front Surface Field and reducing contact resistance) (Fig. 2). An important step towards throughput as required by PV is taken by batch type CVD systems for epitaxy [4]. Ion implantation can also offer the required degree of precision, and is (again) being explored for PV applications [5]. Lattice damage is often quoted as a concern but recent research shows that appropriate dose, energy and annealing conditions can effectively contain lattice damage and is certainly compatible with processing of high-efficiency devices in monocrystalline Si. In the case of implanters, we expect high throughput tool concepts (e.g. P3i) to come about soon in order to address the 'productivity gap' between IC and PV production.
- The opportunities for efficiency improvement by doping are all the more relevant when combined with improved metallization schemes such as those based on **laser ablation and Cu plating** (Fig. 3). Such a scheme allows an almost independent optimization of a shallow emitter profile and the metallization scheme – in contrast with the intricate compromises typical for screenprinted Ag metallization. Cells with efficiencies up to 18.5% have been demonstrated [6]. The remaining challenge is to develop self-aligned seed/barrier layers with the appropriate reliability properties to warrant 25+ years of performance. Several diffusion barrier layers are known to be effective against Cu diffusion into Si.
- Quantum device technology may eventually be essential to exceed the efficiency limitations of single-junction solar cells – for example by larger

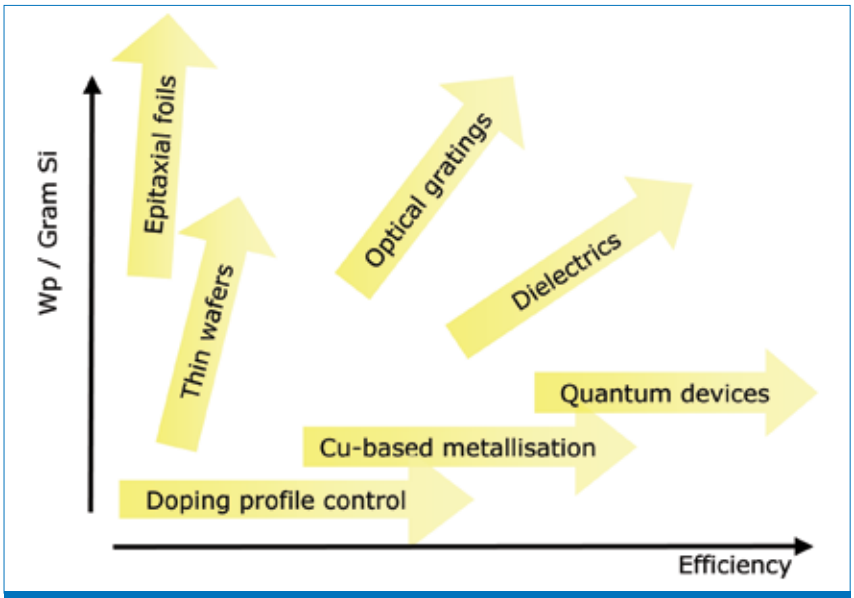

Figure 1. Indication of potential contribution of various novel process technologies to higher efficiencies and lower Si wafer consumption.

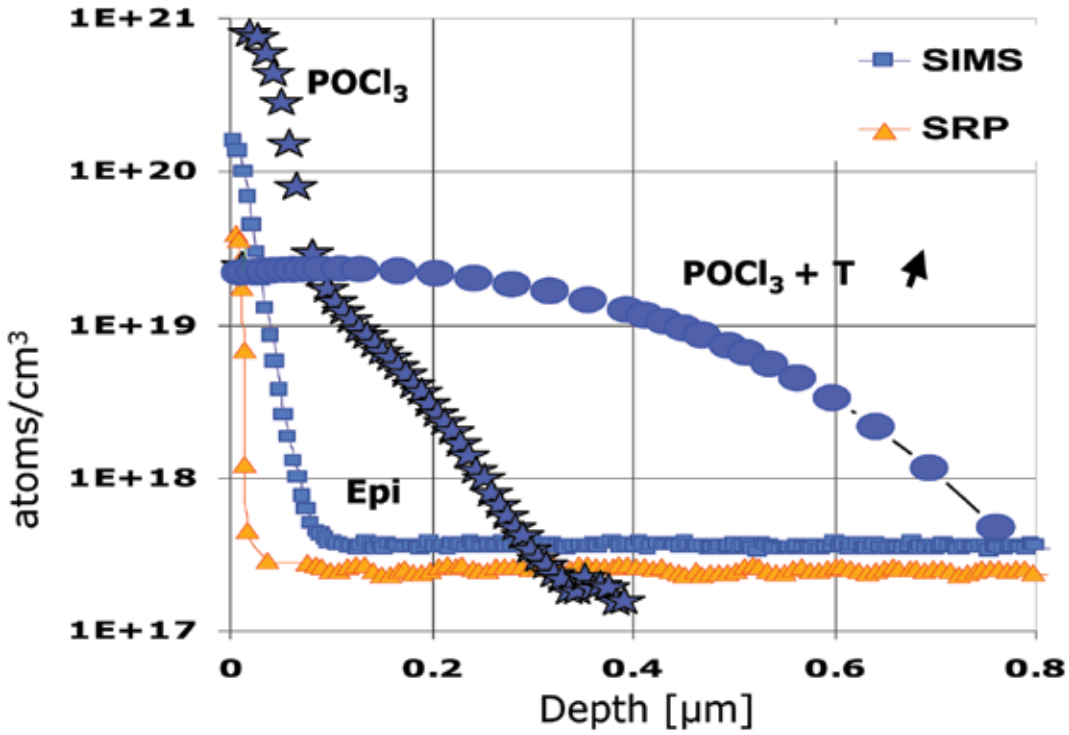

Figure 2. By using CVD epitaxy for the emitter, a very shallow emitter profile with a surface spike can be implemented as compared to the typical Gaussian distribution of a diffused layer.

bandgap (1.7eV) **nanowire solar cells** in all-Si tandem cells [7].

- Improved dielectrics are of paramount importance to increase the efficiency while reducing the amount of active Si. Typical silicon nitride layers as a surface passivation layer do not provide very low surface recombination velocities. **Atomic layer deposition** technology (e.g. Al_2O_3 deposited by thermal ALD) is heavily pursued in view of its unique combination of chemical and electrical passivation, and the repetitive nature of the process is seen as compatible with in-line processing. Recombination velocities as low as 10cm/s have been demonstrated [8] and the layers have been implemented in industrial solar cells [9].
- For very thin cells, optical enhancement schemes beyond texturization are instrumental in keeping high collection efficiencies in the infrared – for example **optical (submicron) gratings** may be put to use.
- Arguably the most important barrier today to using thin wafers in production is the lack of equipment handling below 150µm. This problem is not new, however. **Thin wafer transfer and handling** schemes have been developed in 3D integration that allow processing of Si wafers as thin as 50 or even 20µm. Several of these carrier and transfer techniques are applicable to the PV area.
- A way to circumvent the use of thin wafers altogether is to make use of high quality fully **epitaxial solar cells**, which are grown on low-cost Si substrates. The main challenge for industrialization of this approach is the availability of high throughput epitaxial systems. However, different reactor concepts and prototypes for high throughput epi-systems are currently under development.

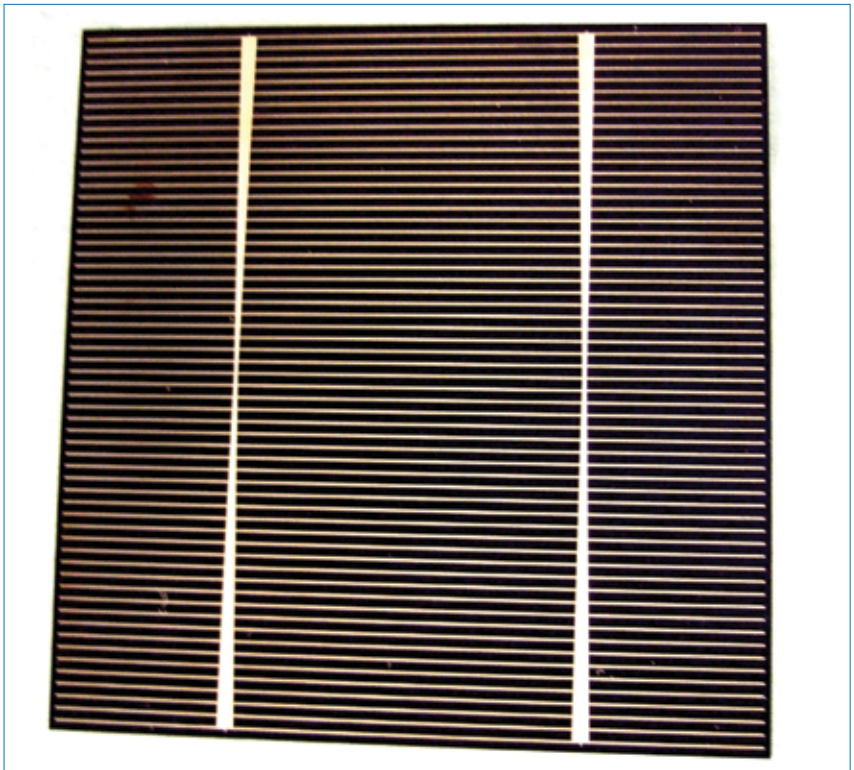

Figure 3. Large-area solar cell with efficiency of 18.3 % [6] made by laser ablated vias and Cu metallization at the front side.

A roadmap towards thinner Si solar cells

While the technical potential of the above technologies is clear, the challenge for their cost-effective introduction in PV production lines is tremendous and requires a concerted industrial effort. To focus R&D efforts amongst the plenitude of options, and to speed up the learning curve, the PV industry (equipment vendors, material suppliers and PV manufacturers) may benefit from collaborative efforts guided by an ITRS-like roadmap. Fig. 4 presents a possible

roadmap showing a drastic reduction of silicon thickness over the next decade.

Today's wafer-based processing concepts look set to be further pursued for a long time; such processing may potentially be extended down to 40µm cells. Several steps will lead to this end goal.

PERL and back-contact solar cells

We expect PERC and PERL-like concepts to enter the market first since these are a logical next step from today's front-side contacted cell manufacturing lines to industrial efficiencies of 20% for wafers of about 120µm ("**i-PERL**").

However, we believe BC cells may dominate further on the road in view of their inherent efficiency advantages (no shadowing) and their 'planar' processing nature (most processing is at one side of the wafer which facilitates integration of thin cells into modules). Today, BC solar cells made in 180µm wafers still require very high diffusion lengths and therefore costlier wafers. However, as thin wafers become more widely used, Si may overtake front-side cells in terms of market share (**i^2-BC**).

Ultrathin wafers, cells and module integration

For U-cells (ultrathin cells of 40µm), there is as yet no cost-effective technology for the production of high-quality ultra-thin wafers. Wire sawing may be limited to 100µm, with a kerf loss equal that width; ribbons are limited either by material lifetime or by industrial throughput. Several technologies are under investigation worldwide, such as that developed by Silicon Genesis [10]. Another possibility currently under investigation at IMEC, may be SLIM-Cut (Stress-induced Lift-Off Method) for fabricating thin foils below 100µm thickness without kerf loss [11]. This kerf-loss-free wafering method has demonstrated promising results down to 50µm, which amounts to savings of a factor of 6.

The challenge is that manufacturing such thin Si layers – with yield – will also require novel wafer handling concepts whereby the wafer is somehow supported during processing. This requires a review of the cell process since the use of a support has its own constraints. Carrier support techniques exploited in the field of 3D integration may be put to use here.

Cells with reduced wafer thickness will also impose specific requirements on the integration into modules. The conventional tabbing and stringing process used today is prone to creating cracks in thinner cells due to the thermo-mechanical stress of this assembly process. For back-contact cells, module integration schemes based on 'flip-wafer' mounting the cells with conductive adhesives or solder balls on a laminate substrate have been demonstrated but are still not widely used. An attractive alternative is a superstrate interconnection technology where back-contact thin cells are embedded on module glass by planar processing, an approach that is based on concepts that have successfully been demonstrated for ultra-thin ICs [12]. This approach can lead to material and manufacturing cost savings as compared to a substrate-based integration.

In view of the critical role of module integration technology on the operational lifetime of any PV system, innovative cell-module integration concepts can only be introduced successfully into the market if due consideration is given to reliability aspects. This requires the availability of ageing models for PV modules, which can be generated based on measurements of thermal/mechanical properties, Failure Mode and Effect Analysis, Finite Element Modelling, and accelerated ageing tests.

Thin-film epitaxial solar cells

But how thin can cells really be made before light trapping becomes elusive? Very encouraging results are obtained by use of **epi-cells** (see lower line in Fig. 4) where only a thin layer of (epitaxially grown) Si is acting as the solar cell. Elaborate optical enhancement schemes are put to work here, with a porous Si grating at the back-side of the cell (between the epi-layer and the substrate). This reflector strongly improves the optical confinement of light in the active part of

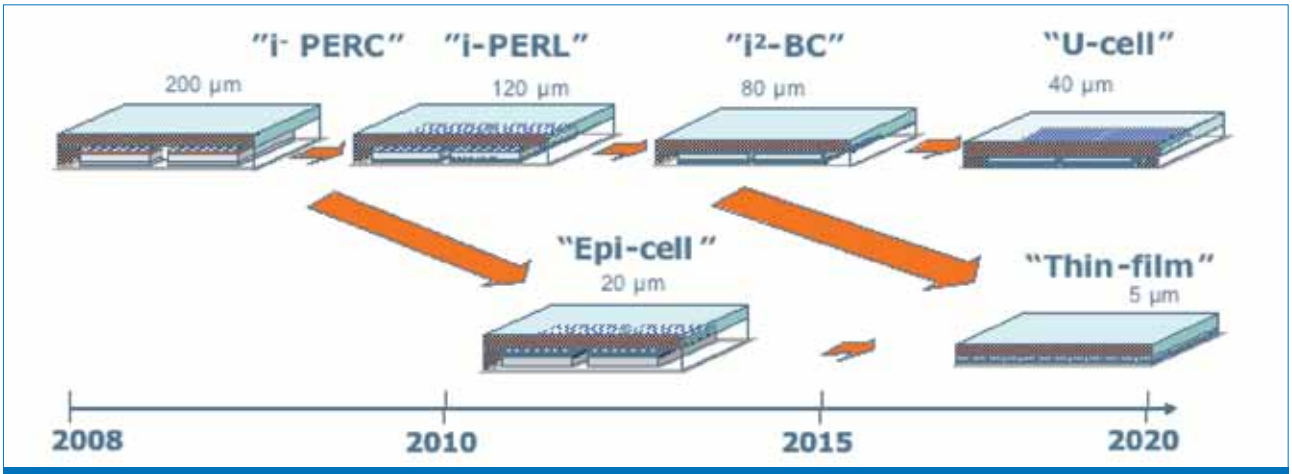

Figure 4. IMEC's crystalline silicon solar cell roadmap, predicting a continuous reduction of active layer thickness.

the cell. Lab efficiencies of 34.6mA. cm^{-2} (corresponding to an efficiency of 16.9%) have already been achieved [9] using a rear-emitter n-type cell with an active Si layer of only 25µm. These results bring industrial implementation of such epi-cells within the realm of possibility. It should be pointed out that this technology can also be used for growing thin-film solar cells on glass, and could one day form the ultimate thin-film Si solar cell.

Open innovation for the PV industry

In the past, introduction of process changes in existing solar cell lines was a relatively slow process, certainly when compared with the rapid technology evolution within the microelectronics sector. Apart from the already mentioned reliability problem, return on investment was also an issue. Due to the increasing size of the existing industrial PV players and the entrance of new players stemming from the microelectronic sector with their strong background in semiconductor processing and the rapid implementation of new processes, the introduction of new technologies is surely going to be accelerated. Thanks to the increased size of the industry, the development of PV-dedicated equipment becomes economically more viable

IMEC has launched a wafer-based silicon solar cell (Si-PV) Program around this Si-PV roadmap. The program aims to deliver the key process technologies required for the next generations of crystalline-Si-wafer-based solar cells. The concept is an 'open innovation' collaboration model, based on sharing of intellectual property and resources. This model has become an established means in the IC industry for enhanced collaboration between IC manufacturers, equipment vendors and material suppliers. Applying this model to the PV industry requires that particular attention be paid to differentiation possibilities for the PV manufacturing partners in the program.

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About the Authors

Dr. Kris Baert obtained his Ph.D. from Leuven University, Belgium, in 1990 on PECVD of thin-film c-Si. He then worked on poly-Si TFT-LCD's at Mitsubishi Electric (Japan) until 1992, after which he joined IMEC (Belgium) where he managed R&D in MEMS and Integrated Microsystems. Since 2008, he has worked as program manager of Si solar cells in the Photovoltaics Department.

Dr. Jozef Poortmans received his degree in electronic engineering from the Katholieke Universiteit of Leuven, Belgium, in 1985. He then joined the newly-built Interuniversitary Micro-electronic Centre (IMEC) in Leuven and received his Ph.D. degree in June 1993. Afterwards he joined the photovoltaics group, where he became responsible for the Advanced Solar Cells group. At the moment he is Program Director of the Strategic Programme SOLAR+ at IMEC and Director of the Solar and Organic Technologies Department.

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