LPCVD polysilicon passivating contacts for crystalline silicon solar cells

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ABSTRACT

Contact recombination has long been identified as one of the key challenges for achieving high efficiency of crystalline silicon (c-Si) solar cells. As well as having the ability to extract majority carriers effectively, a contact to a solar cell should ideally be passivating. The combination of a thin oxide and doped polysilicon to obtain low recombination junctions was demonstrated in the 1980s to be a viable candidate for creating passivating contacts to c-Si solar cells. In recent years variations and innovations of this technology have seen intense development and rapid progress towards demonstrating very high (25%) cell efficiencies. This paper presents the progress made by ECN and Tempress in developing and integrating the processing of polysilicon passivating contacts aimed at use in low-cost industrial cell production. The polysilicon is deposited by low-pressure chemical vapour deposition (LPCVD), and the results are presented for in situ as well as ex situ doping processes. Synergy and compatibility with industrial cell processing is demonstrated – for example, the application of hydrogenation from silicon nitride coating layers, and metallization by screen-printed fire-through paste. This demonstrates the potential application of polysilicon passivating contacts to a variety of cell designs in production in the near future. The way in which the passivating and contact properties depend on the layer parameters and subsequent cell processes is analysed and explained. Results are presented for 6" screen-printed bifacial n-type cells with a diffused boron emitter and an n-type polysilicon (n-poly) back contact, with an efficiency of 20.7%, as an industrially relevant application of the polysilicon technology. Ways to improve cell efficiency to > 22% are indicated.

Introduction to passivating contacts

Good contacts to solar cells should extract one type of charge carrier and have low series resistance, while avoiding recombination of the other type of charge carrier. In industrially produced silicon solar cells, contacts are mostly created by heavily doping the surfaces of the silicon wafer; this allows good Schottky contact to a metal electrode for the majority carriers, while at the same time reducing the minority-carrier density and therefore the minority-carrier recombination at the interface of the silicon with the metal electrode.

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Alternatives to these diffused junctions that are directly contacted by metal have been described and investigated for many years. One such option is *passivating contacts* (the original terminology 'passivat*ed* contacts' seems to have now become superseded by 'passivat*ing* contacts'). Reviews of the need for and potential benefit of passivating contacts, along with several approaches for creating them, were given by Green in 1995 [1] and Swanson in 2005 [2]. Swanson noted that the most ambitious target level could be given by the radiative limit of the silicon bulk – recombination current density J_0 = 0.27fA/cm^2. A (non-exhaustive) list of the most frequently reported approaches is given in Table 1 (see reviews in, e.g., Young et al. [3], Melskens et al. [4], Cuevas et al. [5]; also several materials are evaluated in Feldmann et al. [6]).

For crystalline silicon solar cells, a passivating but conductive interface, combined with an electrode with a low or high work function in order to properly align the conduction or valence band respectively, has been explored [3–6] (if the passivating interface is omitted, J_0 usually increases noticeably). To create electrodes with suitable band alignment to the silicon, heavily doped silicon can be employed. An advantage of this approach is the existence of feasible and widely known techniques for creating a low-recombination interface between the silicon wafer and a deposited doped silicon layer. Sanyo (later Panasonic) pioneered the development, as well as the application with very high performance, of amorphous silicon heterojunctions [7], where the passivating interface is a very

Passivating interface	Contact material	Reference
Intrinsic a-Si:H	Doped a-Si:H	[7]
SiO_x	Doped a-Si:H	[8]
Intrinsic a-Si:H	Set WF (e.g. TCO)	[9]
SiO_x	Set WF (e.g. TCO)	[3–6]
SiO_x	Highly doped polysilicon	†

† See the various references given in the present paper.

Table 1. The main published approaches for creating passivating contacts. In addition to SiO_x, other thin dielectric interfaces, such as Al_2O_3, are being explored. ('Set WF' denotes materials with a well-defined suitable work function in order to align to the conduction or valence band in the silicon; TCO = transparent conductive oxide.)

thin intrinsic amorphous silicon layer, and the carrier selective layer is doped amorphous silicon. Others (e.g. Heng et al. [8]) combine a thin oxide instead as the passivating interface with the doped amorphous silicon. Heterojunctions offer the additional advantage that a minority-carrier band offset enhances the so-called *minority-carrier mirror* effect. SunPower has reported that its Generation 3 interdigitated back-contact (IBC) cells use passivating contacts, but has not given any technical details [10].

Recently, much attention and effort has been directed at the use of doped polycrystalline silicon (polysilicon), in combination with a passivating interface based on a thin oxide. This paper will describe ECN/Tempress's progress and cell development results regarding such polysilicon passivating contacts. Specifically, the polysilicon is deposited by low pressure chemical vapour deposition (LPCVD).

The combination of a thin oxide (SiO_x) and doped polysilicon to obtain low recombination junctions originated in microelectronics, in work on bipolar transistors (see, e.g., Ashburn & Soerowirdjo [11]). This was demonstrated in the 1980s to be a viable candidate for creating passivating contacts on crystalline silicon (c-Si) solar cells [12,13]. The technology appears to have been dormant for many years, at least in terms of the number of published research results. In 2008 Borden et al. [14] published results of polysilicon passivating contacts (or, as they called them, *polysilicon tunnel junctions*) produced by microelectronics processing techniques. Then, in 2014, Feldmann et al. [15] published results for polysilicon passivating contacts produced by a high-temperature anneal of a doped thin amorphous silicon layer deposited by plasma-enhanced chemical vapour deposition (PECVD) on a thin oxide, resulting in a structure called *tunnel oxide passivated contact (TOPCon)*.

The polysilicon passivating contact

Fig. 1 shows a schematic of the structure of a polysilicon passivating contact. A key element is the thin oxide layer, which has a reasonably low interface recombination velocity (S_i), supported by a hydrogenation step. This thin oxide layer serves not only for passivation but also as a tuneable diffusion barrier, which is indispensable for keeping most of the dopant within the polysilicon layer, thus avoiding the creation of a typical diffused junction with disadvantageous Auger recombination in the wafer. The doped polysilicon layer, as a result of the induced field effect, reduces minority-carrier density in the wafer at the interface with the polysilicon, while providing good conductance for the majority carriers to the contacts applied to the polysilicon. With regard to passivation quality, there is no fundamental need for the thickness of the polysilicon to be much greater than the Debye length (only a few nanometres in highly doped silicon).

The interfacial thin oxide, in combination with the low minority-carrier density at the interface, results in a low transmission of minority carriers through the interface, thereby assuring minimal recombination in the polysilicon and at the metal contact. Together with the low-level penetration of dopants in the wafer, the result is excellent passivation. The oxide/polysilicon stacks can be contacted by metal, with (in practice) no indication that this increases the recombination of minority carriers generated in the c-Si wafer.

Example model results of the J_0 dependence on the interface recombination velocity and polysilicon doping level are given in Fig. 1(b). The model used is only approximate and is intended for illustration. Model studies have shown that an interface recombination velocity S_i of less than ~10^3–10^4cm/s [16,17] is sufficient for excellent passivation.

The thin oxide will in practice reduce not only minority-carrier transmission but also majority-carrier transmission. Nevertheless, sufficiently low contact resistances have been reported [15,18,19,20] by direct measurement, and have also been demonstrated by the high fill factors (FFs), in solar cells. Defects (pinholes) in the thin oxide can play an important role in determining the transmission of majority and minority carriers into the polysilicon, and can be more important than tunnelling. Furthermore, a small leakage of dopants through the thin oxide appears to be helpful in reducing series resistance [16] and improving passivation [21]. Römer et al. [18] applied a rather thick thermal oxide (>20Å thickness); this was subjected

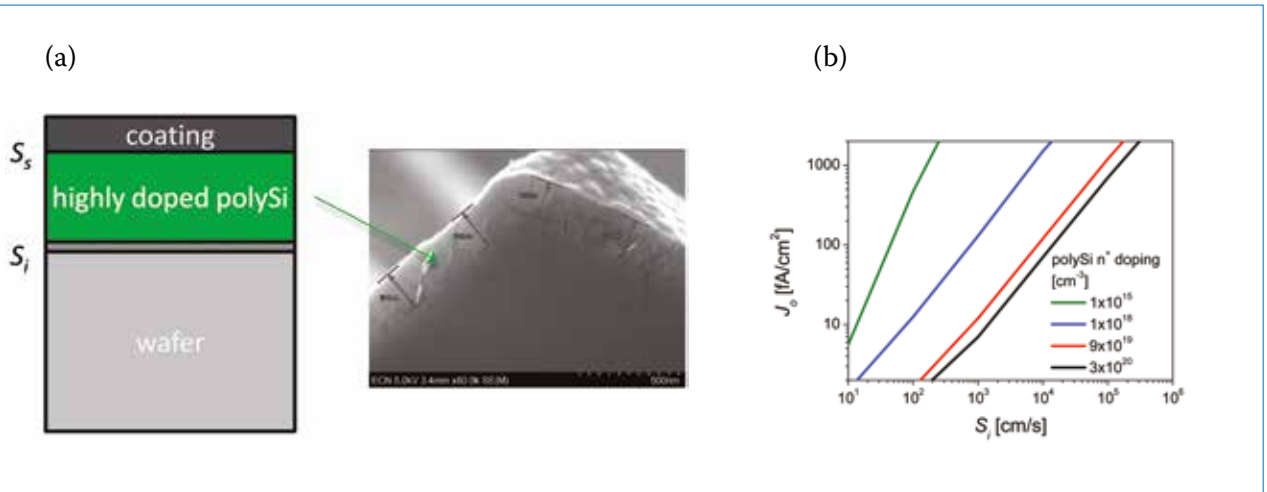

Figure 1. (a) Schematic of the structure of a polysilicon passivating contact. A stack of a thin dielectric (hashed) and doped polysilicon is grown on a silicon wafer. The polysilicon may be coated with metal (for contacting) or a dielectric (for anti-reflection coating, or hydrogenation). The interface recombination velocity S_i is low; the surface recombination velocity S_s does not affect the contact passivating properties and may be high. On the right is an SEM image of one of ECN/Tempress's polysilicon stacks on a textured wafer. (b) Modelled J_0 from PC1D as a function of the phosphorus-dopant concentration in the polysilicon. In the model the effect of the very small transmission of minority carriers into the polysilicon has been replaced by a very low S_s, to render negligible any recombination in or on the polysilicon.

to a high-temperature treatment above 1000°C, which probably decreased the resistance (created pinholes in the oxide).

In ECN/Tempress's results, even when a thin oxide (nominally 13Å thick) is used and 900°C is not exceeded in the process, the contact resistances in the cells, measured by TLM, appear to be inconsistent with a tunnelling model for carrier transport. For simultaneously processed p-type polysilicon (p-poly) contacts and overcompensated n-type polysilicon (n-poly) contacts, with identical oxide, polysilicon deposition and thermal budget, ECN/Tempress found a specific contact resistance ρ_{co} of polysilicon to wafer of about 30mΩ·cm^2 for n-type and 5mΩ·cm^2 for p-type polysilicon [22], with J_0 below 10fA/cm^2 and ~50fA/cm^2 respectively (the p-type J_0 value is quite high, presumably as a result of the low boron doping concentration of 3×10^{19}cm^{-3}, and because of a textured surface). If tunnelling were dominant, a higher ρ_{co} would be observed for p-type polysilicon than for n-type [23]. Recently, Yan et al. [24] also reported a low ρ_{co} for p-type polysilicon.

The excellent low J_0 values of polysilicon passivating contacts are hard to beat by traditional dielectric-passivated diffusions. But conventional high-performance contacts based on local diffusion with metal point contacts can also yield low contact recombination at the cell level, through reducing the contact area. The ratios of specific contact resistance ρ_{co} and J_0 of the metal and the polysilicon are not more favourable for polysilicon: polysilicon combines a J_0 of a few fA/cm^2 with a ρ_{co} of ~10mΩ·cm^2, while diffused metal contacted regions can have a J_0 that is ~100 times higher, but also a very low ρ_{co}, which allows their area to be reduced by a similar factor. However, for metal point contacts, a negative side effect is spreading resistance, which reduces the FF (see, e.g., Glunz et al. [25]). Aspects of the trade-off between area fraction, J_0 and ρ_{co} have been illustrated in detail by other authors [26,27].

> "The excellent low J_0 values of polysilicon passivating contacts are hard to beat by traditional dielectric-passivated diffusions."

To summarize, the attractiveness of polysilicon passivating contacts derives from being able to:

- achieve an excellent J_0;
- avoid Auger recombination from heavily diffused areas in the wafer;
- avoid process complexity and the spreading-resistance effect related to metal point contacts.

Industrial LPCVD of polysilicon passivating contacts

This section will focus on ECN/Tempress's studies of n-type polysilicon passivated contacts. Polysilicon layers grown in a high-throughput LPCVD furnace are employed. An LPCVD process has the advantage of creating very conformal and pinhole-free layers; this ensures that the underlying interfacial oxide is protected against subsequent doping steps and chemical treatments. For mass production, batches of up to a few hundred wafers can be processed, with excellent process uniformity [28].

The thin oxide was produced by thermal oxidation (Th.Ox.) or wet-chemical oxidation (NAOS: nitric acid oxidation of silicon). A reliable absolute thickness measurement is not straightforward; in this work the thickness was estimated by spectroscopic ellipsometry on mirror-polished wafers, with the resulting typical values of 13 to 15Å corresponding to good performance. A high repeatability and tuning of this thickness at the 1Å level is possible. A slightly greater thickness can result in a noticeably reduced FF, whereas a slightly smaller thickness can lead to increased dopant diffusion into the wafer. Of course, this depends on the precise doping processes and thermal budgets, as well as on other process parameters [18,20]. Excellent contact resistance and passivation have been obtained with these thin oxides.

The main focus was on n-type polysilicon, where the LPCVD layer is intrinsic, and subsequently doped by $POCl_3$ diffusion [28,29] (Fig. 2): this results in fast deposition, a tuneable doping level, low diffusion into the wafer, and excellent J_0. In situ p-type doped polysilicon for cell processing has also been investigated [28,30]. Alternatively, in situ doping during LPCVD to create n-type polysilicon, and BBr_3 doping of intrinsic polysilicon to create p-type polysilicon, are in principle also possible [18,31]. However, in situ phosphorus doping during LPCVD has been reported to reduce deposition speed [32], and BBr_3 doping of an oxide/polysilicon stack can cause damage to the thin oxide and

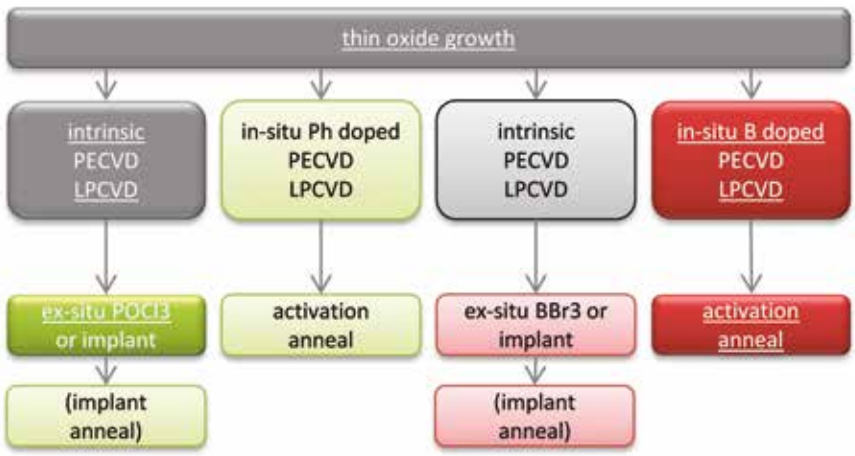

Figure 2. Examples of deposition and doping methods used in creating an n-type or p-type polysilicon passivating contact. (The approaches reported in this paper are underlined.)

thereby result in too much diffusion into the wafer [28].

The application to industrial cell processing is an important aspect, so with this in mind the following were used:

- Hydrogenation from SiN_x:H coating layers deposited by PECVD.
- Contacting of the polysilicon by fire-through screen-printed metallization, without adding significant contact recombination.

In other reported studies hydrogenation is often carried out by an extra processing step, such as a forming-gas anneal, but hydrogenation from SiN_x:H eliminates the need for this. The second point, contacting by screen-printed metallization, has the potential benefit for industrial application of the passivating contact as basically a drop-in replacement for a diffused back-surface field (BSF). With a screen-printed metallization grid, an additional advantage is that a bifacial cell is possible. In view of the use of fire-through metallization, relatively thick layers of polysilicon have so far been investigated.

n-type polysilicon

Fig. 3 shows active phosphorus concentration profiles, measured by electrochemical capacitance–voltage profiling (ECV), in polysilicon layers with thicknesses of 70 and 200nm. The intrinsic polysilicon layers were doped by $POCl_3$ diffusion at three different temperatures. It is noticeable that the thin oxide can be an excellent diffusion barrier. However, a high diffusion temperature together with the use of NAOS oxide resulted in significant diffusion into the wafer. The corresponding R_{sheet} values are also indicated on the graphs. In the results obtained here, the mobility is at best around one-half to one-third of that in monocrystalline silicon, and it can be enhanced somewhat by hydrogenation.

The polysilicon layers in Fig. 3 showed a strong correlation between the sheet resistance and the diffusion temperature. This indicates that the mobility heavily depends on the diffusion temperatures, which is perhaps related to continued crystallization of the polysilicon during the diffusion. After exposure to the lowest diffusion temperatures, the apparent mobility is much lower (approximately one-tenth) than that for monocrystalline silicon.

Fig. 3 also presents the evolution of the recombination parameter J_0 through subsequent processing steps of PECVD SiN_x:H deposition, firing and SiN_x:H removal. An average J_0 per side of less than 10fA/cm^2 was already achieved without a particular hydrogenation step. A rough correlation between the initial J_0 values and the doping levels and leakage can be observed. The higher initial J_0 of the 200nm-thick layers with high R_{sheet} is probably due, at least partly, to the lower doping level, which increases sensitivity to the defects at the interface. For the 70nm layers with Th.Ox., the doping level and J_0 are in the same range as that for the most heavily doped 200nm layer. In the case of the 70nm polysilicon/NAOS stacks, the initial J_0 is probably dominated by the effects of phosphorus leakage through the oxide. After $POCl_3$ diffusion at the highest temperature (72Ω/sq.), the high J_0, probably due to Auger recombination or increased interface defect density, renders the J_0 unsuitable for practical applications.

Improved J_0 values were observed after PECVD SiN_x:H deposition, in particular for the 200nm n-type polysilicon layers with a low doping level. The benefit of SiN_x:H deposition is attributed to the hydrogenation of the SiO_x/wafer interface. The firing of the SiN_x:H layer did not significantly change J_0. Likewise, the removal of the SiN_x layer by wet-chemical etching did not change J_0, as expected, since this etching step should not change the hydrogen passivation of defects at the SiO_x/wafer interface, which is protected by the polysilicon top

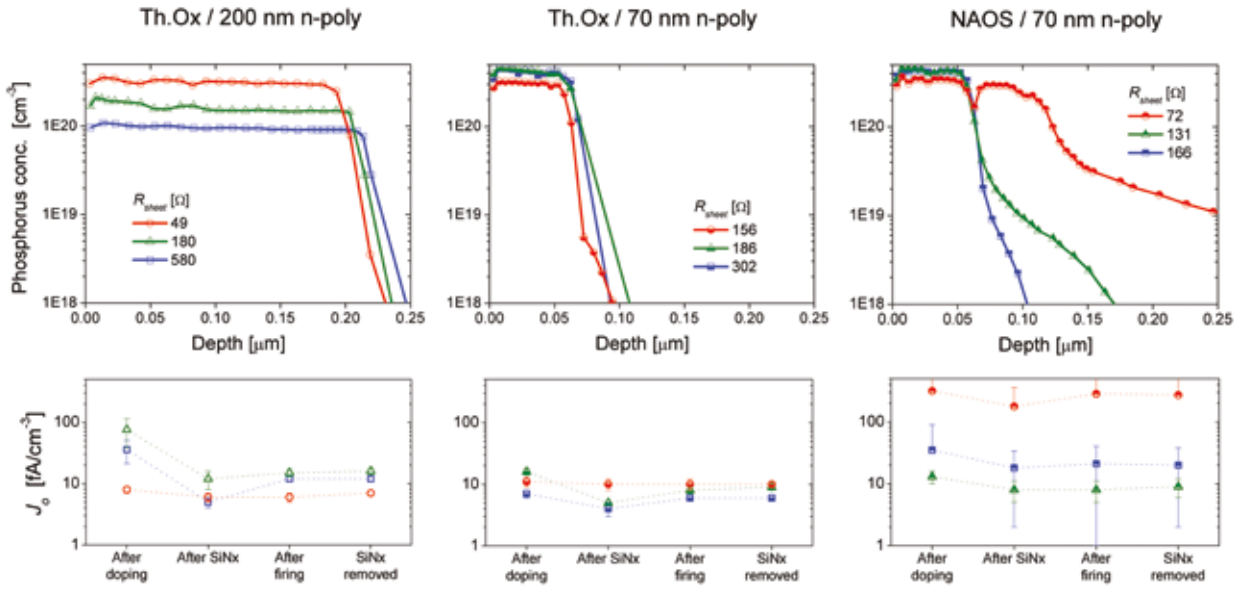

Figure 3. Phosphorus-doping profiles (top row) of several n-type polysilicon/SiO_x/Cz-Si stacks, with the corresponding R_{sheet} values, on polished Czochralski (Cz) wafers. Three different $POCl_3$ diffusion temperatures (the same for all stacks) were used for doping, with high to low temperatures corresponding to low to high R_{sheet} values. Evolution of the surface passivation quality (bottom row), through a sequence of process steps. All J_0 values are per side, and are the average of up to 15 points on three wafers, where the error bars depict standard deviations. J_0 was derived from lifetime measurements using the Sinton WCT-120 tool.

layer. A forthcoming publication [33] will report in detail the polysilicon hydrogenation processes.

Fig. 4 shows the evolution of average J_0, in this case for textured wafers; importantly, it includes fire-through contact metallization. Although the initial J_0 for textured surfaces is larger than for polished surfaces by more than the surface area ratio, after PECVD SiN_x:H deposition the J_0 values are comparable. After the fire-through of a metal contact grid, some degradation of J_0 occurred, the extent of which depends on firing parameters and paste.

p-type polysilicon

Fig. 5 shows the results for p-type polysilicon. In order to properly carry out the boron doping of the polysilicon ex situ, one needs a considerably higher thermal budget than that for n-type doping. This, combined with the fact that silicon oxide is a much worse diffusion barrier for boron, makes the fabrication of a p-type doped polysilicon passivated contact by BBr_3 diffusion much more difficult. Tempress has developed in situ boron-doped polysilicon growth in an industrial LPCVD furnace. An optimization of hardware and growth process results in a uniformly doped polysilicon. A mild anneal temperature can be used to activate the dopant, thus avoiding damage to the underlying interfacial oxide.

The p-type polysilicon is more dependent on surface properties and hydrogenation than n-type polysilicon. An excellent J_0 of 21fA/cm^2 can be obtained on a polished surface after hydrogenation by PECVD SiN_x:H, which is reduced to 12fA/cm^2 by the firing. The p-type polysilicon on a textured surface demonstrated significantly higher J_0. It should be pointed out that the boron concentration of 3–4×10^{19}cm^{-3} achieved so far is lower than that of a typical industrial BBr_3-diffused emitter. It is expected that increases in the polysilicon doping level will lead to an enhancement of the surface passivation and to a reduction in J_0, especially for textured surfaces.

Interestingly, these p-type polysilicon layers can be compensated to n-type by either ion implantation or $POCl_3$ diffusion, resulting in values of J_0 and implied open-circuit voltage iV_{oc} as good as those for non-compensated n-poly (Wu et al. [30], and similar work reported earlier by Reichel et al. [34] and Römer et al. [35]).

Table 2 shows a summary of the best passivation characteristics measured for the samples in Figs. 3–5. For industrially suitable processes, these are already very useful improvements over diffused junctions, even before contact metallization. It is noted that even lower J_0 values, of less than 1fA/cm^2, have been reported in

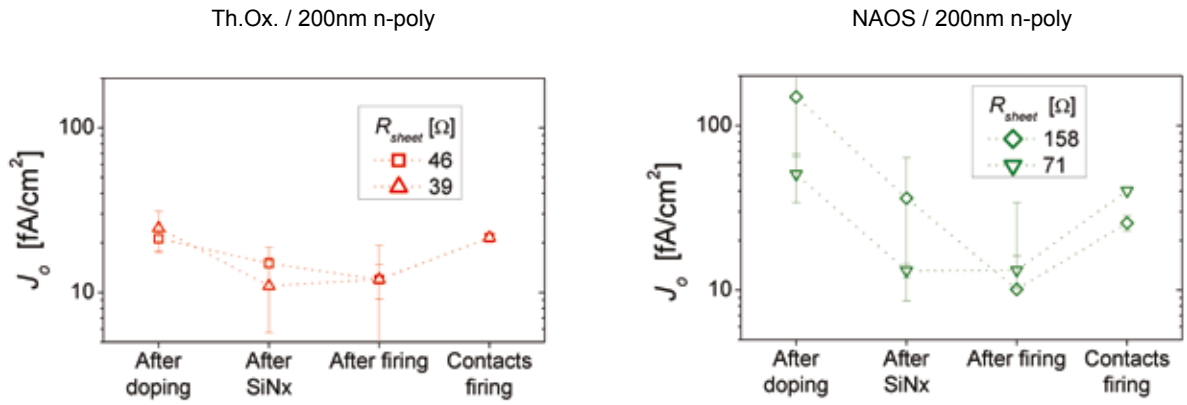

Figure 4. Evolution of J_0 through the process steps relevant to cell production, for textured wafers with 200nm n-type polysilicon, over several test runs. The highest diffusion temperature in Fig. 3 was used for Th.Ox., and the middle temperature for NAOS.

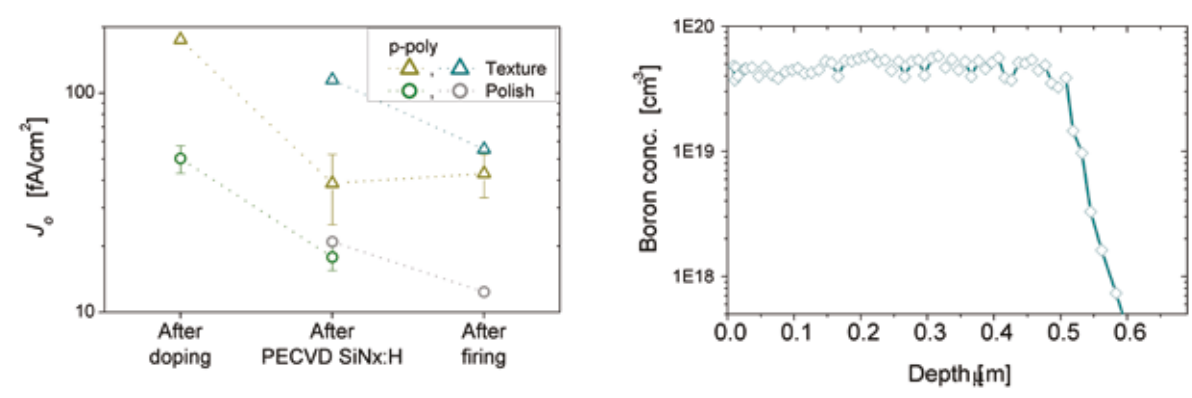

Figure 5. Development of average J_o with SiN_x deposition and firing over several test runs, and ECV doping profile of in situ doped p-type polysilicon/SiO_x passivating contacts.

the literature for n-type polysilicon passivated contacts on polished surfaces [36]. For textured Cz wafers, the recombination currents of ~4.2fA/cm^2 (Table 2) achieved in this study for n-poly are, to the authors' knowledge, the lowest reported to date.

Application to industrial bifacial n-type cells

Various c-Si cell design variations making use of polysilicon passivating contacts are conceivable, using the polysilicon for one or both of the contact polarities. A uniform polysilicon layer can be used at the rear of a cell as the emitter or base contact. Here the results for an n-type cell with a front diffused boron emitter and an n-type polysilicon back contact (Fig. 6) will be elaborated on. This kind of cell with an n-type polysilicon back contact has been widely investigated in recent years, but what differentiates ECN/Tempress's development is the use of a bifacial metallization with fire-through paste, and the full 6" cell size combined with an LPCVD process.

Table 3 lists the status of n-type cells with a front boron emitter and a polysilicon back contact that have been reported in the literature. The designation *PERPoly* (passivated emitter and rear polysilicon) is proposed for the cell design with a polysilicon back contact, in line with the PERT, PERC and PERL acronyms.

ECN/Tempress's n-type cell process on industry-standard 6" Cz wafers has been developed using only the tools currently available to the industry. A diffused boron emitter is used, in order to remain close to ECN/Tempress's industrial n-PERT process. A diffused boron emitter can yield very high performance (low J_0), and is therefore a good match for a high-performance back passivating contact.

The PERPoly cell process is expected to be feasible using a comparable number of process tools to that required for PERC cells, although at the moment some more-elaborate chemistry is still used. A BBr_3-diffused industrial-type uniform emitter with a sheet resistance of 70Ω/sq. was employed on the front side. The emitter was passivated with Al_2O_3 deposited by atomic layer deposition (ALD), and coated with PECVD SiN_x:H; the rear-side polysilicon was also coated with SiN_x:H. Fig. 7 shows that iV_{oc} before metallization is approximately 700mV and fairly uniform over the wafer. In recent tests using a higher emitter sheet resistance, the iV_{oc} was increased to slightly more than 700mV, and the total J_0 was reduced to less than 45fA/cm^2.

	iV_{oc} [mV]	J_0 [fA/cm^2]	Lifetime [ms @Δn=10^{15}cm^{-3}]
Wafer surface = polished			
n-type, after doping	~731	~3.4	~5.0
n-type, after SiN_x	~743	~2.2	~6.6
n-type, after SiN_x and firing	~734	~5.2	~9.4
p-type, after SiN_x and firing	~715	~12	~1.6
Wafer surface = textured			
n-type, after SiN_x and firing	~732	~4.2	~6.2
p-type, after SiN_x and firing	~682	~55	~0.7

Table 2. Best passivation characteristics of polysilicon passivating contacts on PV-grade Cz wafers obtained in this study. ('Lifetime' = effective minority-carrier recombination lifetime; iV_{oc} = implied V_{oc} determined using a Sinton WCT-120; phosphorus-doping level = ~3×10^{20}cm^{-3}; boron doping level = ~4×10^{19}cm^{-3}.)

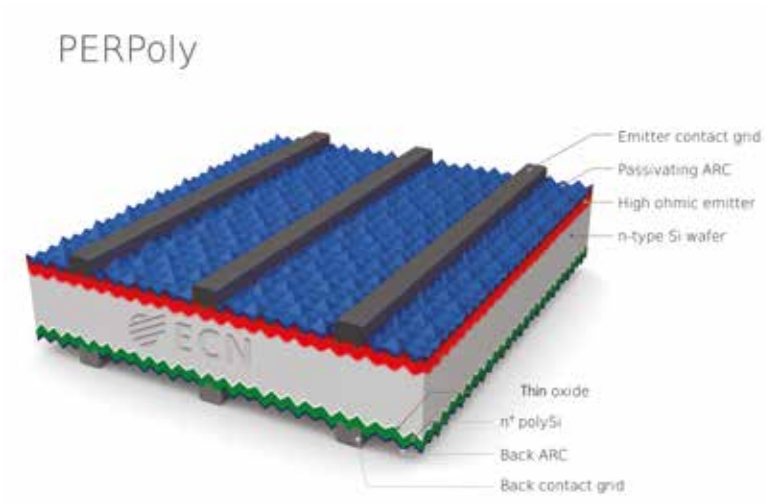

Figure 6. Schematic of the bifacial n-type solar cell design discussed in this paper – PERPoly (passivated emitter and rear polysilicon). The cell features an n-type polysilicon/SiO_x back contact.

Poly deposition	Poly doping	Back contact	Emitter	Front contact	Size [cm^2]	η [%]	Ref.
PECVD	In situ	Ag PVD	BBr_3, SE	Litho/PVD/plate	4	25.1	[25]
PECVD <20nm	In situ	Ag PVD	Implant	Screen print	239	21.2	[37]
LPCVD 40nm	In situ	Ag PVD	Implant	Screen print	132	20.9	[38]
PECVD 50nm	In situ	Al PVD	BBr_3	Not specified	4	20	[39]
PECVD 32nm	$POCl_3$	Al PVD	BBr_3	Litho/PVD	4	20.8	[20]
LPCVD 200nm	$POCl_3$	Screen print	BBr_3	Screen print	239	20.7	[29]

Table 3. Status of front- and back-contact cells with polysilicon passivating contacts.

In the cell process tests, only the 200nm-thickness polysilicon has been employed so far. The front and back metal grids were screen printed using fire-through pastes and co-fired.

"The PERPoly cell process is expected to be feasible using a comparable number of process tools to that required for PERC cells."

Table 4 presents an overview of the best *I–V* results for the bifacial cells. A best cell efficiency of 20.72% (spectral-mismatch-corrected, FhG ISE-calibrated n-PERT reference cell, AAA Wacom system, in house) was obtained, with a V_{oc} of 675mV. The cell efficiency distribution over the six cells of the best group, with a back contact of NAOS/n-poly, was an average of 20.67% with a standard deviation of 0.05%. The main loss mechanisms will be briefly described in the following sections.

Diffused emitter and contact recombination

An analysis and comparison of the half-fabs and cells shows that V_{oc} is mainly limited because of the diffused boron emitter and contact at the front side. This is not surprising, as the rear J_0 is only ~10% of the front emitter J_0, and, after contacting, the difference will be even greater.

The bulk lifetime of the cell half-fabs before metallization is about ~3ms on average, and the total J_0 close to 60fA/cm^2; together this results in an average iV_{oc} of ~693mV. After contact firing, the cell V_{oc} decreases to 675mV. The effect of the fire-through grid, with metallization coverage of around 10%, on the J_0 of the n-poly back contact was estimated on the basis of Fig. 4 to be ~13fA/cm^2; the front contact grid is known to contribute about 60fA/cm^2, because of a specific J_0 of 2,500fA/cm^2 for the fire-through metallization. This results in the breakdown of recombination currents shown in Table 5.

Current loss and bifaciality

In addition to the usual reflection losses, some of the loss in J_{sc} is due to free-carrier absorption (FCA), and

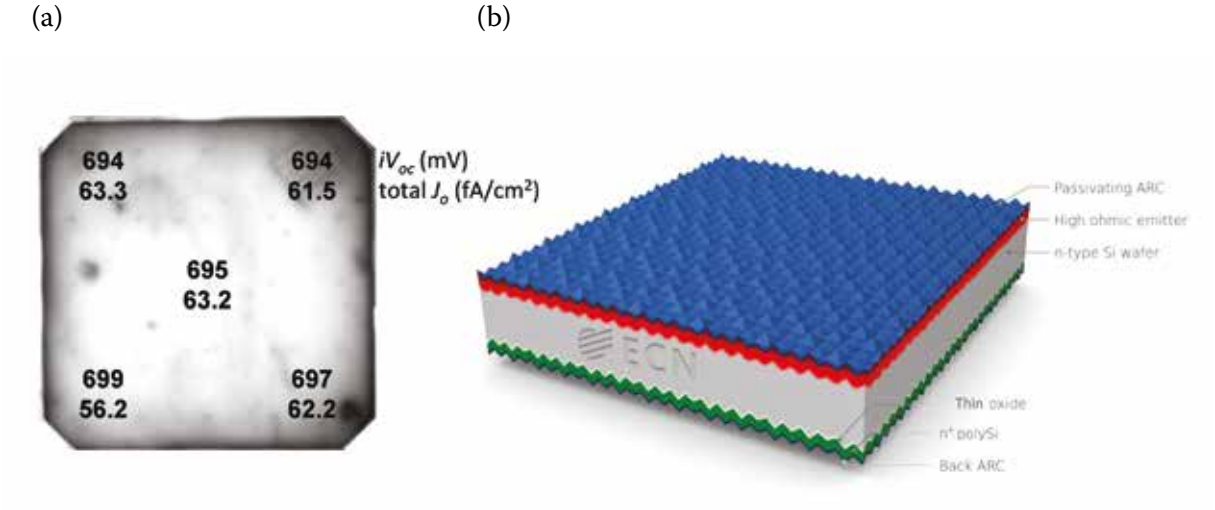

Figure 7. (a) Photoluminescence image of the solar cell half-fabricate (half-fab), with iV_{oc} and J_0 obtained at five locations. (b) Structure of the half-fab. R_{sheet} of the 200nm-thick n-poly is approximately 70Ω.

	J_0 n-poly* [fA/cm^2]	J_0 F+B half-fab* [fA/cm^2]	Bulk lifetime [ms]	iV_{oc} half-fab* [mV]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	pFF [%]	η [%]
Group ave. (6 cells)					674	38.8	79.1		20.67
Best cell	7.7	56.2	6.68	699	675	38.8	79.1	82.8	20.72
Best cell rear response					669	31.3	79.6		16.66

* Best spot

Table 4. Results for the PERPoly cells of ECN/Tempress (this study). Both cell sides were textured. Polysilicon thickness was 200nm. The best cell results are shown, as well as the best J_0, iV_{oc} and bulk lifetime obtained on half-fabs. J_0 F+B is the J_0 of the front and back sides together. The rear metallization coverage is approximately 10%.

Back n-poly	Back contact	Emitter	Emitter contact	Bulk	Total
7	13	50	60	8	138

Table 5. Estimated distribution of the recombination losses (in fA/cm2) of the cells listed in Table 4.

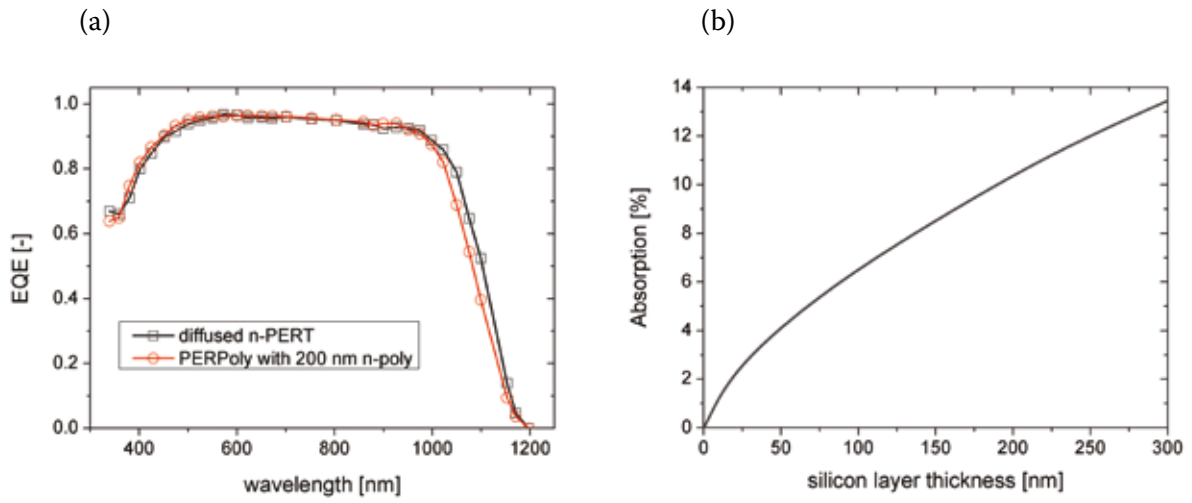

Figure 8. (a) EQE of a PERPoly cell compared with an n-PERT cell, showing in particular the difference due to FCA in the range from 1000 to 1200nm. (b) The absorption of AM1.5 spectrum in thin crystalline silicon as an approximation of the loss in a polysilicon layer when used at the light-incident side of a solar cell.

absorption with carrier generation in the polysilicon. Since the n-poly back contact is quite heavily doped to a low sheet resistance, the FCA is significant compared with bifacial n-PERT cells with a diffused BSF, as visible in the external quantum efficiency (EQE) plots in Fig. 8. The total FCA in the n-poly was evaluated by ray tracing analysis to be approximately 0.9mA/cm^2 for a thickness of 200nm and a phosphorus-doping level of 3×10^{20}cm^{-3}. This FCA can be significantly reduced by decreasing the polysilicon thickness or doping level, if the contact metallization allows. However, because of the reduced carrier mobility in the polysilicon, the FCA in a bifacial design with polysilicon will probably always be somewhat higher than in a corresponding bifacial design with a diffused BSF.

The PERPoly cells have around 80–85% bifacial performance (with rear full-area 200nm-thick n-poly; ~50Ω/sq.), which is ~10% less than for equivalent n-PERT cells with a diffused BSF. This extra 10% loss is in agreement with the estimated absorption of short-wavelength photons in the polysilicon, approximated by the absorption of regular crystalline silicon (see Fig. 8(b)).

Resistive loss

The FF of the PERPoly cells is similar to the typical FF of equivalent n-PERT cells with a diffused BSF, and it seems that there is no significant series resistance (not more than about 0.1Ω·cm^2) in the polysilicon/oxide/wafer junction. This is in agreement with the TLM measurements described earlier.

Outlook

On the basis of the experimental results obtained, a qualitative description of the key features of the polysilicon passivating contact can be given. The thin interfacial oxide layer needs to be sufficiently thin to not limit the transmission of the majority carriers (allowing high FF); however, it should be dense enough to serve as a diffusion barrier, so that most of the doping is contained in the polysilicon layer. Slight dopant in-diffusion into the c-Si wafer is not harmful for the passivation properties, and can be additionally beneficial for the transport of the majority carriers.

The polysilicon layer needs to be sufficiently highly doped to allow adequate lateral transport for the application of bifacial grid metallization and also for the field effect passivation. The polysilicon must be of adequate thickness in order to block any penetration by the fire-through paste into the thin oxide interface. In this study the 200nm polysilicon thickness did not completely avoid contact recombination, but it is expected that, after optimization, the results will be improved and will allow thinner polysilicon as well. The thinner and more lightly doped the polysilicon is, the lower the parasitic absorption losses will be.

It has been observed that, particularly for textured samples, the hydrogenation of the interface defects is very important, and that PECVD SiN_x:H is a very effective hydrogenation source for this purpose.

Fig. 9 presents a roadmap towards achieving 22% efficiency using industrial process equipment and materials. First, the parasitic absorption in polysilicon needs to be reduced by making the layer thinner or by using lighter doping. Second, the total J_0 can be further reduced to 50fA/cm^2 by implementing a higher R_{sheet} emitter (25fA/cm^2 or lower should be possible for a passivated boron emitter) along with less-penetrating fire-through pastes, or a selective emitter (a specific emitter contact J_0 below 500fA/cm^2 will be required). Finally, the resistive losses need to be reduced by optimizing the thin interfacial oxide, optimizing the front and back contact grids, and reducing the wafer resistivity.

Conclusions

This paper has presented ECN/Tempress's studies of polysilicon passivating contacts and their application to the rear side of a high-performance bifacial n-type solar cell with fire-through screen-printed metallization and processed on 6" Cz wafers. This cell design has been named *PERPoly* (passivated emitter and rear polysilicon). The polysilicon/SiO_x passivating carrier-selective contact structures were produced using an LPCVD-based process. The cell manufacturing comprised, in addition to the LPCVD step, processing that uses only a small number of industrial tools, comparable to current n-PERT process flows on the market. A highest efficiency of 20.7% was achieved for the PERPoly cell, along with an average cell V_{oc} of 674mV. As an added benefit, the cells

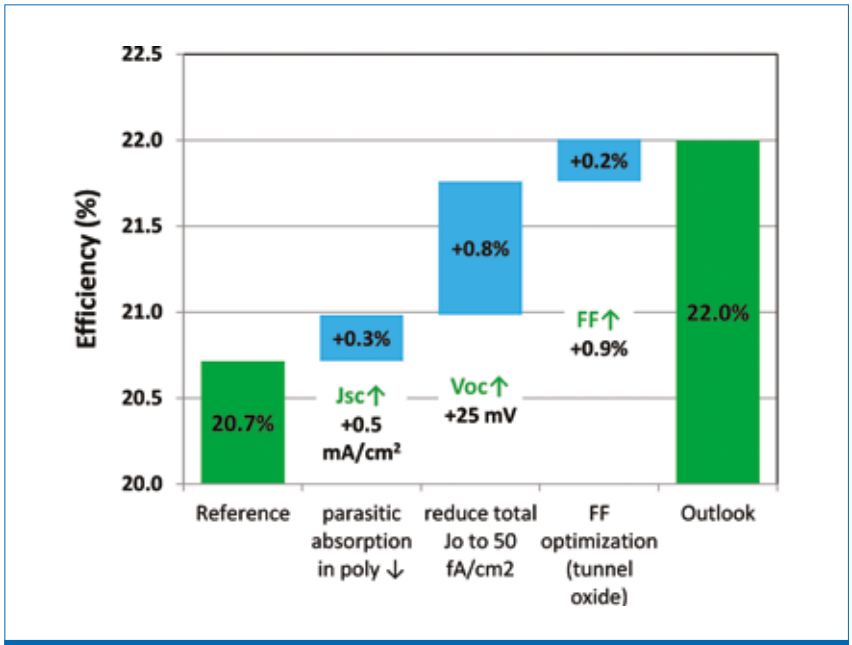

Figure 9. Roadmap towards achieving a 22%-efficiency PERPoly cell.

are bifacial with a bifaciality factor of greater than 0.8. To the authors' knowledge, these are the first 6" cells employing LPCVD for the polysilicon, and also the first cells employing a polysilicon passivating contact with fire-through screen-printed metallization.

> "A highest efficiency of 20.7% was achieved for the PERPoly cell, along with an average cell V_{oc} of 674mV."

The way in which process parameters influence the passivating contact effectiveness was described. Excellent passivation was obtained on polished and textured surfaces, with recombination current densities J_0 of ~2fA/cm^2 and ~4fA/cm^2 respectively. p-type contacts demonstrated a J_0 of ~12fA/cm^2; it is expected to reduce this by using a higher boron doping level in the polysilicon. The effect of the fire-through grid on the J_0 in the case of the 200nm-thickness n-poly contact was evaluated to be in the range 10–20fA/cm^2.

These results demonstrate the high potential of this technology for augmenting current cell processes, with a lot of headroom in the future in terms of performance. Achieving 22% seems feasible through making a number of improvements, especially on the emitter side. This brings the use of polysilicon passivating contacts closer to becoming a reality in low-cost industrial solar cell processing.

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