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Exploiting the microelectronics toolbox to boost Si PV manufacturing

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ABSTRACT

To make solar energy cost effective, the photovoltaic (PV) industry has to reduce its manufacturing costs well below 1€/Wp. To reach this cost target, roadmaps for c-Si technology foresee a drastic reduction in the amount of high-purity Si used and an increase in solar cell efficiencies beyond 20%. But this requires advanced cell concepts that put more stringent requirements on process steps such as doping, cleaning and surface passivation. Several processes in the technology and analysis toolbox of microelectronics offer opportunities to meet these stringent requirements. In this paper, we give examples of recent progress in solar cell development that has been achieved by implementing CMOS-like process steps, and we discuss how these processes can be attuned to the needs and benefits of the solar industry.

Introduction

For several years, the photovoltaic (PV) market has been dominated by crystalline Si (c-Si) solar cells, with a market share of about 85% of the total worldwide solar cell production in 2010. Today, the majority are manufactured from Si wafers which are about 180µm thick and have an Ag metal grid at the front side and an Al contact fully covering the back side. The cells are then assembled into modules and the resulting PV system costs about 2–3€/Wp, which in north-western Europe is equivalent to an electricity cost of 0.25–0.35€/kWh. This is still too high if economic competitiveness of PV electricity with conventional power plants is to be ensured. Consequently, the PV industry is systematically lowering the production costs of this process. It is doing this by increasing the cell's efficiency, in combination with improved manufacturing practices, increase of areal throughput of equipment, upscaling of fabs and vertical integration within the value chain. With the implementation of these measures, the '1€/Wp' system cost is now coming in sight [1].

Yet this will not be sufficient to reach a cost target of 0.5€/Wp, prompting the need for innovative solar concepts that use new materials and production techniques. For example, solar cells using less of the precious Si per Wp (at present 8–9g/W) are needed, and other expensive and non-sustainable materials like Ag must be replaced. We foresee that the industry will gradually move to back-contact cells, which may eventually become as thin as 80 or even 40µm, if novel techniques to realize and handle such thin foils become available. Such thin cells can be handled only by module-level processing in which the processing of cell and module eventually merges. Simultaneously, the high cost of PV module assembly can most readily be reduced by assembling even more efficient PV cells, with efficiencies that go beyond 21%, in a cost-effective way [2,3].

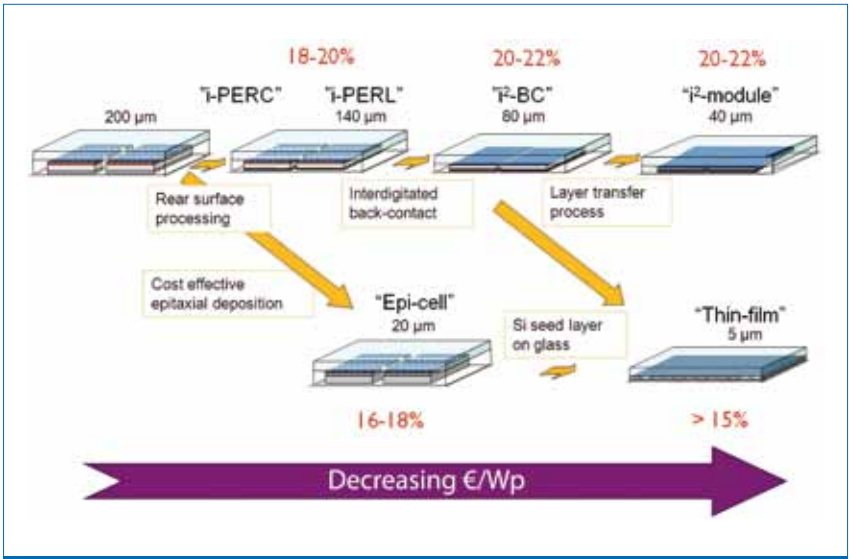

Figure 1. Schematic representation of the imec vision for c-Si solar cell technologies, indicating target thickness and efficiencies for large-area industrial-type c-Si solar cells.

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In order to realize such high efficiencies in very thin cells, engineers are facing challenges that have never been an issue before now. For example, doping profiles have to be controlled more precisely than is currently possible by diffusion, the prevailing approach in cell production today. Also, the lifetime of the minority carriers needs to be increased, calling for very efficient cleaning and handling methods to reduce metal contamination. Solar cell performance can be enhanced by replacing Ag by Cu, but this requires diffusion barriers that prevent the metal from diffusing into Si. Several processes in the technology toolbox of CMOS manufacturing are attractive ways to meet these stringent requirements. Obviously, this only makes sense when the technologies are compatible with the required low cost of ownership for photovoltaic applications. Below, we will give some more detailed examples of how the photovoltaic industry can benefit from the microelectronics experience and what is needed to further 'solarize' the CMOS toolbox – that is, adapt it to the needs of the PV community [4].

Ion implantation – road to better-controlled doping profiles

Si solar cells need a junction in order to operate and to collect electron-hole

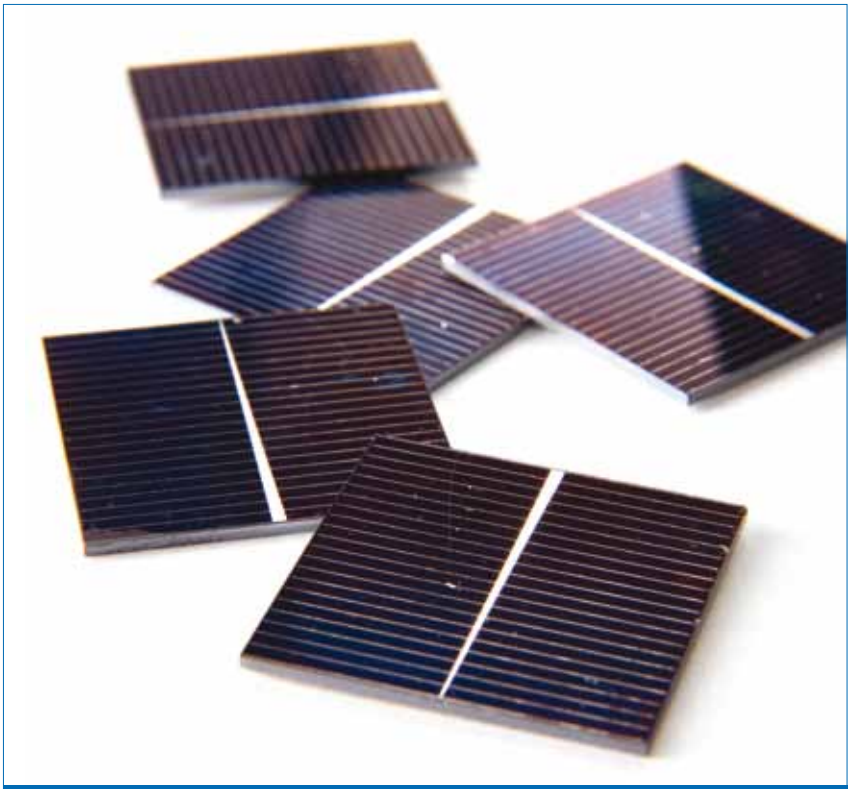

Figure 2. Imec's thin-film epitaxial Si solar cells – one of the pathways to working with very thin Si layers.

pairs. The resulting dopant profiles are tailored to enhance the cell performance. If the ultimate in cell performance is to be reached, the dimensions of these doping profiles need to be optimally controlled. For example, by better engineering the emitter profile, the UV response of the cell and its open-circuit voltage V_{oc} can be increased. Currently, dopants are introduced by diffusion, but this does not offer the required degree of precision. Ion implantation provides a possible alternative, as it yields an excellent areal uniformity and run-to-run producibility. Moreover, the design and integration of advanced profiles (e.g. very shallow emitters) is facilitated by the tool flexibility, and the design of back-contact solar cells can be significantly simplified. However, the tools developed for the IC industry have proved to be ill suited to reaching the required throughput of PV manufacturing lines (> 1500 wafers/hour). Therefore, the industry is now moving on to making new types of equipment that allow a higher throughput, but at the same time maintaining a sufficiently wide process window attuned to the specific profiles required by PV cells.

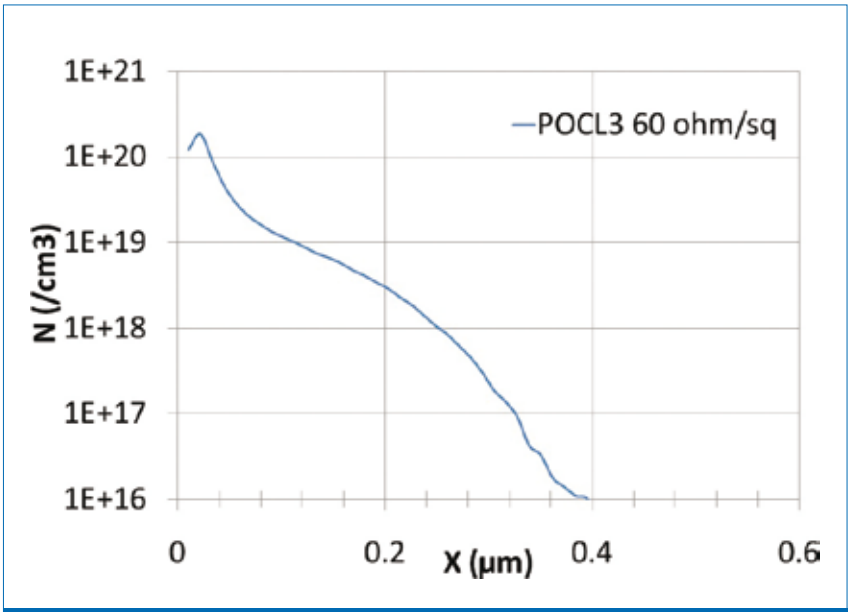

Figure 3. SIMS of a typical diffusion profile of a $POCL_3$ 60Ω/sq emitter.

It is in this context that imec has very recently developed an innovative process flow that consists of replacing the double-sided, high-temperature diffusion step taking around one hour, by a one-sided, low-temperature implantation step taking just a few seconds. This process flow was used to implant 160µm-thick *p*-type c-Si wafers with phosphorus. Next, the front side was passivated using a plasma-enhanced chemical vapour deposition (PECVD) SiN_yH_x layer. The dopants were electrically activated by a rapid thermal anneal step in a firing furnace. Wafers were then locally ablated on the rear side, metallized and fired to create the local back-surface field (BSF). The cells were metallized using a Cu-plating technique. The complete process resulted in an efficient solar cell with 18.8% efficiency, a V_{oc} of 638mV, a J_{sc} of 38.5mA/cm^2 and a fill factor of 76.6%. The implanted phosphor emitter had a sheet resistance of around 60Ω/sq. The innovativeness of the technique is the low-energy (10keV) implantation and short anneal step, creating shallow emitter profiles, but a major advantage, compared with traditional diffusion, is the reduction of the cycle time and the amounts of material and energy that are consumed. Techniques such as these will bring the industrialization of implantation for the solar industry one step closer [5].

Atomic layer deposition (ALD) of Al_2O_3 – a new option for surface passivation

For cells much thinner than 180µm, the influence of the non-illuminated side of the cell becomes increasingly important. Indeed, on this side, carriers can easily recombine due to the high number of surface defects. Traditional passivation schemes of Si solar cells are based on 'regular' dielectrics such as silicon-nitride (SiN_x), but these cell types do not have the potential to achieve efficiencies above 20%. For example, on *p*-type surfaces, SiN_x contains positive charges that attract minority carriers instead of repelling them. A next generation material for surface passivation of c-Si is ALD Al_2O_3, a dielectric with negative fixed charges [6]. At imec, know-how gained from semiconductor processing has been used in order to study the amount of charge in the dielectric layers and to understand the passivation mechanism. In addition to electrostatic-field-assisted passivation, ALD Al_2O_3 has the remarkable property of introducing very little interface carrier traps with Si. This chemical interface passivation was improved by the screening of several cleaning and drying methods derived from semiconductor processing. The cleaning cycle turned out to be one of the critical parameters

in achieving low surface recombination velocity values on large-area wafers. As a result, excellent recombination velocities (< 10cm/s) have already been demonstrated by ALD Al_2O_3 on the lab scale and are now being implemented in industrial-type solar cells.

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However, conventional time-resolved ALD is limited by its low deposition rate. The deposition reaction of this type of ALD is divided into two time-sequenced, self-limiting half reactions, each one being separated by a purge step to preserve a clean reaction chamber. It is clear that a faster and cost-effective ALD concept is needed in order to cope with the required low cost of ownership for PV. Therefore, several higher throughput pathways are under investigation and are now competing for market introduction. One of them is spatially separated ALD of Al_2O_3: instead of temporal separation of the half reactions, this ultra-fast ALD concept is based on a spatial separation. It makes purge steps obsolete and brings half-reaction timescales down to a few milliseconds. In this way, very high deposition rates are achieved, while maintaining the required high film quality. By using an experimental high-deposition-rate prototype ALD reactor based on the spatially separated ALD principle, imec was able to demonstrate that, on *p*-type CZ Si, 10 and 30nm spatial ALD Al_2O_3 layers can achieve the same level of surface passivation as equivalent temporal ALD Al_2O_3 layers [7].

Cu metallization – key to sustainable and efficient solar cells

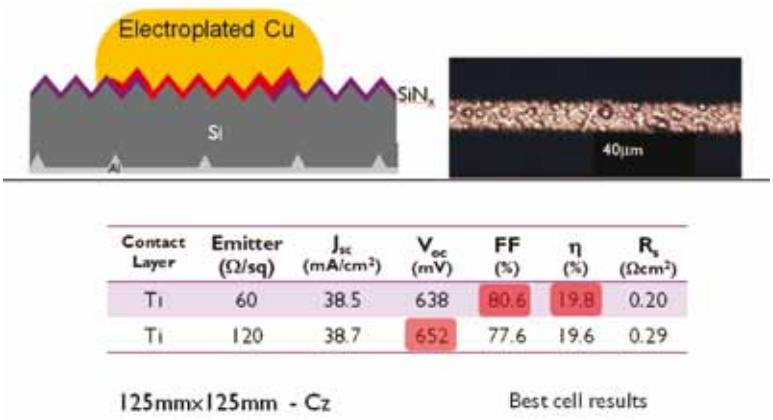
At the moment, the most widely used industrial method for making the top contacts of c-Si solar cells is screen printing of Ag pastes. But this technique is one of the limiting factors in moving towards lower costs and higher efficiencies. Being a contact metal, Ag is among the most material-intensive parts of a Si solar cell and today accounts for a large part of the cell's manufacturing cost. And this will only get worse: factoring in the increasing size of the PV market, experts predict a shortage of the scarce Ag within the next 10 years. A safe solution is to replace Ag by a conducting material that is not on the list of rare materials. The most likely candidate for this replacement is copper (Cu), a metal with a conductivity comparable to Ag. The preferred metallization scheme is the creation of laser-ablated via holes to open the passivation layer, and the subsequent deposition of Cu using electroplating, a technique that is well known in the metal industry.

Figure 4. Traditional surface passivation technique: in-line vacuum system for etching, and subsequent passivation by very high frequency PECVD of SiN.

Besides an obvious material-cost advantage, an electroplated Cu metallization scheme can lead to more efficient solar cells. Not only does the process reduce the shadowing losses (since narrower fingers – down to 40µm – with higher aspect ratios are possible) but it also improves J_{sc} and V_{oc}. Recently, imec was able to demonstrate large-area Cu-contact cells (170µm thick, 125 × 125mm^2) with efficiencies up to 19.8% and shadowing losses under 4% [8].

"Besides an obvious material-cost advantage, an electroplated Cu metallization scheme can lead to more efficient solar cells."

But the introduction of Cu equally brings along some challenges for the solar cell manufacturing engineer. First of all, Cu has a severe impact on the lifetime of Si, and therefore adequate barriers are necessary to prevent Cu from reaching the active Si region. Once again, we can rely on experience in microelectronics: several years ago, Cu was introduced as a replacement for Al in advanced interconnect integration schemes, mainly due to its lower resistivity. Several materials such as titanium nitride and tantalum nitride were investigated for



Contact Layer	Emitter (Ω/sq)	J_{sc} (mA/cm²)	V_{oc} (mV)	FF (%)	η (%)	R_s (Ωcm²)
Ti	60	38.5	638	80.6	19.8	0.20
Ti	120	38.7	652	77.6	19.6	0.29

125mmx125mm - Cz Best cell results

Figure 5. Cells with 40µm Cu front grid metal reach efficiencies approaching 20%.

use as an effective barrier layer against Cu diffusion, and the experience gained provided an interesting starting point for the integration of such barriers in a c-Si solar cell process flow. Another key question is the long-term reliability of Cu-based metallization. For example, unlike Ag, Cu oxidizes into a porous oxide when exposed to air. To address this issue, we can rely on the progress made with Cu in IC packaging and interconnection technologies such as, for example, Cu through Si vias (TSV) in 3D stacked integrated circuits.

… and many more

The knowledge and experience gained within the context of microelectronics are helping us to improve on doping profiles, surface passivation and contact metallization to make c-Si solar cells more efficient, cost effective and sustainable. However, this list from the processing technology toolbox is far from complete. In order to enhance the carrier lifetime, very efficient cleaning and handling methods are necessary in view of metal contamination. More precise patterning methods are required to cope with the ever more complex cell patterns. In the longer term, small optical features in the cell will probably be needed to enable more efficient light trapping. In addition, the toolbox contains a myriad of analytical tools and techniques that facilitate, for example, the study of the types of charges at the Al_2O_3 passivated surface, the characterization of the quality of the Si substrate, and an understanding of the degradation phenomena taking place in the solar cell.

'Solarizing' the microelectronics toolbox

All these examples illustrate that the microelectronics toolbox can be exploited to make highly efficient, thin, large-area solar cells. But the examples also highlight the fact that processes from CMOS manufacturing cannot simply be copied over to our PV lines. The throughput of techniques such as ion implantation and ALD is much too low, and the cost of most of these techniques is far too high, for use in the PV industry. So, if these tools are to be successfully introduced in the PV industry, adapted equipment and new processes must be developed that allow for an increased throughput and reduced tool costs. As discussed, we are witnessing the first steps in this direction. Moreover, the emergence in the PV field of many semiconductor equipment companies, also involving the above-mentioned non-conventional approaches, represents clear proof that the required low cost of ownership is achievable.

Imec and its partners are developing the c-Si solar cell technologies in an industrial affiliation programme. This programme aims to bring together established PV manufacturers, microelectronic companies wanting to exploit their semiconductor expertise in PV manufacturing, and newcomers from the energy sector. The technical content of the affiliation programme is oriented towards the development of process technologies for advanced crystalline Si solar cells and modules. The programme's goal is to deliver to imec's partners short learning cycles for the development of new processes so as to help the partners to be well placed in the race towards lower costs. Besides increasing the efficiency of industrial crystalline Si solar cells to greater than 20%, the programme also aims to improve the reliability of crystalline Si solar cell modules in order to guarantee lifetimes exceeding 20 years.

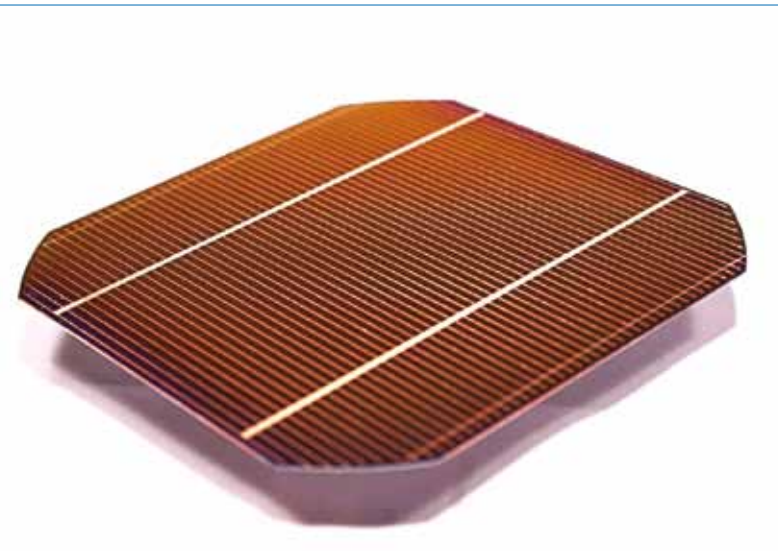


Figure 6. Imec's Cu-plated large-area Si solar cell.

Conclusion

We have given clear examples of how materials and process methods derived from IC manufacturing are improving the cost per Wp of c-Si solar cells. Ion implantation can be used instead of thermal diffusion to better engineer dopant profiles and lower the energy and material budget of the doping step. Al_2O_3 deposited by ALD is a likely candidate for passivating the surface of high-efficiency c-Si solar cells, and Cu as a top metal can boost the cells' efficiency and, at the same time, replace the rare and costly Ag. The first cells to be made using these new process steps look promising.

But, just as importantly, the IC-manufacturing processes cannot simply be copied over to our PV lines. Instead, they must be adapted to the benefit of the PV community by increasing their throughputs and lowering their costs. In this context, equipment manufacturers are supplying the first tools to the PV industry. We are convinced that this close association with microelectronics will play a significant role in achieving the cost and performance goals of solar cell manufacturing, in crossing the 1€/Wp barrier.

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