‘Less is more’: Ultrathin heterojunction cells offering industrial cost reduction and innovative module applications

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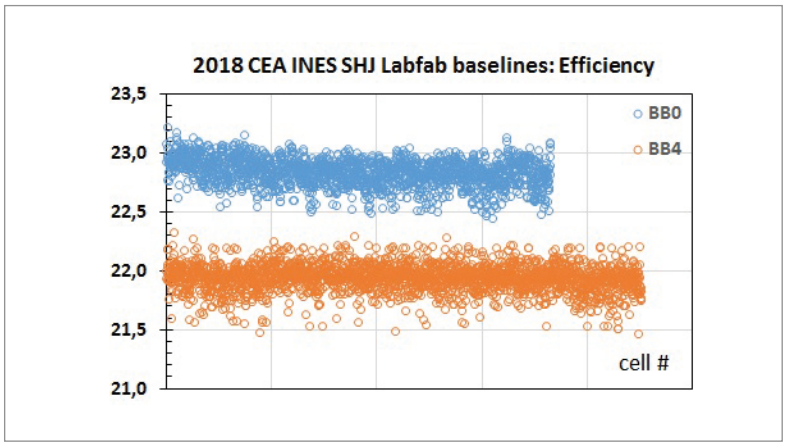
Abstract

Because of its symmetrical a-Si/c-Si/a-Si structure, silicon heterojunction (SHJ) cell technology offers the possibility to use much thinner wafers, and thus to reduce material and production cost. In order to evaluate the industrial feasibility of these thinner heterojunction cells, wafers from the standard thickness of 160µm down to 40µm were processed on the heterojunction pilot line at CEA-INES. It was found that no major modifications to the line were required to maintain stable cell performance down to a thickness of 80µm. For thicknesses below 80µm, wafers had to be processed in a semi-automatic/manual mode. The sweet spot in terms of cell performance, line compatibility and production cost was found at a thickness of around 90µm, roughly half that of the current mainstream thickness. These 90µm cells, with dimensions 156mm × 156mm, were then assembled into 60-cell modules, both glass–glass (bifacial) and glass–backsheet (monofacial) configurations, without changes to the interconnection and lamination process or to the bill of materials. A cell-to-module (CTM) performance above 99% was obtained, and the symbolic target of 1Wp per gram of silicon was reached. The thinner wafers also made it possible to manufacture ultralightweight (< 1kg/m²) and semi-flexible modules for product-integrated PV (PIPV).

Introduction

As now widely recognized, the amorphous/crystalline silicon heterojunction (a-Si:H/c-Si, SHJ) is one of the most attractive solar cell architectures, combining high performance and industrial compatibility. The low-temperature, high-throughput and cost-effective processes involved, the bifaciality, and the option of a rear-contact cell design are the competitive advantages of SHJ technology over other cell architectures [1,2]. Because of such advantages, an SHJ market is currently emerging, with a 5GW production capacity forecast in around 2020 [3]. The SHJ cell concept currently holds a world-record efficiency of 26.7% in its back-contact configuration [4].



The CEA-INES Labfab SHJ process baselines in 2018 for thousands of wafers with standard thickness. Busbarless cells average efficiency is 22.8% thanks to lower sensitivity to metal finger resistivity and less shadowing. Best cell at 23.8% on record process batch. The 2018 process baseline of four-busbar cells is 21.95% with best cell at 23.0% from record process batch.

CEA-INES has been exploring heterojunction cell technology for over 10 years, and an industrial pilot line has been in operation since 2011. The pilot line offers a turnaround time of <8h from as-cut wafers to electrical cell testing and sorting, at a nominal capacity of 2,400 wafers per hour, in combination with flexible R&D activities for each individual process step [5,6]. In 2016 and 2017, a hundred thousand wafers per year were fed into the pilot line to respond to industrial partner requests and to develop SHJ process know-how at CEA-INES. The production baseline performance during the first quarter of 2018 is shown in Fig. 1.

Work at the CEA-INES SHJ cell pilot line is complemented by an automated module pilot line to develop encapsulation and interconnection options. This notably includes bifacial modules and low-temperature cell interconnection options, such as the Meyer Burger SmartWire Connection Technology (SWCT) concept [7]. SWCT is especially suited to thinner cells, as the mechanical stress peaks generated on the cell are lower than in the case of standard ribbon interconnection. Moreover, SWCT is a redundant interconnection concept, with the impact of cell cracks on module power being lower. The module pilot line is supported by indoor testing facilities (climate chambers and mechanical test benches) and diagnostic tools for evaluating long-term module reliability, as well as by outdoor testing facilities [7].

This paper describes the work carried out on processing ultrathin (70–100µm) 156mm × 156mm wafers. The goals are twofold: 1) to reduce cell production costs; and 2) to enable innovative module designs, such as lightweight modules, either flexible

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or rigid in nature. The need for cost reduction is driven by the fact that current wafer production costs (including material and sawing) still represent as much as 35% of the total costs of an industrial PV module [3].

The second goal, relating to innovative module architectures, is driven by the PV application potential in areas such as aerospace, vehicles, boats or building integration, where non-planar shapes and weight reduction (including that of the cells) can be a key requirement. Figs. 2 and 3 show examples of such lightweight modules integrated in unmanned aerial vehicles for observation and telecommunication. In these two particular cases, the targeted module weight is less than 700g/m², in contrast to the weight of 12kg/m² for standard glass–backsheet modules, and to the weight of standard 180µm silicon cells, which already amounts to 450g/m².

The potential for reducing the thickness of the SHJ cell is based on some of the following key characteristics. The SHJ cell design is symmetrical with respect to the front and back sides (see Fig. 4), and all steps of the cell and module process operate at moderate temperatures below 250°C (compared with about 800°C for most other cell designs). This makes the cell much less sensitive to bowing/warping during cell metallization, which are bothersome phenomena for thin wafers [8]. Most importantly, surface recombination mechanisms generally become more important as wafer thickness is reduced. Here, the SHJ cell offers a competitive advantage over other cell designs, as the thin a-Si layer provides an outstanding surface passivation of the c-Si. Thinning the wafer leads to enhanced electron–hole pair generation as well as to reduced recombination in the c-Si bulk, effectively resulting in an increase in open-circuit voltage V_{oc}, as will be demonstrated in the following sections.

In the following discussion, the way in which the cell production process of the pilot line has been adapted to deal with wafers of thicknesses down to 40µm will be described. Standard wafers from three different commercial suppliers were used; for evaluation purposes, these wafers were chemically thinned. It will be demonstrated how the mechanical and electro-optical characteristics of SHJ cells appear better suited to cell thinning than other cell architectures. The key process steps for the module assembly of these thin cells will be discussed,

Figure 2. A solar-powered drone co-developed by CEA-INES, commercialized by SUNBIRDS in 2017. The PV module weighs 640g/m².

Figure 3. Artist's impression of STRATOBUS, the solar-powered high-altitude pseudo-satellite (HAPS) under development by Thales Alenia Space, with industrialization foreseen in 2020.

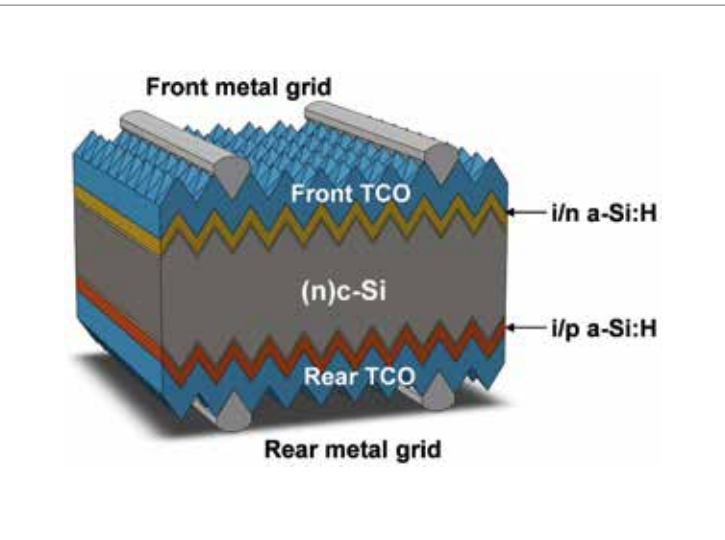


Figure 4. The symmetrical bifacial structure of the silicon heterojunction (SHJ) cell.

and some prototypes presented. Finally, it will be indicated how these characteristics contribute to an overall cost reduction when an optimal cell thickness of around 90µm is chosen.

Dealing with thin wafers in an SHJ cell production environment

The CEA-INES 'LabFab' pilot line has a standard capability of producing 130 to 160µm SHJ cells at a processing rate of 2,400 wafers/hour. The global breakage rate on the line is well below 1.5% for this standard thickness. The breakage rate as a function of wafer thickness has been monitored along the whole process chain (Fig. 5), revealing wafer automation (transfer/load/unload) during deposition and metallization to be the main cause of breakage [9]. Wafer flexion tests demonstrate that thin wafers are initially no more fragile than the reference wafers (Fig. 6). An initial integration with standard line settings has allowed an identification of the main issues for the production of thin wafers on the SHJ production line. The significant increase in breakage rate below 100µm appeared to be mostly related to the handling between deposition chambers and cassettes, the wafer stiction during wet processing, and the metallization screen printing.

Several line adjustments have been performed to reduce breakage rate and global cell defectivity. This iterative line optimization includes automation tuning

No breakages were observed during *I–V* testing or sorting, for either busbarless or 4BB cells on wafers >60µm. With these straightforward line adjustments, a reduction in the total line breakage rate was obtained during 2017 (Fig. 7). Although line throughput is currently affected for wafers <100µm (slower wafer robotics, fewer wafers per carrier), processing of wafers down to 80µm could be maintained at nominal throughput using simple modifications of cassettes or pickers. On the other hand, for thicknesses below 70µm the current production line and equipment would require major upgrades (such as single-side wet etch and cleaning tools, and new transfer systems) to maintain a high throughput and a low breakage rate. Cells have therefore been processed from 70 to 40µm wafers in a semi-automated/manual mode.

SHJ cell performance for thicknesses down to 40µm

Sets of wafers with different thicknesses down to 90µm were processed with no modification of the current production flow. As an illustration, Fig. 8 shows the effect of wafer thickness on the increase in the number of wafers obtained from an ingot, compared with the 160µm reference thickness: at a wafer thickness of 90µm there is a 40% increase in the number of wafers. With the cost of silicon material contributing 24% to the final module costs [3], a reduction of 10% in module cost for 90µm wafers is implied.

Results for one batch of 4BB bifacial cells are

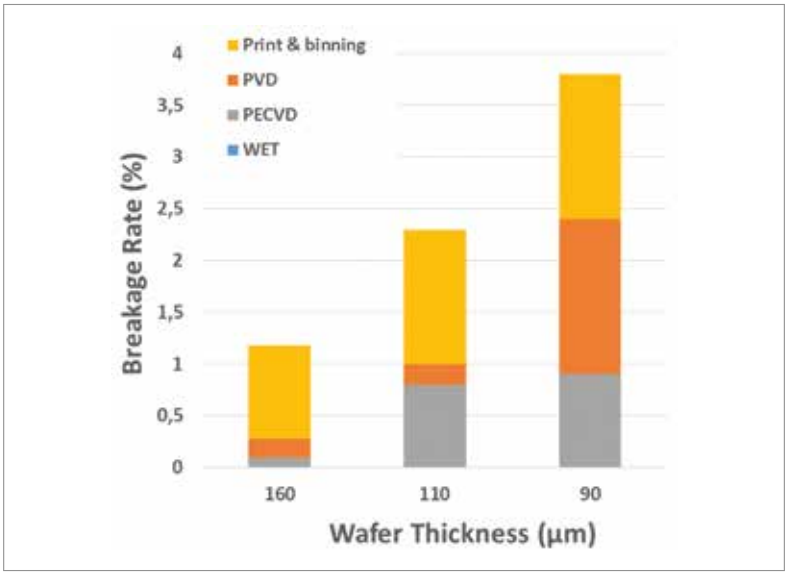


Figure 5. Impact of wafer thickness on breakage rate (without modification of the current production flow).

Figure 6. Flexibility of a 60µm SHJ bifacial cell (156mm × 156mm).

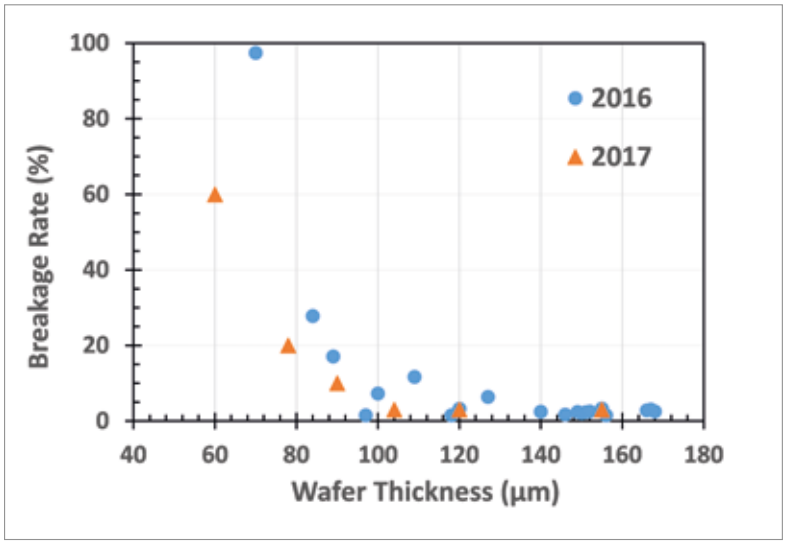


Figure 7. Improved breakage rate with specific line adjustments.

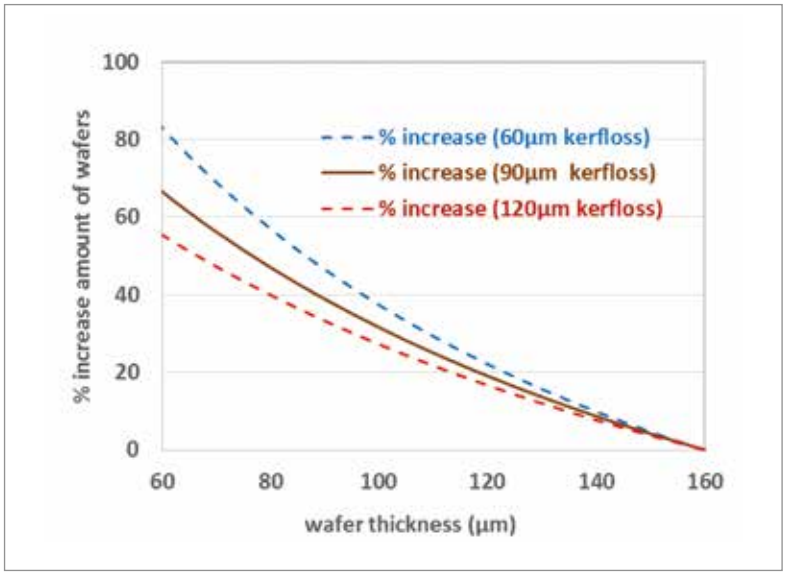


Figure 8. Increase in the number of wafers from an ingot as a function of wafer thickness, for three different values of kerf loss.

presented in Fig. 9. For cell thicknesses ranging between 160µm and 90µm, the final cell efficiency remains approximately the same. For all the batches, with a typical size of 30 to 200 wafers, it was noticed that record efficiencies in the 90–100µm range are very close to those for the reference wafers at 160µm, namely 22.1% versus 22.3%, proving the compatibility of such thin wafers with very high efficiencies. Average efficiency is more affected than record efficiency, which implies that process defectivity is slightly higher for the thinner wafers. This defectivity seems not to be due to handling-related wafer damage, but rather to wafer misalignment during PVD TCO deposition, causing edge isolation issues (i.e. shunts), as shown in Fig. 10.

The good overall efficiency performance of the thin cells is mostly due to the increase in V_{oc} for thinner cells, as shown in Fig. 11. This V_{oc} gain is in turn due to the outstanding surface passivation of the c-Si wafer by the a-Si layers. This wafer thinning, however, comes at the expense of a lower short-circuit current (I_{sc}), attributed to reduced photon absorption in the infrared (IR) region of the solar spectrum. In practice, the gain in V_{oc} does in fact almost offset the loss in for wafers below 100µm, which is represented in Fig. 12. The IR response of thin cells can be increased by specifically optimizing the electro-optical properties of the rear TCO layer in order to improve internal reflection and IR light trapping [10]. Other options for optimizing the cell current, such as the use of a back reflector at the cell rear side or a module with a white reflective backsheet, would be at the expense of bifaciality.

Figs. 10, 11 and 12 show the results for three different wafer providers, used to evaluate the impact of the incoming wafer quality/purity. Fig. 12 shows how these three wafer qualities have a similar J_{sc} loss behaviour of around 0.01mA/cm² per micron thickness. Interestingly, Fig. 11 reveals that the lower

wafer quality of provider 3, with the lowest V_{oc} at 160µm thickness, is seen to improve the most with wafer thinning, achieving a V_{oc} at around 90µm thickness, which is similar to that obtained with the higher wafer quality counterparts. A transition to thinner wafers would therefore allow the use of lower-quality wafers, and thus offer an additional reduction in wafer cost.

Finally, the feasibility of integrating wafers of thicknesses down to 40µm was evaluated on the pilot line; the results are given in Fig. 13 and Table 1. Wafers below 80µm were processed on the line operated in a semi-automatic mode with manual loading, unloading and *I–V* testing to avoid breakage by the wafer-transfer conveyor used in the automatic mode. On the other hand, this manual handling introduces additional defectivity issues. The current pilot line encounters its limits at a wafer thickness of 40µm, at which point the breakage rate rapidly approaches 100%.

Module assembly of thin SHJ cells

The feasibility of a module assembly incorporating 90µm SHJ cells was evaluated on the module pilot line at CEA-INES. Full-size 60-cell modules and 4-cell mini-modules were fabricated; these included monofacial (glass–backsheet) and bifacial (glass–glass) module designs, using ribbons or SmartWire technology as cell interconnection. The module assembly was performed without any changes to the standard bill of materials (BOM) used for the assembly of 160µm cells. An industrial laminator was used for cell encapsulation, as well as an industrial tabber/stringer for the ribbon interconnection using conductive adhesives (ECA). The electroluminescence (EL) images in Fig. 14 reveal defect-free modules after lamination and subsequent thermal cycling in accordance with IEC 61215. The power loss of these modules after the 200 thermal cycles is shown in Fig. 15 and appears to be less than 3%, well below the 5% criterion of the IEC 61215 certification standard.

On the basis of these encouraging results for 4-cell mini-modules, full-size 60-cell modules were assembled, for both glass–backsheet (monofacial) and glass–glass (bifacial) architectures. The EL image and performance of an example of a 60-cell glass–backsheet module is shown in Fig. 16: the module features a cell-to-module (CTM) ratio of 99.1% and a very low massic module power (Wp per gram of silicon), achieving the symbolic target of 1Wp/g Si.

Another example, given in Fig. 17, shows a 24-cell module assembled with 115µm-thick SHJ cells and intended for semi-flexible applications on a stratospheric airship (or HAPS: high-altitude pseudo-satellite) for telecommunication, under development by Thales Alenia Space. The module efficiency is 18% and the power loss is less than 5% after 500 thermal cycles. The thin cells also contribute to the very low specific weight of only 600g/m², which allows a higher effective payload of the airship.

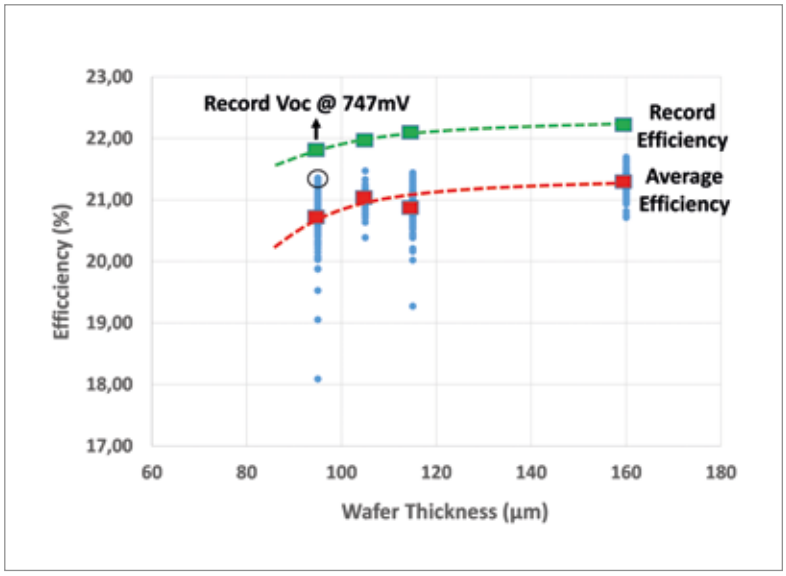


Figure 9. Impact of cell thickness on efficiency, for one batch of wafers based on 2016 process of reference.

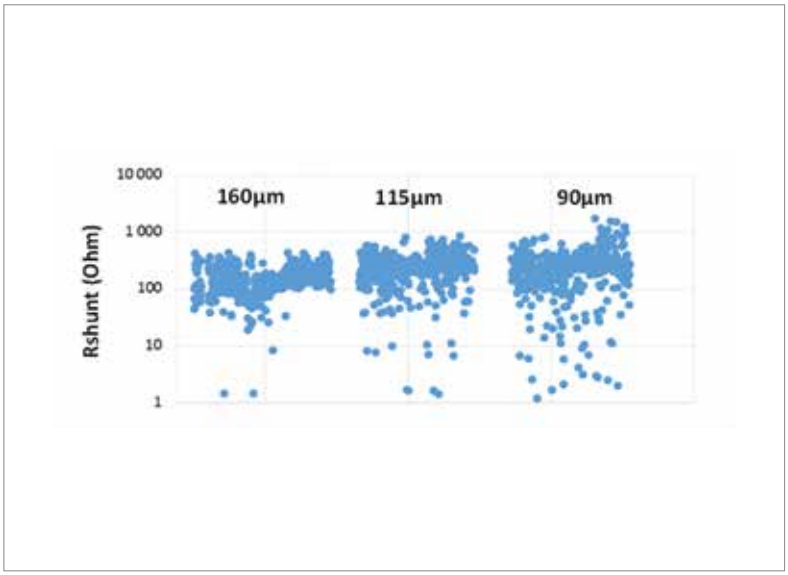


Figure 10. Dispersion in shunt resistance (R_{sh}) increases below 90µm wafer thickness.

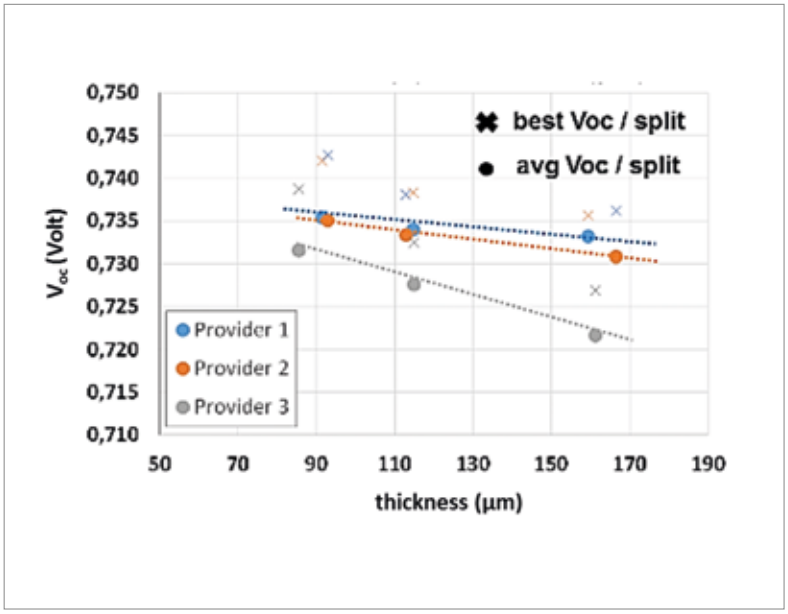


Figure 11. Impact of wafer thickness on V_{oc} for three wafer providers.

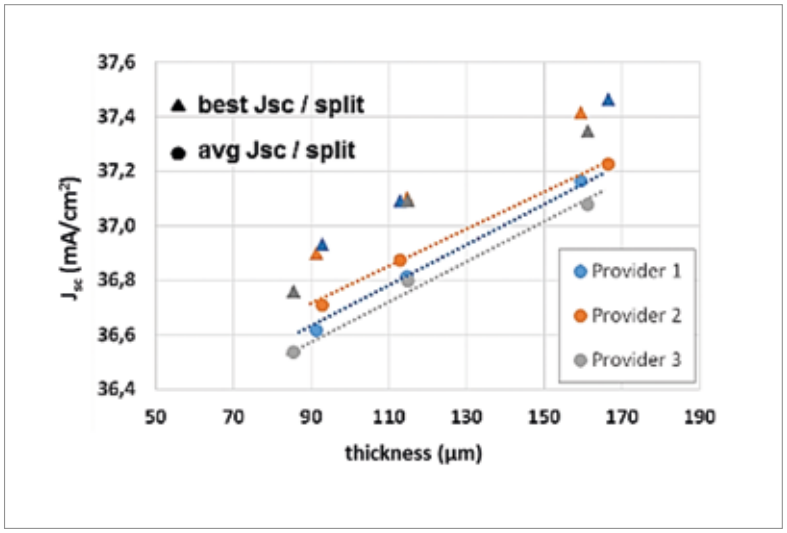


Figure 12. Impact of wafer thickness on short-circuit current density (J_{sc}) for three wafer providers.

"The optimal cell thickness was estimated between 90µm and 100µm."

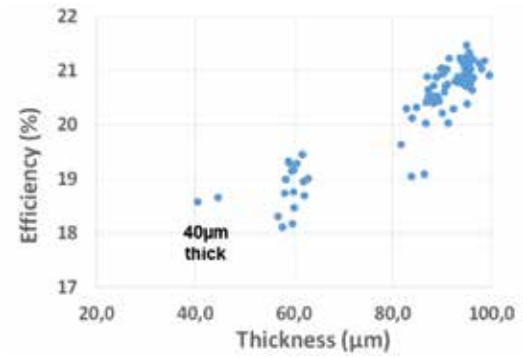
Cost considerations

The potential cost reduction thanks to the use of thinner wafers in an SHJ industrial production line (80MW nameplate capacity, 4BB cell configuration) was evaluated using an internal cost model similar to that given in Louwen et al. [11]. On the basis of the current pilot line results obtained, the optimal cell thickness was estimated between 90µm and 100µm (Fig. 18). For even thinner wafers, the main challenges for the future are the likely decrease in efficiency and increase in breakage rate, which might no longer be offset by the lower substrate costs.

Complementary to these cost considerations versus wafer thickness, it is interesting to note that analytical calculations of cell performance as a function of thickness also gave an optimal value of around 100µm, as illustrated in Fig. 19 [12]. These calculations were based on a similar approach to that reported in Richter et al. [13], but with additional defect-induced recombination mechanisms and using characteristic values for recombination and resistivity of the SHJ cells, as measured on the CEA-INES pilot line.

Conclusion and outlook

The industrial compatibility of thinner wafers for the manufacturing of heterojunction cells has been demonstrated down to a thickness of 80µm and even further, down to 40µm, on the semi-industrial LabFab pilot line at CEA-INES; at 90µm thickness, an average cell efficiency of 20.8% has been achieved, with a record efficiency of 22.1%. The optimal thickness range, with respect to performance, production cost and compatibility with the current pilot line layout, was identified



Thickness [µm]	J_{sc} [mA/cm²]	V_{oc} [mV]	*FF* [%]	η [%]
40	34.7	730	73.3	18.6
45	35.1	732	72.7	18.7

Figure 13. SHJ cell efficiencies obtained for ultrathin wafers of thicknesses down to 40µm, fully processed on the CEA-INES pilot line based on a 2016 process of reference

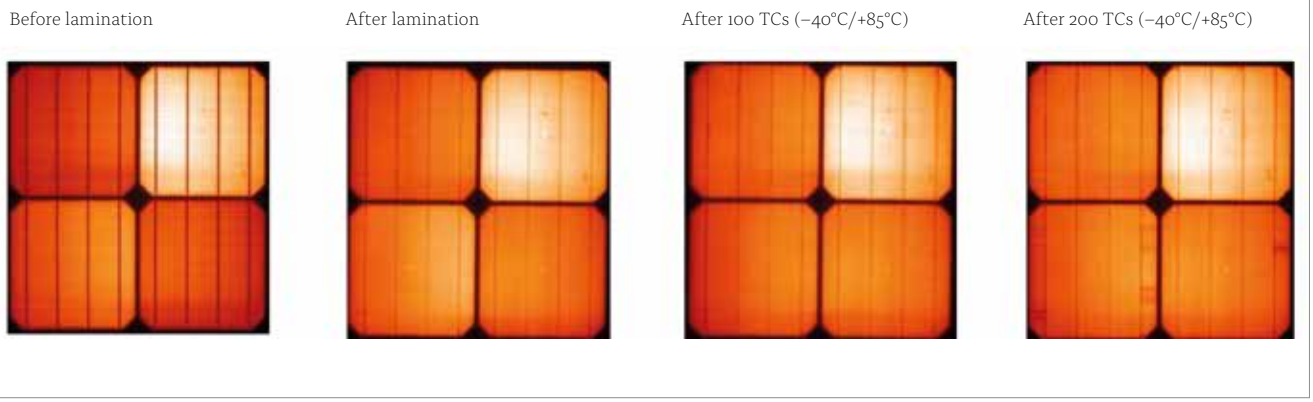


Figure 14. EL inspection of 4-cell glass–backsheet mini-modules with 110µm SHJ cells, after lamination and IEC thermal cycling (100 and 200 thermal cycles).

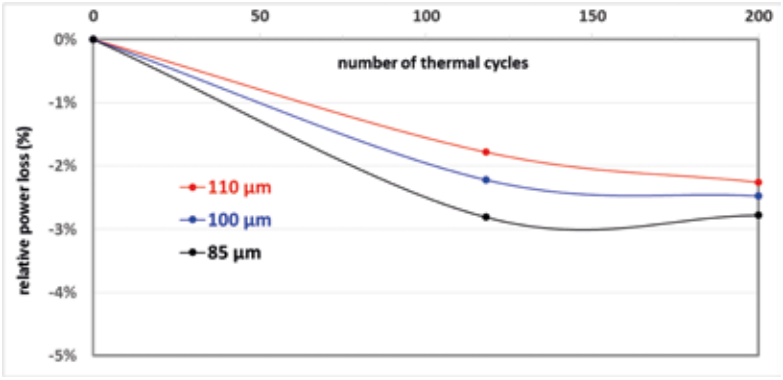
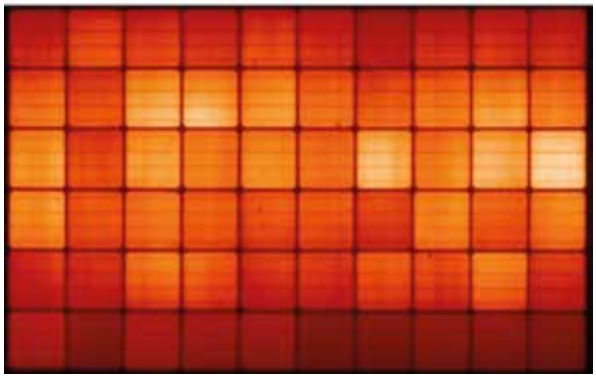


Figure 15. Relative power loss during 200 thermal cycles of SHJ glass–backsheet modules with cell thicknesses of 110, 100 and 85µm.



Thickness [µm]	P_{mpp} [W]	I_{sc} [A]	V_{oc} [V]	*FF* [%]
Total cells	315.6	8.8	44.3	80.1
Module	312.7	9.1	44.2	77.8
CTM	99.1%	103.2%	99.8%	97.1%

Figure 16. EL image and performance of a 60-cell glass–backsheet module with 93µm cells, yielding a massic module power of 0.98Wp per gram of Si.

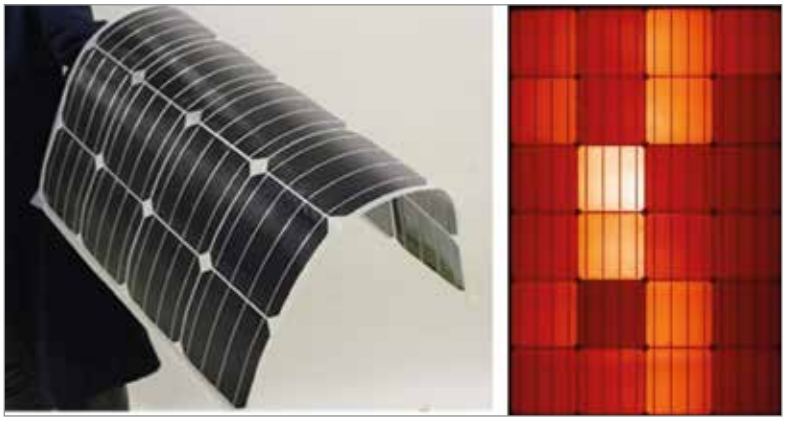


Figure 17. A 24-cell semi-flexible module incorporating 115µm SHJ cells, for the Thales Alenia Space HAPS application.

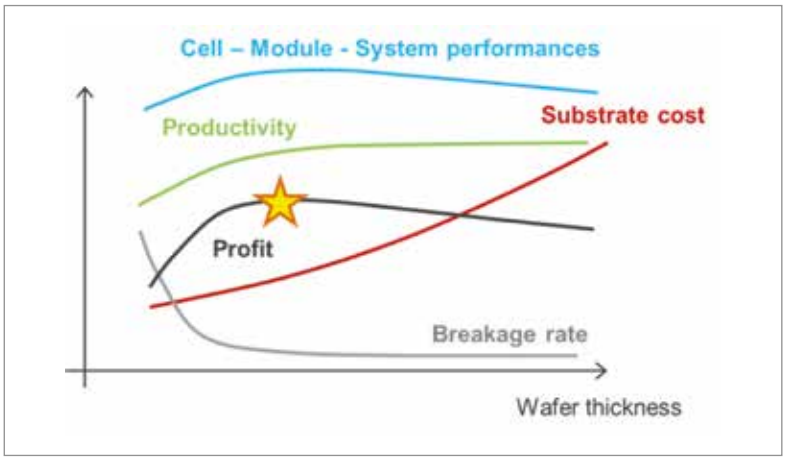


Figure 18. Cost, productivity and performance trends in reducing wafer thickness. The optimum thickness is estimated to be in the 90–100µm range for maximizing the final product earnings before interest and taxes (EBIT).

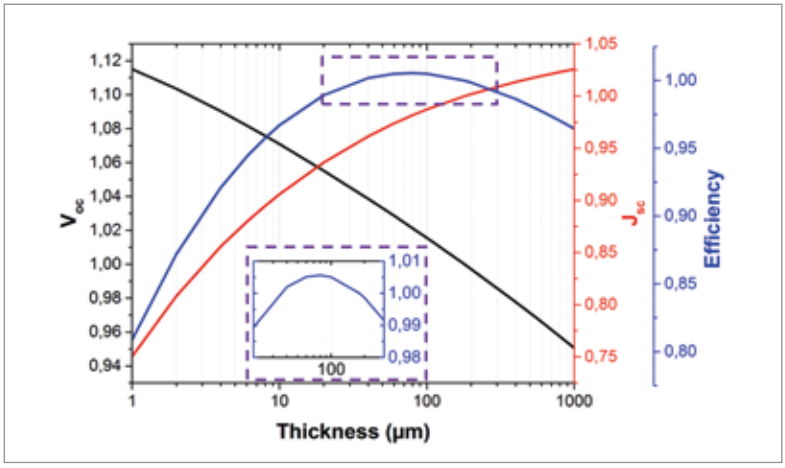


Figure 19. Simulated performance (V_{oc} in black, J_{sc} in red, efficiency in blue) of SHJ solar cells as a function of thickness. Values are given relative to those for 180µm thickness. The inset shows the simulated SHJ cell efficiency in the range 20 to 300µm. [13].

to be around 95µm. Modules incorporating these thin 95µm cells were successfully assembled, which allows a leveraging of the reduced mass and increased flexibility of these cells, targeting lightweight or semi-flexible module applications. Module performance measurements and reliability testing yielded CTM ratios beyond 99%, a massic output of 1Wp per gram of silicon, and full compliance with IEC certification standards during thermal cycling tests. It was found that a stable high efficiency for thin cells sets higher standards in process control of the production line (defectivity, monitoring, etc.).

Ultrathin heterojunction cells offer industrial cost reduction, high performance and innovative module applications, ultimately demonstrating that 'less is more'.

Acknowledgements

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Eric Gerritsen studied physics at Twente University (Netherlands) before joining Philips Research Labs (Eindhoven, NL) in 1985 to work on ion implantation, for which he received his Ph.D. from Groningen University in 1990. He then held various positions at Philips (Lighting, Semiconductors) in Germany, The Netherlands and France, before joining CEA-INES in 2008 to work on PV module technology and applications.

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Dr Charles Roux is the Head of the Silicon Heterojunction Cell Laboratory at CEA-INES and joined CEA in 2009. He contributed to the start-up of the CEA Heterojunction Labfab pilot line. He has built his expertise in industrial processes and technology transfer for the PV and semiconductor industries at Applied Materials in France and in Spain from 2000 to 2009 after a thesis on II-VI semiconductors. Since then, he has performed various audit missions of industrial PV manufacturing sites.

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