Texture etching technologies for diamond-wire-sawn mc-Si solar cells

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Abstract

Texturing approaches for diamond-wire-sawn multicrystalline silicon (mc-Si) wafers represent a very active and important R&D field in solar cell manufacturing. Diamond-wire sawing (DWS) of mc-Si wafers demands new approaches for the texturization, as this type of cutting leaves a relatively smooth surface, which poses a significant challenge for texturing using standard acidic texturing methods. Many equipment manufacturers have been working on solutions to prepare mc-Si for DWS by using different dry- and wet-chemical-based approaches. Some of these approaches create a nanotextured surface, often called *black silicon*, which necessitates further adaptations of subsequent processing steps, such as emitter diffusion, passivation and metallization. This paper describes the most common texturing methods, and lists the currently available commercial solutions from equipment suppliers.

Introduction

Optical confinement is essential in order to increase the amount of photogeneration in a crystalline silicon (c-Si) solar cell. Especially in conventionally textured multicrystalline silicon (mc-Si) solar cells, the highly reflecting surface is one of the major limiting factors causing reduced short-circuit current density (J_{sc}) of the solar cell. Additionally, the switch from standard multiwire slurry sawing (MWSS) to diamond-wire sawing (DWS) for mc-Si wafers calls for new approaches for the texturization of the wafer surface during solar cell processing. DWS itself has the potential to almost halve the wafer-manufacturing cost for mc-Si wafers (Fig. 1).

"DWS leaves a relatively smooth surface, which presents significant challenges with regard to texturing using standard acidic texturing approaches."

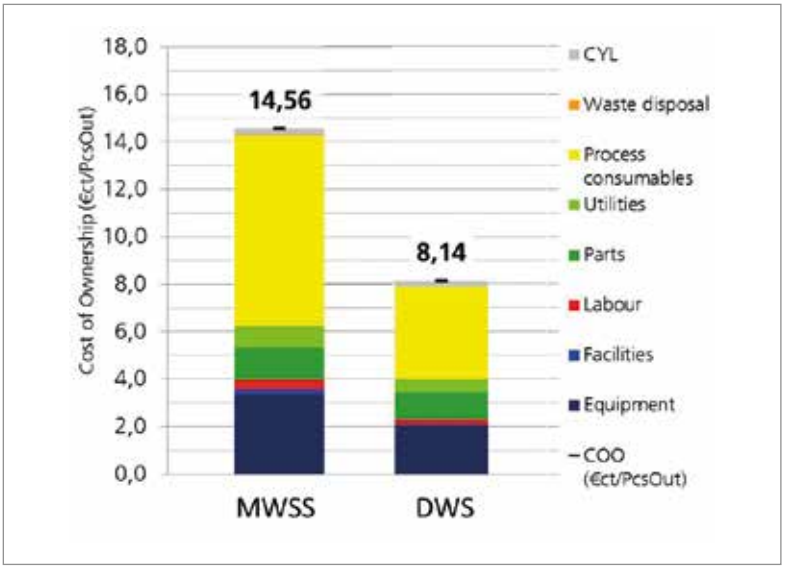


Figure 1. Total cost of ownership (TCO) comparison of MWSS and DWS approaches for cutting mc-Si wafers.

The DWS process is faster than the slurry method and silicon kerf loss is lower; moreover, its operational costs are dramatically lower, because the fixed abrasive principle frees wafering fabs from expensive and complex slurry use and management. The DWS approach has nearly completely replaced the traditional slurry cutting for monocrystalline silicon wafers, whereas for mc-Si only about 5% of the manufacturers were using DWS as of 2016, according to the International Roadmap for Photovoltaics (ITRPV) [1]. The relatively slow introduction of DWS for mc-Si is due to the fact that DWS leaves a relatively smooth surface, which presents significant challenges with regard to texturing using standard acidic texturing approaches.

Many equipment manufacturers have been working on solutions to make mc-Si ready for DWS by using different dry- and wet-chemical-based approaches, the most prominent and commercially viable solutions being:

- Acidic texturing with additives
- Standard acidic texturing with pretreatment
- Metal-assisted etching (MAE) or metal catalyst chemical etching (MCCE)
- Reactive ion etching (RIE)
- Atmospheric dry etching (ADE)
- Laser texturing

Many of the currently developed texturing approaches claim to produce a 'black-silicon' surface, where *black silicon* refers to silicon surfaces covered by a layer of submicron structures. Black silicon helps to reduce reflectance in different ways, depending on the size and shape of its surface texture. First, there is a reduction in reflection because of a multitude of interactions of light with the textured surface. Second, when the size of the texture features is large compared with the wavelength of the solar spectrum, surface scattering is responsible for an elongated light path and enhanced absorption. Third, for sub-100nm nanostructured silicon, the surface feature

sizes are so small that the surface essentially acts as an effective index medium and is optically flat.

Because of the nature of black-silicon-textured surfaces, adaptations of the subsequent processing steps – such as emitter diffusion, passivation and metallization – become necessary.

Overview of commercial wet-texturing solutions

The wet texturing of mc-Si is a standard process in solar cell manufacturing, most commonly carried out within inline wet-chemical equipment. The traditional HF/HNO_3 texturing solutions, with either a HF-rich or a HNO_3-rich composition, use the saw damage from the slurry sawing to etch deep into surface defects initially, and then to widen the resulting holes. As previously mentioned, DWS wafers do not have such deep damage, and therefore the DWS wafers etched in $HF/HNO_3/H_2O$ remain smooth and the sawing grooves are still visible as lines.

Adapted standard acidic texturing solutions

The simplest approach to adapting existing HF/HNO_3 texturing solutions for DWS of wafers is the use of additives in the texturing solution. Cell manufacturers would easily be able to implement these solutions within their existing tool set-ups, without major additional investment.

The company RENA claims to have already sold a couple of GWs of its adapted metal-free chemistry based on standard HF/HNO_3 etching solutions. No specific information about this solution has been released so far [2]; however, the additive solution allows inline processing with footprints similar to those of conventional acidic texturing tools.

The LINEX inline system developed by Singulus incorporates a texturing process that removes the saw marks made by the diamond wire on the wafers when cut. The innovation is a two-step process using new additives and ozone for post-cleaning to create a homogeneous structure [3]. Singulus has also developed a new conveyor system within its LINEX inline processing tool; the company says that this innovation guarantees 'extra-gentle' handling of the multi wafers, thereby delivering a marked reduction in breakages. Unlike mono wafers, multi wafers can become fragile when sawn, leading to problems with texturing.

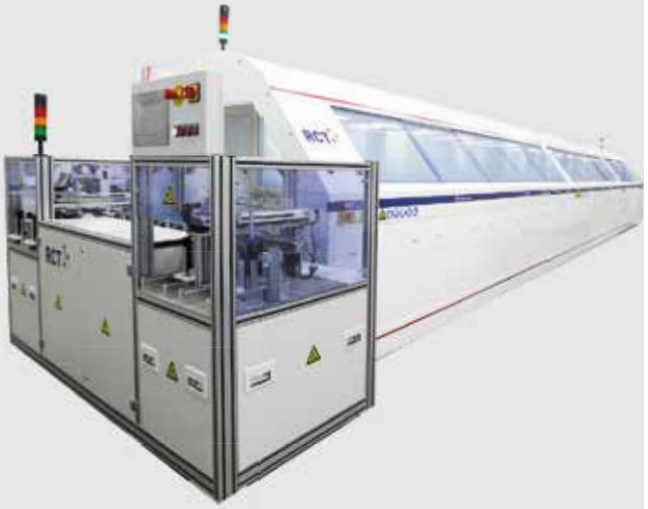
Another possibility for texturing smooth surfaces is a solution consisting of HF/HNO_3 and sulphuric acid (H_2SO_4) developed by Fraunhofer ISE. The favourable texturing behaviour of this solution as opposed to HF/HNO_3 might be due to the high viscosity of the sulphuric acid. For $HF/HNO_3/H_2SO_4$ mixtures, the process temperature plays an important role in controlling the etch depth and the reflection. At temperatures above 45°C, it is possible to achieve a texture with total reflection values of 22% at 600nm, a total etch depth of 15µm in 60s, and a structure height of 2µm (see Fig. 2). This result represents a promising starting point for finding an adequate additive for the mc-Si DWS texturing process (further results to be published soon).

The Technology Company

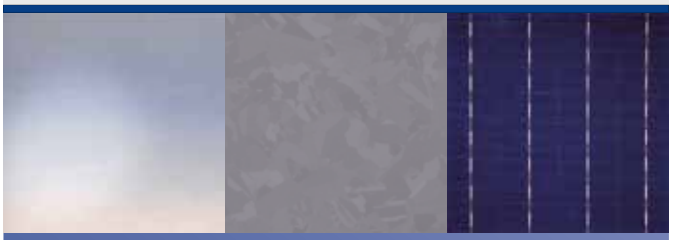
RCT solutions

Black Silicon

Inline processing for DWS multi wafers



- Lowest COO in industry
- no additive cost
- Max. module power guaranteed by high Voc and FF
- also available as upgrade tool to existing inline texturing tools



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A slightly different approach has been developed by the company Schmid: instead of using additives for the actual HF/HNO_3-based texturing process, Schmid has implemented a pretreatment step with the aim of generating micro-defects at the silicon surface in order to enable subsequent conventional acidic texturization. The preconditioning procedure, called *DW PreTex*, is a simple one-step process implemented before multicrystalline wafers are textured [4].

Metal catalyst chemical etching (MCCE)

Silicon can be etched in the presence of HF and an oxidative agent, catalysed by noble metals, to form micro- or nanostructured surfaces with various morphologies [5]. In a typical etching process, the silicon substrate is partly covered by noble metal nanoparticles and immersed in a solution of HF and an oxidative agent [6–8]. For the noble metals, gold (Au) and silver (Ag) are the most popular candidates; upon attachment to the silicon substrate, noble metal ions acquire electrons from the silicon valence band and are reduced to form seed nuclei which develop into nanoparticles. Concurrently, these ions inject holes underneath the silicon, causing oxidation into SiO or SiO_2, which are then removed by HF (see Fig. 3) [6].

As a result of the continuous formation of silicon oxide underneath the metal particles and the corresponding removal action by the HF, the metal particles sink into the silicon and create porous structures. Once the desired surface structures have been created, the metal nanoparticles are removed by another etchant – such as HNO_3 – and a cleaning process then follows.

A generic process flow for metal catalyst chemical etching (MCCE) of a crystalline silicon wafer is given in Fig. 4 [9]; all the relevant steps necessary for processing a wafer from an as-cut state to readiness for emitter diffusions are included. The saw damage after wafering needs to be removed (about 3 to 5µm); this can be performed as a separate process step or during the MCCE. Since the MCCE is a process in which a metal is used as a catalyst in order to promote etching in the vicinity of the metal, the respective metal precipitates need to be deposited, e.g. Ag nanoparticles. Metal nanoparticle deposition is carried out by dipping the wafer into a wet-chemical solution containing metal ions, which is in most cases a solution of $AgNO_3$. Additionally, HF needs to be present to initiate the deposition.

After metal deposition, the texturing process begins, which requires an oxidant (e.g. H_2O_2 or HNO_3) and HF. Depending on the bath composition, a porous Si layer can be formed. The surface morphologies can also vary (Fig. 5): as an example, a pit-like structure can be obtained, with typical diameters in the range 50 to 200nm, with depths in a similar range. In addition, alternative structures, such as nanowires or pores, can be created. Such structures can lead to low reflectivity; however, their use in solar cells is not ideal (as they are deep and steep structures, with high surface enlargement and challenges for good surface passivation, including low J_{oe}). Therefore, post-treatments are optionally carried out (either alkaline or acidic) in order to determine an optimum structure for superior solar cell performance; this optimized structure is a trade-off between low reflectivity (necessary for high J_{sc}) and reduced surface enlargement (necessary for high V_{oc} and fill factor *FF*). In addition, the wafer

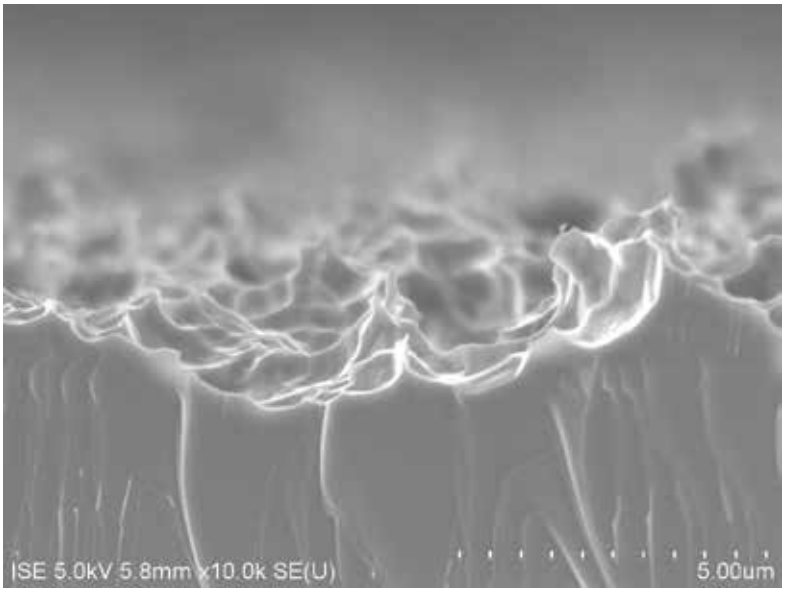

Figure 2. Scanning electron microscope (SEM) image of an mc-Si DWS wafer textured in HF, HNO_3 and H_2SO_4.

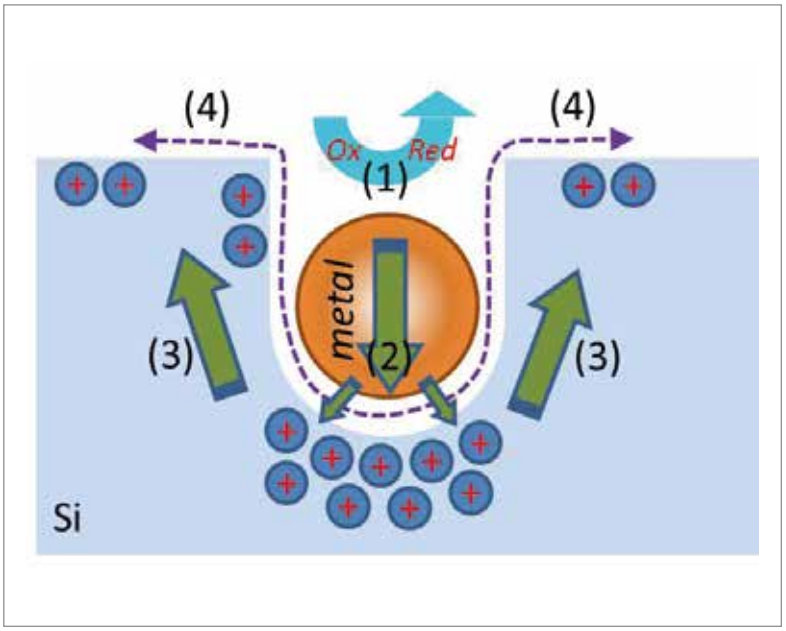

Figure 3. Illustration of the metal catalyst chemical etching process: (1) reduction of an oxidative agent (such as H_2O_2) catalysed by a noble metal particle; (2) injection of holes generated during the reduction reaction into the silicon substrate, with the highest hole concentration underneath the metal particle; (3) migration of holes to silicon sidewalls and surfaces; and (4) removal of oxidized silicon via HF [6].

surface needs to be cleaned of any metal and contaminations prior to emitter diffusion.

In the field of MCCE, Advanced Silicon Group (ASG) uses a version of metal-enhanced etching of silicon, a process that can be run on modified standard wet benches. ASG has innovated changes to the standard MCCE process to make it more uniform and repeatable, and also to allow control over the nanotexture geometry. Furthermore, since a novel material requires a new device design to make use of the material's unique properties, ASG has made alterations to the device design to obtain improved performance and lower cost. The cost of the technology per wafer is comparable to that of standard mc-Si texturing, and ASG has so far seen efficiency gains between 0.5 and 1.5%$_{abs.}$, depending on the starting process. With these efficiency gains, the price per watt is lower than that for standard texturing; this is in addition to the materials cost savings made possible by the use of diamond-wire-sawn wafers, which the process accommodates. ASG offers consulting to help companies optimize their cell process using black silicon, and then provides a licence to manufacture cells using the improved process.

Another supplier in the MCCE field is the company RCT solutions, who has called its product *i-BlackTex*. The tool on offer accomplishes the entire surface treatment – saw damage removal, texturization and cleaning – in a single inline system. As in the case of the other MCCE processes, RCT employs silver nitrate as the metal, but avoids the use of any additives or H_2O_2. The system employs standard chemicals that are typically used in the texturing process – HF, HNO_3, water and KOH for cleaning. Another important feature of the system is its length of 12m, which is the same as the well-known branded texturing wet benches, and therefore allows easy replacement. The process can be adjusted to obtain reflectivities between 12 and 20%. The lower reflectivity, however, entails additional attention within the solar cell process – especially for emitter formation and passivation (see below) – to harvest the full benefit. RCT affirms an efficiency gain of 0.2 to 0.4%$_{abs.}$ at the cell level over standard mc-Si cells.

MCCE represents a very attractive solution for the texturization of DWS mc-Si wafers; however, large-scale exploitation of MCCE texturing approaches in industrial manufacturing will also pose challenges, especially in terms of waste management. Large amounts of metal nanoparticles need to be filtered out of the waste water, which requires additional effort and investment in waste-water treatment plants. From the solar cell perspective, metal contamination is also a major concern with this technique, and thorough metal removal and cleaning processes are essential in order to address this problem.

Overview of commercial dry-texturing solutions

Plasma-based texturing has been widely investigated as a dry-texturing alternative for forming nanotextures in c-Si, achieving very low reflection values in both monocrystalline and multicrystalline wafers.

From the field of microelectronics, reactive-ion-etching (RIE) processes using oxygen-fluorine-containing etching gas mixtures to effectively pattern silicon surfaces have long been the accepted standard method [10–12]. In these processes, the directionality of the RIE plasma etching is exploited in order to realize precisely defined vertical etching structures. A so-called *black-silicon method* was developed by Jansen et al. [13], which was then applied by Schnell et al. [14] to solar cells on a laboratory scale; weighted reflectivities of less than 3% were achieved, but with (at that time) relatively poor homogeneity and reproducibility over large areas.

In the last 10 years many different research groups, as well as dry-etch equipment manufacturers, have investigated technical solutions for the large-scale application of plasma-based texturing. Not only have technical issues had to be taken into account, but also environmental

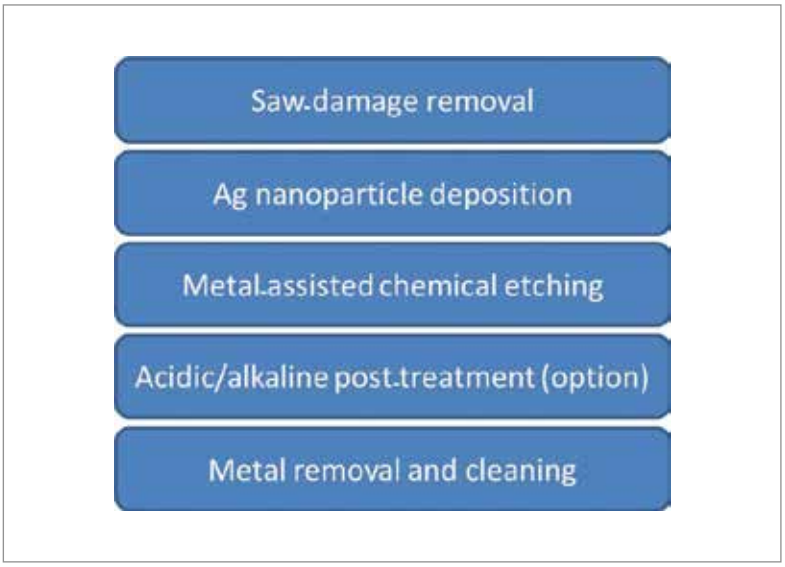

Figure 4. Generic process flow for black silicon based on metal catalyst chemical etching (MCCE) [9].

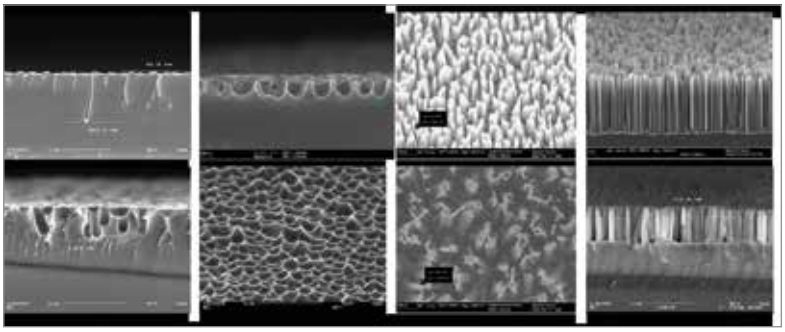

Figure 5. MCCE processes can produce a wide variety of nanotexture structures (SEM images provided by ASG).

aspects. Generally, gases with high global-warming potential (GWP) – such as SF_6, CF_4 and NF_3 – are used as a source of fluorine species in order to etch silicon [15]. This means that high-end in situ abatement systems are additionally needed in order to curb direct emissions from the etching process, which still cannot provide a 100% capture rate of the waste gases. In the industrial-scale production of solar cells, high amounts of F-containing gases need to be used, and this exacerbates the effect of these waste gases on the climate [16]. Developments in the direction of more environmentally friendly gases, such as F_2, are therefore needed to ensure the large-scale exploitation of this technology at acceptable costs, and to keep solar cell production a climate-friendly industry.

Reactive ion etching

The use of RIE to form grass-like black-silicon surfaces was first reported by Jansen et al. in 1995. This method employs SF_6 and O_2 gases to generate F* and O* radicals. F* is responsible for etching silicon, producing volatile products such as SiF_x. These products, particularly SiF_4, react with O* to form a passivation layer of SiO_xF_y on a cooled silicon substrate (Fig. 6). This passivation layer is partly removed by ion bombardment, and the exposed silicon is further etched by F*. The etching reaction is exothermic, and reduces the chance of producing a new passivation layer, since SiO_xF_y is prone to desorption upon heating.

In contrast, there is far less ion bombardment on the side walls of the formed silicon columns; thus, the passivation layer in those regions is largely preserved, preventing further etching. This etching/passivation competition mechanism leads to the formation of random silicon microstructures with very high aspect ratios in a self-masking fashion (Fig. 7).

The morphology of the black silicon fabricated in this manner can be adjusted by changing various RIE parameters, such as gas composition and flow rate, system temperature, substrate bias and RF power.

Another alternative reactive gas is Cl_2; although it offers a lower etching rate than SF_6/O_2, it is much easier to manage, owing to the formation of non-volatile by-products, and thus makes the control over the passivation layer deposition and silicon etching comparatively straightforward. Cl_2 can also be added into SF_6/O_2 to extend the gas composition working window.

Commercial solutions for RIE-based dry-texturing are offered by the Korean companies WONIK IPS and Jusung and the Japanese company ULVAC; however, no further details of the individual process set-ups have been released by these companies.

Atmospheric dry etching (ADE)

F_2 is known for its role in the isotropic etching of Si in a plasma-less process for bulk micromachining of Si for its application in microelectromechanical systems (MEMS). A very high reactivity to Si in atmospheric pressure conditions and a zero GWP make F_2 an interesting candidate for applications in photovoltaics. Atmospheric pressure texturing of Si is based on the principle of

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spontaneous reaction of F_2 with Si to release SiF_x species; this reaction occurs with a very low energy barrier, and without any need for ion-induced excitation.

Fig. 8 shows the basic layout of the etching tool developed by NINES PV: diluted F_2 is used as the only etchant. The etching gas is preheated to a certain temperature before it is delivered to the Si wafer in order to facilitate partial dissociation of F_2 molecules into individual atoms. The heated wafer is transported continuously through the reactor at a set velocity. A series of gas curtains contains the reactive gases inside the reactor, while allowing the continuous feeding of wafers. The temperature of the wafer governs the surface kinetics of the reaction. Elevated temperatures to supply more energy to the F_2-Si reaction system are possible. The F_2 can be diluted by mixing it with N_2, and the F_2/N_2 gas mixture is delivered uniformly to the wafer.

The wafer is etched at a constant speed while passing through the reaction zone. The etching process is single sided, which means that only the side facing the etching gases is textured. The dynamic etch rate is a function of F_2 concentration, total gas flux, temperature of the heated gas, temperature of the wafer, and velocity of the transport band. The process parameters can be optimized to form nanotextures of different aspect ratios: for example, nanotextures with a depth of up to 1µm and an estimated weighted reflection (R_w) of < 2% for <100> Si and < 5% for mc-Si.

Challenges of implementing black silicon in solar cell processing

The creation of black-silicon surface structures on the front side of a solar cell dramatically lowers its final surface reflection. Especially in case of mc-Si surfaces, the final surface reflection achieved by this method is much lower than in the case of the traditionally used acidic texturing. However, the incorporation of these black-silicon structures in a solar cell is not straightforward because of the notable difference in feature sizes compared with the structures formed by standard texturing techniques.

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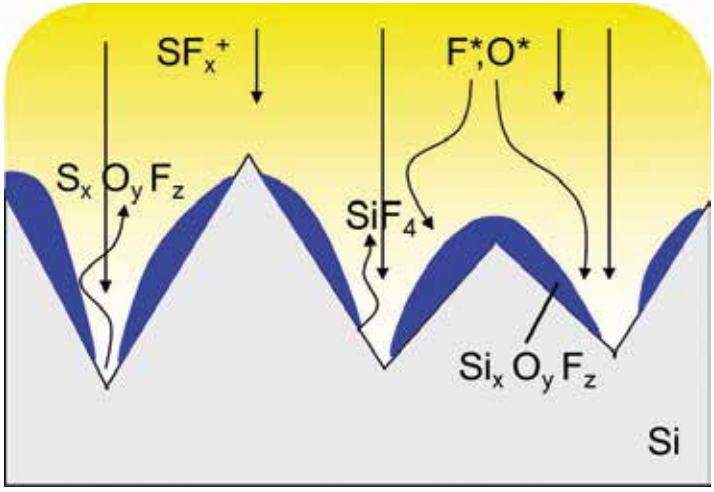

Figure 6. Etching mechanisms for plasma-based dry etching of silicon surfaces.

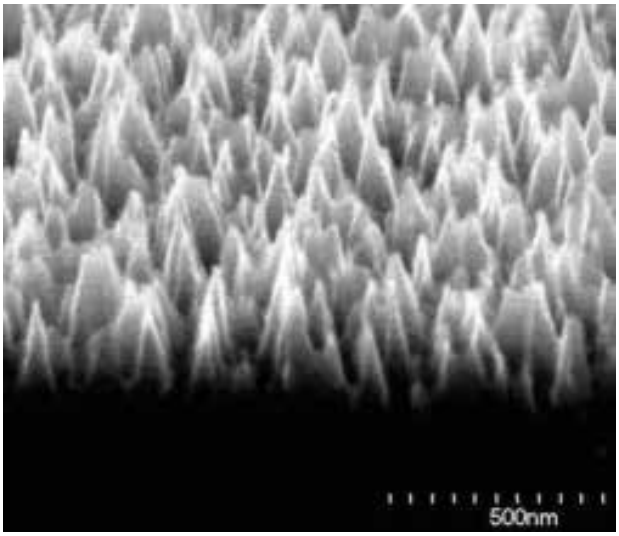

Figure 7. SEM image of a typical black-silicon structure fabricated by RIE.

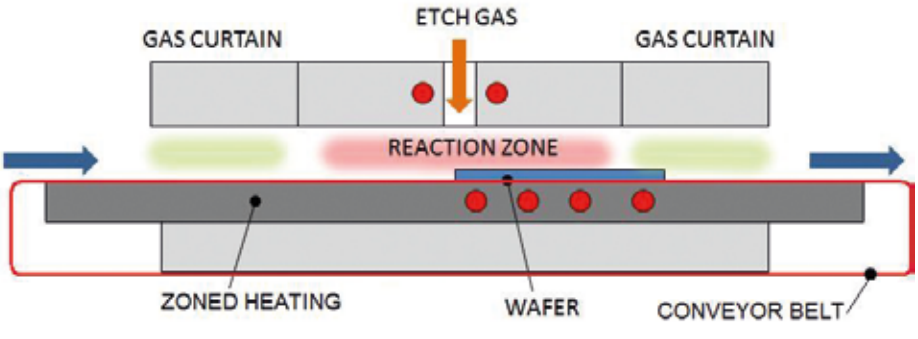

Figure 8. Schematic showing the chemical etching process of Si by thermally activated F_2 gas at atmospheric pressure conditions. The mixture of inert gas (N_2) and process gas (F_2) is led through a heated zone to facilitate a partial dissociation of F_2 atoms or to form radicals.

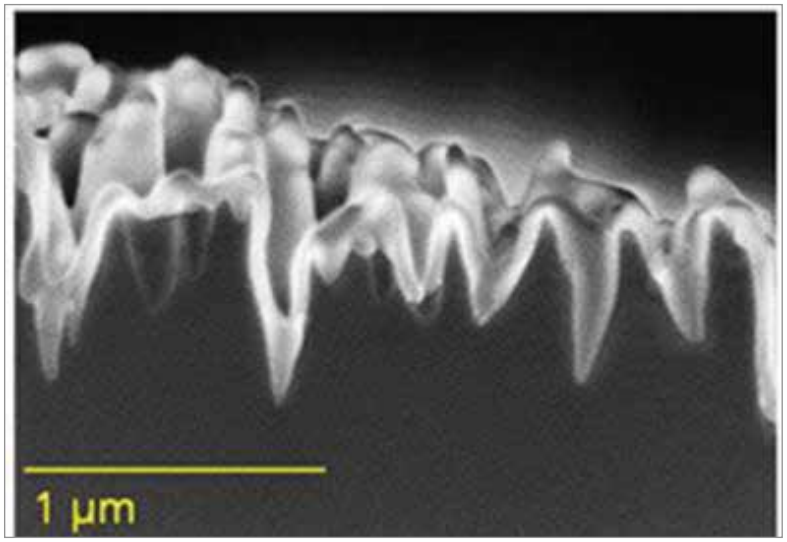

Figure 9. SEM image showing conformal deposition of phosphosilicate glass (PSG) layers on a nanotexture during the emitter diffusion process [34].

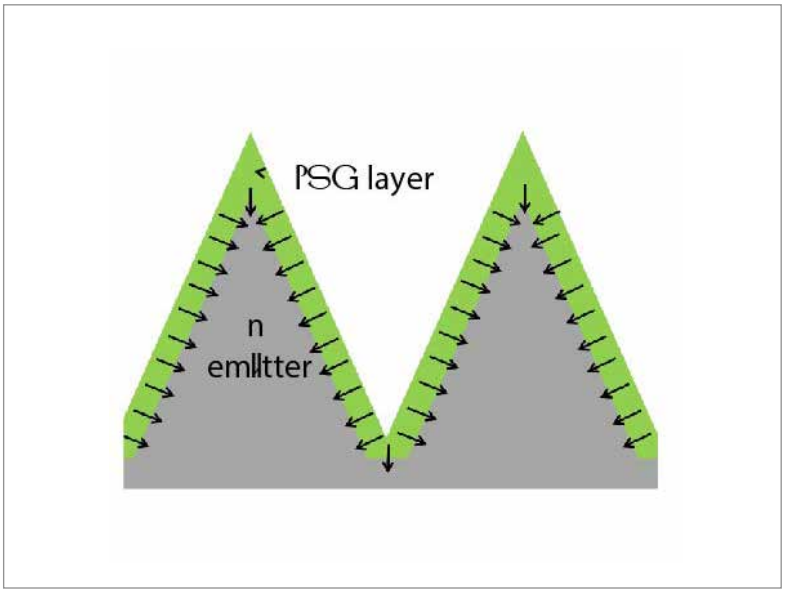

Figure 10. Sketch of heavy diffusion of phosphorus from the deposited PSG layers in a nanotexture [34].

"The surface passivation of nanotextured surfaces has been found to be one of the major challenges in fabricating high-efficiency solar cells."

Since the surface texturing of a Si wafer is one of the first steps in solar cell fabrication, each of the subsequent processes is significantly influenced by the introduction of a nanotexture with unique surface features; therefore, an adaptation of these process steps is necessary in order to fabricate efficient solar cells on nanotextured surfaces. Furthermore, the selection of process tools and technologies in a solar cell production line is currently made with the aim of optimizing the efficiency, production and yield of standard solar cells. If conventional texturing is replaced by a novel process, the adoption of additional novel technologies could be essential in order to realize the full potential. Nevertheless, these technological developments should also be feasible for rapid upscaling from the laboratory to industry in order to provide economic competitiveness. The introduction of nanotextures therefore presents new challenges that need to be addressed to ensure that the higher power gain promised by their excellent light-trapping abilities is eventually realized in the industrial production lines in an economically competitive way.

Surface passivation

The passivation of nanotextured surfaces has been found to be one of the major challenges in fabricating high-efficiency solar cells. The black-silicon structures are reported to be difficult to passivate by the typically used plasma-enhanced chemical vapour deposition (PECVD) SiN_x layer [17–19], whereas a variable level of passivation is achieved after applying a thermal SiO_x layer [20,21]. The major reasons behind the insufficiency of the passivation are: 1) greater surface area; 2) potentially more surface defects because of texturing damage; 3) higher level of crystal-orientation-dependent recombination; and 4) conformality issue of the deposited layer.

Meanwhile, the rapid development of the atomic layer deposition (ALD) technique has made it possible to form conformal AlO_x layers on nanostructured surfaces and to achieve surface recombination velocities that are comparable to those of the reference texture [22–25]. Several studies have subsequently focused on the issue of surface passivation on nanotextured surfaces, and a good understanding has been developed, especially in respect of the application of ALD AlO_x layers.

Another strategy to improve the conformality of the deposited layer is a modification of the surface topography; this method has been simultaneously developed by many groups in recent years [26–33]. The individual results have not been reviewed here, but can be consulted in the listed references.

Emitter diffusion

Another challenge for nanotextured surfaces relates to the formation of the pn junction. Typically, the application of a standard emitter diffusion process to nanotextured surfaces has resulted in poor electrical performance. This downside is attributed to a lower level of surface passivation and a high active doping in the emitter region; in particular, the Auger recombination mechanism is reported to dominate other recombination channels in nanostructures. These accounts have been supported by both experimental observations and device simulations (see Figs. 9 and 10).

On the basis of carrier-lifetime measurements on diffused nanotextured surfaces, Oh et al.

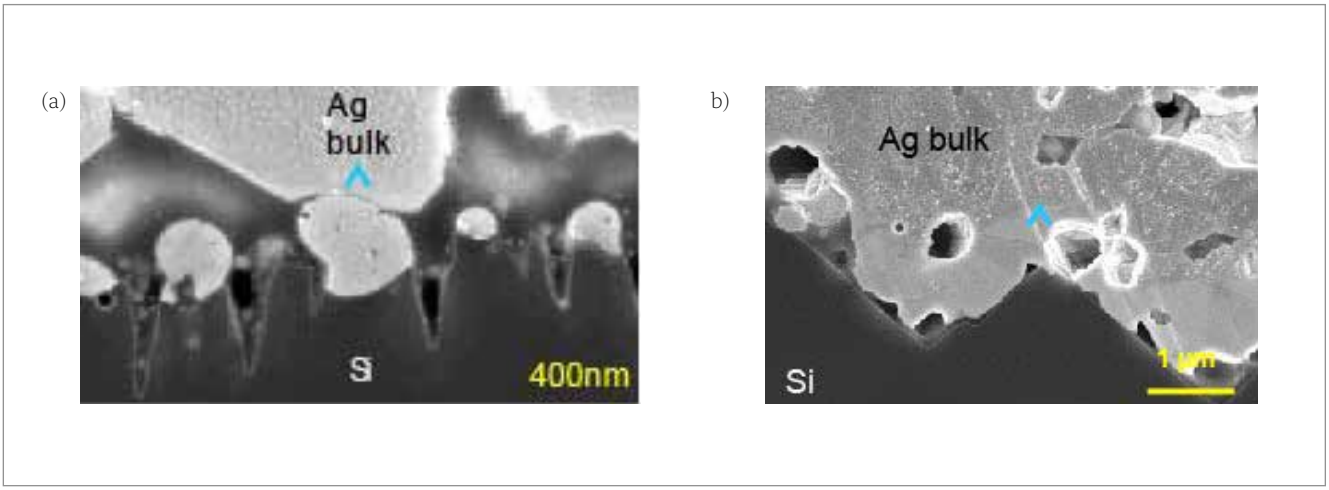

Figure 11. SEM images showing ion-beam polished Ag-Si contact interfaces of (a) a nanotextured surface, and (b) an alkaline-textured sample. The blue arrows indicate the possible physical current path from the Ag bulk to the emitter [34].

[26] showed that Auger recombination is more dominant in comparison to surface recombination in the case of high to medium doping of the emitter. A higher emitter sheet resistance (R_{sh}) is associated with a lower Auger recombination, and is reported in many studies to improve the quantum efficiency of the nanotextured solar cell in the short to medium wavelengths [17,26–27]. Furthermore, several authors have reported a reduction in emitter recombination either by tailoring the size of the nanotexture [17,26,27,31,35,36] or by increasing the R_{sh} [37]. Similar conclusions have been reached by simulating diffused nanostructures using PC1D, and regarding them as a planar surface with a highly doped region (dead layer) that does not account for current generation [27,36]. Hence, a broad agreement in this field of research is that reducing the Auger recombination is the key to increasing the performance of p-type nanotextured solar cells.

Metallization

Apart from the composition of the silver paste, the firing process and the thickness of the dielectric coating, the emitter properties and the surface topography are assumed to play an important role in the contact formation process [38,39]. A low specific contact resistivity (ρ_c) value for both pyramid- and acidic-textured samples has previously been attributed to the better wetting behaviour of the glass layer [39,40], which leaves the tips of these structures virtually free and promotes direct contacting [39,41]. Further investigations performed by varying the size of the pyramids have shown that when the size of pyramid is larger than the thickness of the glass layer, then the ρ_c values do not change abruptly [39]. On the basis of microscopic investigations of contact areas, it is maintained that the direct local interconnection of Ag crystallites to the Ag bulk and/or the formation of direct macroscopic contact between the Ag bulk and the emitter surface offer the major contribution to the current transport mechanism in all nanotextured surfaces (see Fig. 11).

To the authors' knowledge, no dedicated study with the goal of understanding the contact formation on nanotextured surfaces (which have significantly smaller feature sizes than conventional textures) has so far been carried out. In the literature relating to nanotextures, there have been several conflicting reports about the possible impact of nanotexture dimensions on the series resistance (R_s) and fill factor (FF) values of solar cells. Hsu et al. [20] reported that the increasing depths of the nanorods are detrimental to the series resistance for screen-printed contacts. In another study, Repo et. al. [42] explained their lower FF value on a black-silicon solar cell as an inability of evaporated metal to reach the valleys of the texture. In the meantime, high FF values on similar surfaces have been achieved by several other authors [28,29,31,35,43]; however, the difference in emitter and/or lack of detailed information about the contacting procedure make it difficult to correlate the contact behaviour with the nanotexture dimensions.

Summary

Several promising wet- and dry-etching-based technologies for the texturing of diamond-wire-sawn mc-Si are currently available for high-throughput industrial application in solar cell manufacturing. Up to now, none of these technologies has made its way to representing the current standard in the industry; however, simple approaches, mainly using the same tool set-up of existing production lines (acidic texturing process), offer some advantages. These approaches basically offer only the means of homogeneously texturing DWS silicon wafers; they do not offer the possibility of creating a superior texturing alternative with significant lower surface reflectance. For that, technologies (such as MCCE, RIE or ADE texturing) that are able to create black-silicon-like surface

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structures are necessary. To fully exploit the potential of these more advanced texturization processes, additional efforts and adaptations of the subsequent processing steps during solar cell manufacturing are necessary. From a cost of ownership perspective, the overall efficiency gain resulting from black-silicon textures needs to be weighed against the cost of these potential adaptations (additional CAPEX) in the later processing chain, up to module fabrication.

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