Progress in co-plating contacts for bifacial cells designed for multi-wire interconnection

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ABSTRACT

For many applications, bifacial modules offer a cost-effective way of increasing energy yields, which explains why the interest in bifacial cells in the PV industry is steadily growing and is expected to continue. However, the metallization of bifacial cells creates new challenges, as the same materials and techniques developed for n surfaces are generally not directly, or simultaneously, applicable to p surfaces; this necessitates sequential metallization of each side, resulting in added cost and/or complexity. This paper introduces a simple co-plating approach with the objective of simplifying the metallization of bifacial cells in a cost-effective way, and which is designed for multi-wire module integration. The metallization route is described, and high cell efficiencies of up to 22.4% are demonstrated using this co-plating approach with bifacial nPERT+ cells (where '+' signifies the bifacial nature of these cells). Initial thermal-cycling reliability data of test structures and 1-cell laminates is presented. Finally, cost-of-ownership (COO) estimates are given, which predict the co-plating approach to be ~40% cheaper than bifacial screen-printed metallization. It is shown that the combination of the high efficiency potential of nPERT+ cells and the reduced costs of co-plating has the potential to deliver module-level costs of ~$0.25/Wpe (glass–glass configuration).

Introduction

Interest in bifacial solar cells is steadily growing in the PV industry, and this is reflected in the prediction by the 2016 ITRPV roadmap [1] of a 20% market share by 2026. The reason for this interest is that bifacial cells can offer an effective way of increasing module power without significantly increasing processing costs. When bifacial cells are integrated into glass–glass modules, energy yield gains above 10% (kWh/kWp) compared with monofacial cells have been reported with just 20% albedo [2]; significant gains have also been reported over a wide range of operating conditions [3–7]. An additional advantage is that bifacial cells can also harvest more light when integrated into traditional glass–backsheet modules, as less light falling between cells (compared with glass–glass integration), or otherwise absorbed at the monofacial cell rear, is lost [8]. Many companies are now offering bifacial glass–glass modules (Yingli, PVGS, Panasonic, SolarWorld, Motech, Sunpreme, etc.) and/or glass–backsheet configurations (LG, SolarCity [now Tesla], Mission Solar, etc.). Although the PV industry's interest in bifacial cells is on the increase, certain challenges remain with regard to measurement standards and to the increased complexity in predicting annual energy yields from bifacial systems, which increases uncertainty in bankability.

Currently, industrial bifacial cells are typically based on a passivated emitter and rear cell structure (PERC) using p-type wafers, or on passivated emitter and rear totally diffused (PERT) or silicon heterojunction (SHJ) structures using n-type wafers [9]. Compared with PERC, PERT cells are more tolerant of the use of thinner (and hence cheaper) wafers [10] but typically require more processing steps [11].

> "The metallization of bifacial cells is technologically more challenging than with monofacial cells."

The metallization of bifacial cells is technologically more challenging than with monofacial cells, as shading losses are required to be low on both the n and the p side, potentially increasing series resistance losses, and most techniques applicable to one side are not directly applicable to the other.

Screen printing is widely used but has certain disadvantages. On the n side, a poor contact resistance Rc is typical at low doping levels ($<5.10^{19}cm^{-3}$). On the p side, with the use of AgAl pastes it is difficult to avoid Al spiking, causing low V_{oc}/FF; in addition AgAl pastes also suffer from lower conductivity than Ag pastes. Forming p contacts using non-firing-through Al pastes is an alternative, but again these suffer from low conductivity and need to be aligned to (laser) openings, thus increasing the usable finger width and shading. Metallizing silicon heterojunction bifacial cells has additional restrictions, since they cannot withstand the temperatures used for firing standard pastes and require the use of expensive low-temperature Ag pastes, which also have lower specific conductivity than standard Ag pastes. Apart from these issues, there is the fundamental concern that silver is expensive and suffers from price volatility, which explains why much effort is made to reduce silver consumption in solar cells.

Metallization by plating is also challenging for bifacial cells, as light-induced plating (LIP) – a common technique used in plating monofacial cells – can only be used to plate onto the n-side contact area. One option is to plate the n and p sides separately, one after the other, using two different techniques: the n side using LIP, and the p side by field-induced plating (FIP) [12]. In the case of FIP, the n side is electrically contacted but not in contact with the plating solution, and the cell is forward biased, providing electrons at the p-contact area for the reduction of the metal ions in the plating solution and the deposition of metal [13]. This approach is sequential and therefore slow and high in capex, as well as requiring relatively complex cell contacting and manipulation. Another approach, used mainly with high-efficiency SHJ cells, features a blanket-sputtered seed layer, a mask and electro-plating, as described in Geissbuhler [14].

Very narrow and high-aspect-ratio fingers are achievable by masking, but this process introduces significant additional material costs (physical vapour deposition (PVD) seed layer, and mask deposition/removal) and higher capex costs (three tools are necessary).

Imec's bifacial cell metallization approach

At imec an attempt has been made to address some of the shortcomings outlined above in the current screen-printing or plating techniques used to metallize bifacial cells. Imec's metallization approach is based on fulfilling three main objectives: 1) low (or zero) Ag usage in order to reduce material costs; 2) a tool set that is simple and capable of high throughput in order to reduce capex costs; and 3) enable stable high cell/module efficiencies.

An approach believed to be capable of meeting these objectives is described below; it is based on electroless and immersion plating to enable simultaneous contact-free co-plating of n and p contacts. A multi-wire interconnection approach relaxes the finger line conductivity requirement in order to achieve good fill factors, so that sufficient line conductivity can be obtained by nickel plating capped with a thin immersion Ag layer. The metallization sequence developed at imec is shown in Table 1. As only two thin metal layers are required, the processing time is relatively short; moreover, being a batch plating process, the throughput can be easily scaled.

The key attractive features of this metallization route are:

- Self-aligned plating (no mask deposition/removal)
- Batch processing, with no contacting to cells
- Simultaneous co-plating of the n and p surfaces
- Low-capex equipment, with tank size determining the throughput

> "The surface activation step developed at imec is silicon selective, requires no post-anneal and is relatively inexpensive."

The main technical challenge in this plating sequence is to sufficiently activate the n and p surfaces to allow reliable electroless Ni plating without introducing unwanted effects. Although it is possible to simultaneously plate Ni using electroless nickel onto n and p silicon without an activation step, it is not possible using stable long-lasting electroless nickel-plating solutions and/or at similar rates on both surfaces [15]. A palladium activation step can be used, but this is relatively expensive and tends to also activate the areas where plating is not desirable, for example on silicon nitride, creating unwanted ghost plating [16]. The surface activation step developed at imec is silicon selective, and so only the silicon areas exposed for metallization will be activated. It requires no post-anneal and is relatively inexpensive (see later for a cost estimation). The technique is also effective, as it enables a thin conductive layer to be deposited on the n and p silicon surfaces, so that the subsequent electroless Ni plating effectively plates onto the same conductive surface on either side, rather than directly onto n and p silicon (Fig. 1).

The electroless Ni solution used

Process step (n and p surfaces)	Chemistry	Time	Function
Surface activation	Imec	< 2 min	Silicon selective surface activation
Electroless Ni	MacDermid	< 15 min	Ni plating on n and p surfaces
Immersion Ag	MacDermid	~2 min	For line conductivity and capping
Sinter < 450°C	Low [O_2] atmosphere	< 10 min	Reduces line and contact resistance

Table 1. The co-plating process sequence developed at imec.

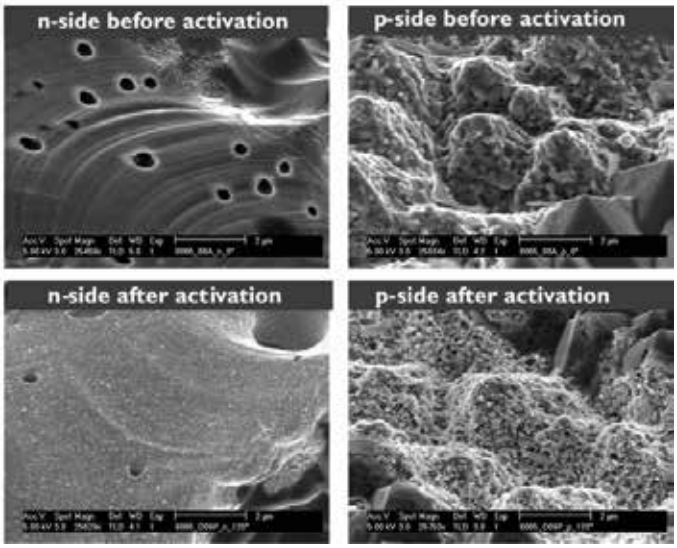

Figure 1. Laser-doped (locally-flattened) n surface and laser-ablated p surface, before and after the activation step prior to Ni plating. Note that the pits in the laser-doped n surface are artefacts of the doping process.

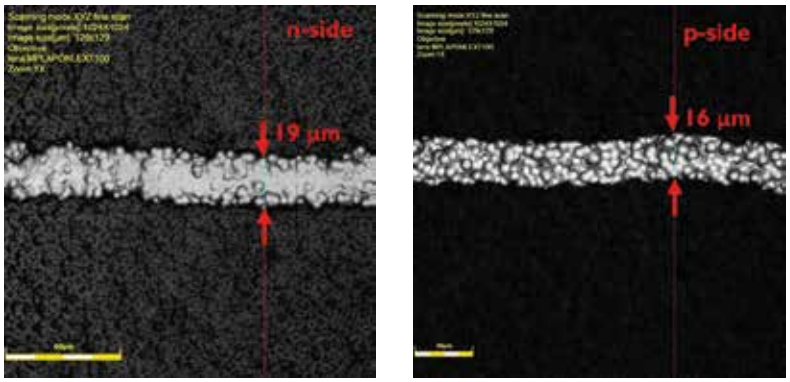

Figure 2. Optical microscope images of Ni/Ag co-plated lines on n and p Si opened by laser doping on the n side and by laser ablation on the p side (narrower laser opening).

in this work is a standard commercial solution from MacDermid, designed for high stability and long bath life, but there are many suitable alternatives. Optical microscope pictures of plated fingers after electroless Ni plating and Ag immersion show the high selectivity of the activation and plating processes, with no ghost plating occurring (Fig. 2).

Cell results

The co-plating process described earlier was used to metallize bifacial passivated emitter rear totally diffused cells on n-type wafers (nPERT+). The cell structure is shown schematically in Fig. 3, and the processing sequence is outlined in Fig. 4.

After KOH saw-damage removal and texturing, the wafers are subjected to a BBr_3 diffusion to form the emitter. The diffused layer is subsequently removed from the rear by means of single-side wet etching. After a front-side masking step and $POCl_3$ diffusion to form a back-surface field (BSF), front and rear passivation is performed. A stack of thermal SiO_2 and SiN_x is applied to the rear n^+ surface, and a stack of atomic layer deposited (ALD) Al_2O_3 and plasma-enhanced chemical vapour deposited (PECVD) SiN_x is used for front-side p^+ passivation. Laser patterning then opens the finger contact areas, allowing narrow line widths without masking (no busbar is patterned). On the rear side, a laser-doping process using a phosphorus-containing spin-on dopant is employed [17]. On the front side, ps UV laser ablation defines the contact. Next, a defect annealing step is performed in a belt furnace to mitigate laser damage, before the metallization sequence as outlined in Table 1 is applied.

Cells with both n^+ and p^+ sides passivated with thermal SiO_2 and PECVD SiN_x have also been fabricated; the results are compared in Table 2. The cell *I–V* data in this table were obtained using a Pasan Grid^{TOUCH} measurement system [18] (with 30 wires for current extraction plus 5 wires for voltage measurement on the front and rear) on a low-reflection back chuck; J_{sc} is corrected to remove measurement wire shading [19]. Since finger line resistance R_{line} is relatively high in these cells, there is a small but significant voltage offset between the voltage and current wires in the Grid^{TOUCH} system, which causes cell fill factors to be overestimated. The data in Table 2 show the downward-corrected fill factor values (FF) obtained from re-plotting the *I–V* curve after taking this offset effect into account and with the knowledge of the cell finger line resistances.

The known superior passivation of p^+ surfaces using Al_2O_3 is clearly seen in these results: the overall cell efficiency is improved by ~0.5%$_{abs}$. High pFF (>84%) and V_{oc} (>690mV) values demonstrate the potential for high cell efficiencies, with 22.4% currently the

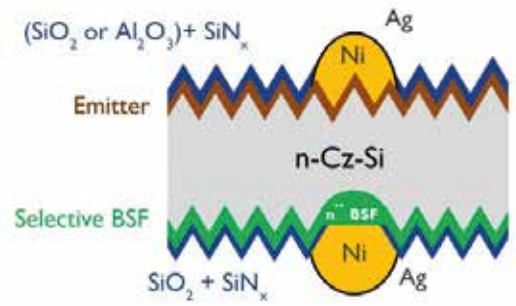

Figure 3. The nPERT+ cell structure.

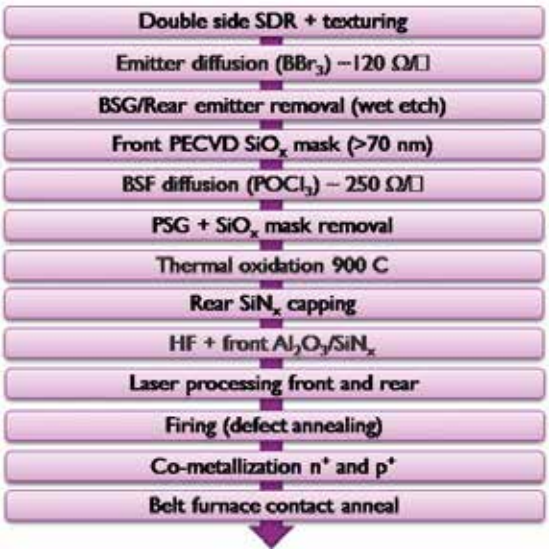

Figure 4. Outline of the nPERT+ cell process sequence.

P+ passivation		J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	η [%]	Bifaciality [%]	R_s [Ωcm^2]	pFF [%]
SiO_2/SiN_x	Average (4)	40.2±0.0	671±1	79.7±0.2	21.5±0.0	96.2±0.4	0.8	84.5
	Best	40.2	672	79.6	21.5	96.8	0.7	84.7
Al_2O_3/SiN_x	Average (4)	40.5±0.1	688±1	79.1±0.2	22.0±0.1	95.7±0.2	0.7	84.3
	Best	40.5	689	79.4	22.2	95.7	0.6	84.3
Al_2O_3/SiN_x (later run)	Best	40.6	692	79.9	22.4	95.7	0.6	84.3

Table 2. *I–V* data comparing two p^+ passivations, measured using a Pasan Grid^{TOUCH} contact system on a WACOM I-V solar simulator. (Cell area = 239cm^2, M0-sized wafers, wafer resistivity = 5Ωcm, wafer thickness = 180µm, *I–V* measurement based on a calibrated reference cell from Fhg-ISE Callab.)

best full-area cell result. The bifaciality (defined as the ratio of the J_{sc} measured when the back is illuminated to when the front is illuminated) is high, yielding values above 95%, which demonstrates excellent rear light-harvesting capability. Higher bifaciality values close to 100% have been obtained at imec if process modifications are made and if texture quality is not degraded during emitter removal on the rear side.

"High pFF and V_{oc} values demonstrate the potential for high cell efficiencies, with 22.4% currently the best full-area cell result."

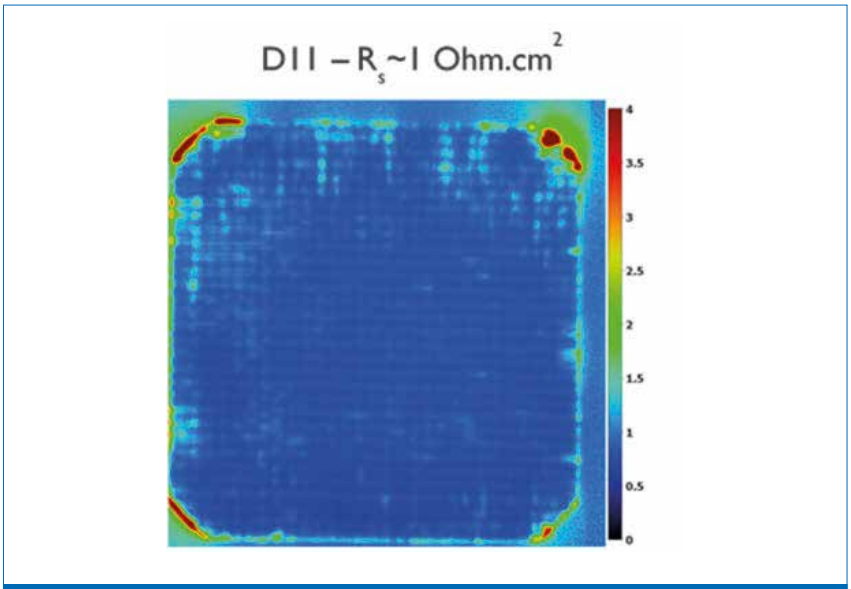

Figure 5. R_s map for laminate D11, showing increased R_s at the corners and at the cell edges.

Laminate results

The proposed plating sequence providing relatively low finger line conductivity is designed for multi-wire interconnection; it is therefore essential that a low and stable contact resistance between the wires and plated fingers be achieved. To evaluate this aspect, 1-cell modules using nPERT+ cells and multi-wire foils based on the Meyer Burger smart-wire approach were fabricated. The modules were created using a glass–backsheet configuration, and the multi-wire foils were created by embedding 30 equally spaced 320µm-diameter copper wires in a polyester/thermoplastic olefin (TPO) stack foil. During module lay-up, two such foils were placed either side of the cell, wires touching fingers, before finally front and rear encapsulants were added. The 30 Cu wires were coated by a thin layer of SnIn, which melts during the lamination process, creating the ohmic contact between the wires and the Ni/Ag plated fingers. Table 3 shows the *I–V* parameters of two nPERT+ cells before and after lamination.

The Grid^{TOUCH} measurements have J_{sc} and FF values adjusted as previously explained. The 1-cell laminates were measured using a 160mm × 160mm square mask to

Type	*I–V* details	Area [cm^2]	J_{sc} [mA/cm^2]	V_{oc} [mV]	FF [%]	η [%]	R_s [Ωcm^2]	Wp [W]
Cell_D11	GRID^{TOUCH}	239	40.5	689	79.4	22.2	0.6	5.3
1-cell laminate	*I–V* probes	256	*37*	689	77.8	*19.8*	1	5.1
Cell_D13	GRID^{TOUCH}	239	40.4	688	79.1	22	0.7	5.3
1-cell laminate	*I–V* probes	256	*37*	690	77.1	*19.7*	1.1	5

Table 3. *I–V* data before and after lamination, for two 1-cell laminates.

	I_{sc} [A]	V_{oc} [V]	FF [%]	1-cell laminate power [W]	60-cell module power [W]	η – full module [%]**
nPERT+ Bifacial/multi-wire/Ni/Ag glass/backsheet-M2	9.68*	41.3	77.8	5.19	311	18.9
LG Neon 2 Bifacial/multi-wire/SP glass/backsheet-M2	10.05	40.9	77.9	5.33	320	19.5

*I_{sc} is adjusted from M0 to M2 wafer size by the area ratio of the wafers.
**A module area of 1.640m^2 is assumed.

Table 4. Predicted 60-cell nPERT+ module performance compared with the performance of an LG Neon 2 module.

simulate the optical enhancement from the white backsheet surrounding a cell, as in a normal module configuration (with 2mm distance between cells). The laminate J_{sc} was calculated using the larger masked area (256cm^2).

The cell and laminate V_{oc} values were quite similar. Fill factor values for the laminated cells will depend on the number of multi-wires used, their dimensions and the finger line conductivity. The increase of ~0.4Ωcm^2 in series resistance R_s after lamination and the lower fill factor are due to two factors: 1) an additional ~0.2Ωcm^2 is the result of the multi-wire resistance affecting the laminate measurement but not the Grid^{TOUCH} measurement; 2) the remaining additional ~0.2Ωcm^2 is attributed to non-ideal current collection near the cell edges in the laminates as a result of the fingers not extending sufficiently into the corners of the cell. R_s maps from the laminates clearly show the latter effect, as can be seen in Fig. 5; the central region of this map demonstrates good uniformity, with values of ~0.8Ωcm^2, which indicates excellent wire-to-finger contacting.

As a benchmarking exercise, Table 4 shows the predicted power of a 60-cell module using the D11 1-cell laminate data compared with the bifacial LG Neon 2 320N1C-G4 module. The nPERT+ data is adjusted to the M2 wafer configuration by increasing I_{sc} by the M2/M0 wafer area ratio.

Although the nPERT+ module prediction is lower with regard to I_{sc} and power than for an LG Neon 2 module, the result is encouraging, as several areas of the nPERT+ module are still to be optimized. For example, the cell ARC coating is not optimized for a module, and the number of multi-wires versus finger conductivity is not optimal.

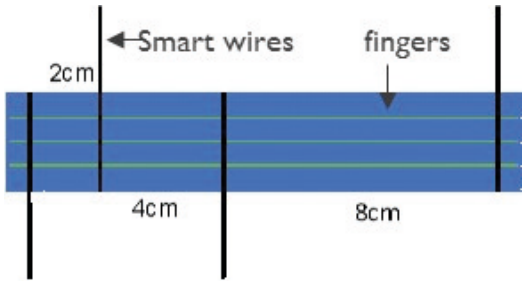

Figure 6. Design of laminate test structures for reliability testing.

Reliability results

To investigate the stability of wire-to-finger contacts when subjected to thermal cycling, a series of laminate test structures were constructed, as depicted in Fig. 6. Four single wires (cut from multi-wire foils), spaced 2, 4 and 8cm apart, contact the cell fingers on one side of a cell during lamination. By measuring the series resistance (4-wire method) for the six different distances between the wire contacts (2, 4, 6, 8, 12 and 14cm) and plotting series resistance versus contact spacing, the wire-to-finger contact resistance (Ωcm^2) and line resistance (Ω/cm) were able to be determined. Straight-line fits to the R_s versus wire spacing data yielded R^2 values of greater than 0.99, thus validating the approach.

Test structures were constructed with three different line widths using the same Ni/Ag plating by varying the laser ablation line width. Fig. 7 shows how the measured wire-to-finger contact resistance changed during 200 thermal cycles (–40°C to +80°C) for the three line widths. Wider fingers yielded a smaller change in wire-to-finger contact resistance on thermal cycling in this experiment, suggesting that the wire-to-finger contact area is important for stable contacts. Table 5 gives predictions of how the laminate fill factor would change as a result of the measured finger line conductivity and wire-to-finger contact resistance changes at 200 thermal cycles. These data provide encouraging evidence that integrating imec's bifacial co-plating process with multi-wire interconnection in accordance with IEC 61215 module reliability criteria is achievable.

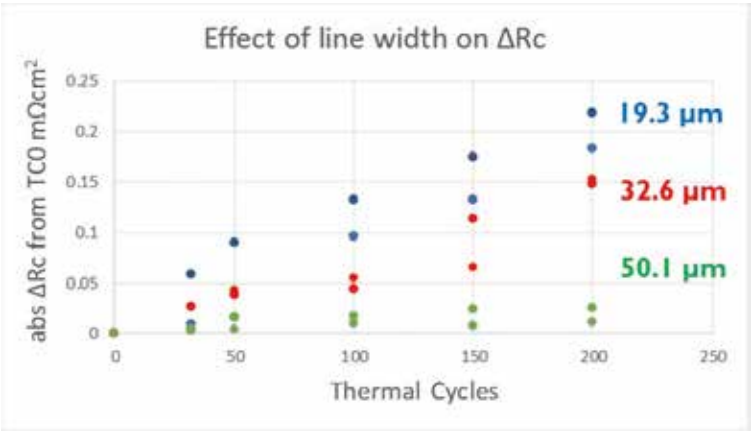

Figure 7. Change in wire-to-finger contact resistance during thermal cycling for three different plated-finger thicknesses.

Samples	Plated line width [µm]	Estimated ΔFF from ΔR_{line} @TC200 [$\%_{abs}$]	Estimated ΔFF from wire-to-finger ΔR_c @TC200 [$\%_{abs}$]
2	19.3	–0.01	–2.4
2	32.6	–0.00	–1.1
2	50.1	–0.01	–0.09

Table 5. Predicted laminate FF changes derived from line and contact resistance changes measured at 200 thermal cycles.

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The initial data from two 1-cell laminates subjected to thermal cycling, shown in Fig. 8, are also encouraging. Two metallization routes for the nPERT+ cells were used, while the laminates were made using the glass–backsheet configuration previously described. One control cell was metallized using a salicide process, in which Ni was blanket sputtered on both sides and sintered to form $NiSi_x$; the remaining Ni was etched off, followed by electroless Ni/iAg, as in the co-plating process. The other cell was metallized using the co-plating process, with the surface activation step replacing the PVD Ni/sintering step. The plated line widths were ~19µm. At 250 thermal cycles, both 1-cell laminates showed a P_{max} loss of less than 3% (Fig. 8), which is in line with the test-structure data.

Future work will investigate the optimization of the finger width and the wire and wire-coating thicknesses for reliability. More extensive reliability

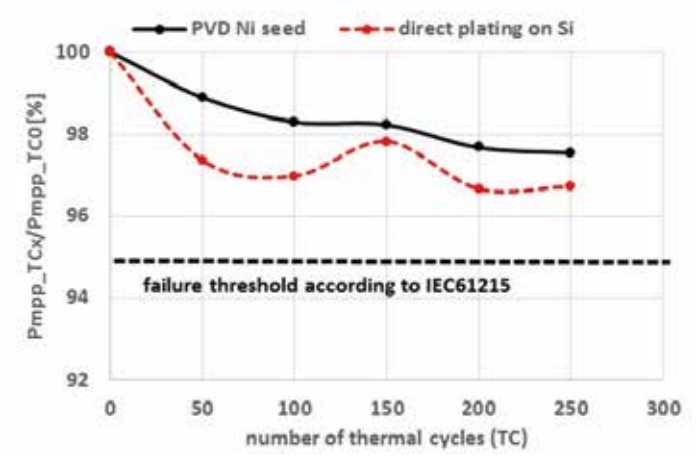

Figure 8. Change in P_{max} during thermal cycling for two 1-cell laminates, fabricated either using a PVD Ni seed layer or by co-plating directly on silicon.

Screen print (SP)	Ni/Ag
3,600 wfr/hr	3,600 wfr/hr
• AgAl front (fingers) • Dry • Ag rear (fingers) • Dry • Fast-firing • Test/sort	• Laser front (fingers) • Laser rear (fingers) • Fast-firing • Ni/Ag plating • N_2 anneal • Test/sort

Table 6. Process steps included in the metallization COO comparison between screen printing and co-plating of bifacial nPERT+ cells.

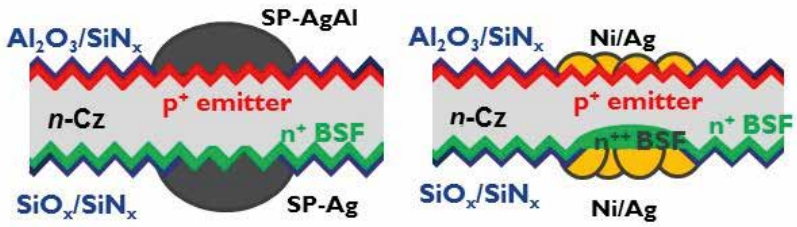

Figure 9. Screen-printing and co-plating cell structures used for COO comparisons.

testing is planned with 60-cell modules and additional tests conforming to IEC 61215 (e.g. damp heat and humidity–freeze/thermal-cycling sequences in accordance with IEC 61215).

Co-plating cost of ownership (COO)

One key advantage of imec's co-plating process is that it is cheaper than alternative bifacial metallization routes. With traditional Ag screen-printing technology, the use of multi-wires enables reductions in finger conductivity and in the consumption of Ag (and hence in cost). When Ni/Ag co-plating is used, an additional reduction in cost is achieved, driven by further savings in Ag consumption (to ~5mg/cell), but differences in other processing costs between the two technologies also need to be taken into account. On the basis of the processing sequences shown in Table 6 and of the cell structures depicted in Fig. 9, the costs of using screen printing and Ni/Ag co-plating to metallize nPERT+ bifacial cells were estimated. These projected costs include not only material costs but also costs related to depreciation, labour, waste, utilities, floor space and yield losses, as shown in Fig. 10.

Some key assumptions in the cost estimates are:

- Equipment depreciation is taken to be over seven years.
- Labour costs typical for Asia are used.
- 60mg/cell of AgAl is used for the emitter side.
- 40mg/cell of Ag is used for the BSF side.
- Waste disposal costs for contaminated rinse water and plating chemicals are included in the case of plated contacts.
- Multi-wire lamination costs are the same for both cases.

The breakdown comparison of metallization costs in Fig. 10 reveal the co-plating sequence to be ~40% cheaper than bifacial screen printing. Furthermore, it is calculated that at the module level the nPERT+ cell process can result in manufacturing costs as low as $0.25/Wpe. The 'equivalent' Wpe here refers to the additional power obtained from the bifacial illumination. Key assumptions in this calculation are a 22% average cell efficiency on 140µm-thick M2-sized wafers, a glass–glass module with a CTM ratio of 97%, and a 10% bifacial energy yield gain, resulting in a 72-cell module power of 411Wpe. This represents a significant reduction in costs compared with the current mainstream p-type mono-PERC, which achieves ~21.5% average cell efficiency and costs around $0.35–0.4/Wp.

Summary and outlook

An n and p surface Ni/Ag co-plating process has been developed at imec for the metallization of bifacial cells that is suitable for multi-wire module integration. Key features are very low Ag usage (typically <5mg/cell), line widths below 20µm, and batch cassette processing (no electrical contacts required to cells), enabled by a novel silicon selective activation step prior to Ni plating. Efficiencies of up to 22.4% have been achieved on nPERT+ bifacial cells using this metallization process, with a V_{oc} of greater than 690mV and a bifaciality of greater than 95%. Limited 1-cell laminate reliability data are so far encouraging, with IEC 61512 thermal-cycling test criteria being met.

Driven by much-reduced Ag usage and low-capex/high-throughput tools, the costs associated with this metallization process are estimated to be ~40% lower than with fine-line, busbar-free, bifacial screen printing for

multi-wire interconnection. The cost of ownership at the module level is estimated to be potentially ~$0.25/Wpe using reasonable assumptions, which is around 40% lower than for current mainstream modules.

Future work will focus on boosting module efficiency and further reliability testing at the 60-cell module level. Improved module efficiency, in particular module J_{sc}, is expected through the optimization of wires (number/diameter) and finger line conductivity, better UV response, and the use of a cell anti-reflection coating (ARC) optimized for laminates. A 22% average cell efficiency on 140µm-thick wafers is targeted with a cell-to-module (CTM) ratio of 97%, to provide a 72-cell module power of 411Wpe (assuming a 10% bifacial energy yield gain).

> "Future work will focus on boosting module efficiency and further reliability testing at the 60-cell module level."

Co-plating may also be applied to other cell architectures; for example, it is expected that this technology will also be advantageous for current pPERC+ bifacial cell structures. Another possibility is to capitalize on the fact that once a conductive 'seed' layer is applied by co-plating to both the n and the p side, it is relatively simple to simultaneously electroplate copper to both polarities if busbars exist. This opens up the possibility of Ni/Cu/Ag co-plating bifacial cells with busbars that require greater finger line conductivity than is achievable using non-contacting Ni/Ag co-plating. Inexpensive plated bifacial cells suitable for the Schmid multi-wire approach [20,21], or with three to five busbars for traditional interconnection, are potentially feasible using this approach.

Finally, although much work is still required before industrialization, the authors believe that the key elements relating to the viability and usefulness of co-plating for bifacial cells have been demonstrated.

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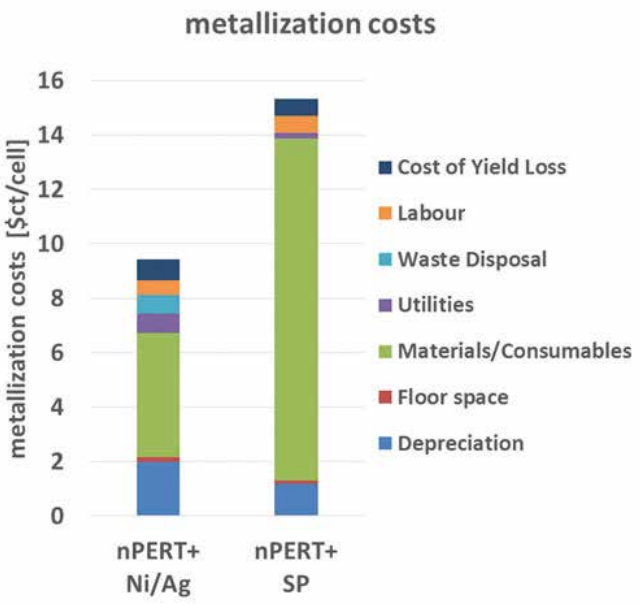

Figure 10. Screen-printing vs. co-plating metallization COO breakdown for nPERT+ bifacial cells.

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