Metallization and interconnection for silicon heterojunction solar cells and modules

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ABSTRACT

Silicon heterojunction (SHJ) solar cells demonstrate key advantages of high conversion efficiency, maximum field performance and simplicity of processing. The dedicated materials, processes and technologies used for the metallization and interconnection of this type of cell are reviewed in this paper. It is shown that fine-line printing, combined with multiple-wire interconnection, allows the cost of cell metallization to be drastically reduced, with as little as 30mg of Ag being used per cell side, which is compatible with high-performance and reliable modules. Copper-plating technology is demonstrated to be applicable to silicon heterojunction solar cells, allowing highly conductive fine fingers as well as high performance. While this process eliminates Ag usage, dedicated low-cost patterning technologies are nevertheless required.

Introduction

Silicon heterojunction (SHJ) technology is triggering a lot of interest in the PV community, owing to the high conversion efficiency achieved at an industrial production level with a limited number of production steps (a prerequisite for keeping costs low). The SHJ cell structure is an excellent demonstration of so-called 'passivating contacts'. Hydrogenated amorphous silicon (a-Si:H) layers and transparent conductive oxide (TCO) layers are deposited on both sides of a textured and cleaned n-type silicon wafer, over the entire surface, forming carrier-selective hetero-contacts with high-passivation properties [1,2].

The intrinsic a-Si:H layers deposited directly on the wafer surfaces provide excellent chemical passivation properties, yielding a minority-carrier lifetime that is potentially on a par with theoretical limits [3]. The doped a-Si:H layers then allow the selective collection of one type of carrier while blocking the other: the p-type doped layer acts as a hole-selective contact, and the n-type doped layer as an electron-selective contact. Finally, the TCO layers enable an efficient contact to be made between the a-Si:H doped layers and the cell metallization, and moreover provide lateral conduction and an anti-reflection effect. The typical structure of an SHJ cell is illustrated in Fig. 1.

> "One of the key advantages of the passivated contacts of SHJ solar cells is that increased operating voltages are attainable."

One of the key advantages of the passivated contacts of SHJ solar cells is that increased operating voltages are attainable; for instance, with this technology open-circuit voltages above 740mV can be achieved on commercial 180µm-thick (nominal thickness) Cz silicon wafers [3–7]. The main performance limitation is then linked to the fact that the full-area hetero-contacts exhibit parasitic light absorption in the thin TCO and a-Si:H layers. Advanced engineering of these layers is therefore required in order to maintain the high operating voltage while maximizing light transmission. An optimum trade-off can be realized, and an efficiency above 22.5% at the production level can be achieved [6,8]. The hetero-structure can be further optimized, and a record conversion efficiency was recently demonstrated by the company Kaneka in Japan [7] at the R&D level using this SHJ cell structure, with up to 25.1% cell efficiency being achieved on 151.9cm^2. This is the highest efficiency ever achieved on such an area for a double-side-contacted silicon solar cell, and demonstrates the potential for high performance of the simple SHJ cell architecture.

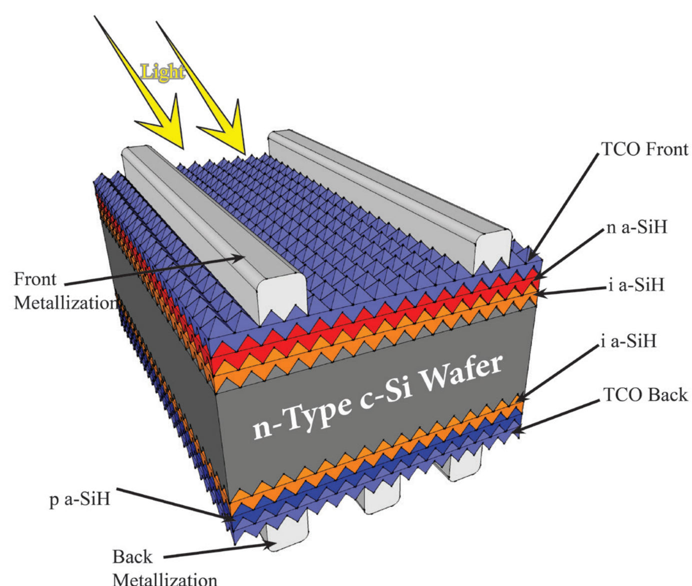

Figure 1. Schematic representation of the symmetrical structure of a bifacial silicon heterojunction solar cell with a rear-emitter configuration.

In addition, SHJ solar cells exhibit a key advantage of maximum field performance, or in other words improved kWh/kWp. These cells have a low temperature coefficient of –0.2 to –0.3%/°C, in contrast to around –0.4%/°C for standard diffused-junction technologies. Moreover, they are bifacial 'by nature' and can be used and optimized either with the p layer on the sunny side (referred to as a *front-emitter structure*), or with the n layer on the sunny side (referred to as a *rear-emitter structure*). The symmetrical SHJ architecture therefore allows high bifaciality above 90%, and potentially up to 100%. The passivated contacts and symmetrical structure of cells of this type also make them perfectly suited to an efficient use of thin silicon wafers. The excellent surface passivation allows high performance to be maintained, even for thin wafers less than 100μm [4], while the symmetrical layer structure on both sides of the wafer equilibrates mechanical stress, reducing the risk of wafer bending and breakage. These factors make SHJ solar cells the technology of choice for pushing forward the industrial implementation of thinner wafers.

The SHJ process sequence is kept simple, with just a few well-established production steps consisting of full-wafer deposition by plasma-enhanced vapour deposition (a-Si:H based layers) and mostly sputtering (TCO), all occurring at a low temperature (~200°C). This simple process sequence enables the best efficiency to be achieved.

An intrinsic process limitation of SHJ solar cells, compared with diffused silicon technologies, is the requirement of a low-temperature processing step following the a-Si:H layer depositions, in order to avoid degradation of the passivation properties. At the metallization level this constraint imposes the use of low-temperature-cured Ag pastes, with curing temperatures typically below 250°C. The printing of state-of-the-art low-temperature-cured Ag pastes yields Ag lines demonstrating typical bulk resistivity higher than 6 to $10\times10^{-6}\Omega\cdot$cm, or approximately a factor of two to three times higher than that for state-of-the-art metallization based on the firing-through of high-temperature Ag pastes. The higher Ag line bulk resistance for SHJ solar cells, compared with homojunction solar cells, therefore imposes economical and performance limitations for standard H-pattern metallization with two busbars (2BB) to five busbars (5BB): not only is more Ag required to achieve similar line resistance, but also lines with higher resistivities or larger dimensions have to be employed. With the use of state-of-the-art low-temperature-cured Ag pastes for H-pattern cells with 3BB to 5BB, improved performance can be achieved by, for instance, multiple printing. A typical laydown mass of 180mg of Ag per side represents a metallization cost of 8$cts/cell (assuming a Ag price of $460/kg); for a cell efficiency above 22.5%, the costs are typically ~1.5$cts/Wp per side, or 3$cts/Wp for a bifacial cell. (For simplicity, it is assumed that the Ag paste cost is the same as the Ag cost.) To overcome this cost and performance limitation because of the metallization, three approaches are taken: 1) a continuous enhancement of the electrical characteristics of low-temperature cured Ag lines; 2) a switch to multiple-wire interconnection; and/or 3) a switch to copper lines by employing electroplating processes.

Advanced metallization and interconnection for silicon heterojunction solar cells

Screen printing and busbar/ribbon interconnection

In the first approach, as SHJ cell technology continues to attract increasing industrial interest, certain paste and ink manufacturers continue to improve their low-temperature-cured products, allowing the bulk resistivity of the printed Ag lines to be decreased. A reduction to less than $5\times10^{-6}\Omega\cdot$cm, for instance, will allow the amount of Ag to be typically decreased to around 130mg, which reduces the cost to ~5.7$cts/cell.

For the interconnection of SHJ cells with busbars, standard ribbon soldering can be applied on optimized pastes for that purpose, as proposed in early 2013, for example, for a 5BB interconnection of SHJ cells [9]. To limit the temperature during ribbon contacting, alternative technologies have since been proposed, such as the printing or the dispensing application of electrically conductive adhesives for ribbon attachment (e.g. the method proposed by teamtechnik [10]). The latter approach further facilitates the introduction of light-capturing ribbons, which can increase the module power output by about 1 to 2% [11].

Fine-line printing and multi-wire interconnection

In the second approach, alternative advanced interconnection technologies using multiple wires can be employed to significantly relax the constraints on the SHJ solar cell metallization conductivity. SmartWire Contacting Technology (SWCT) makes use of copper wires supported by a polymer foil (see Fig. 2) [12–14]. The wires are

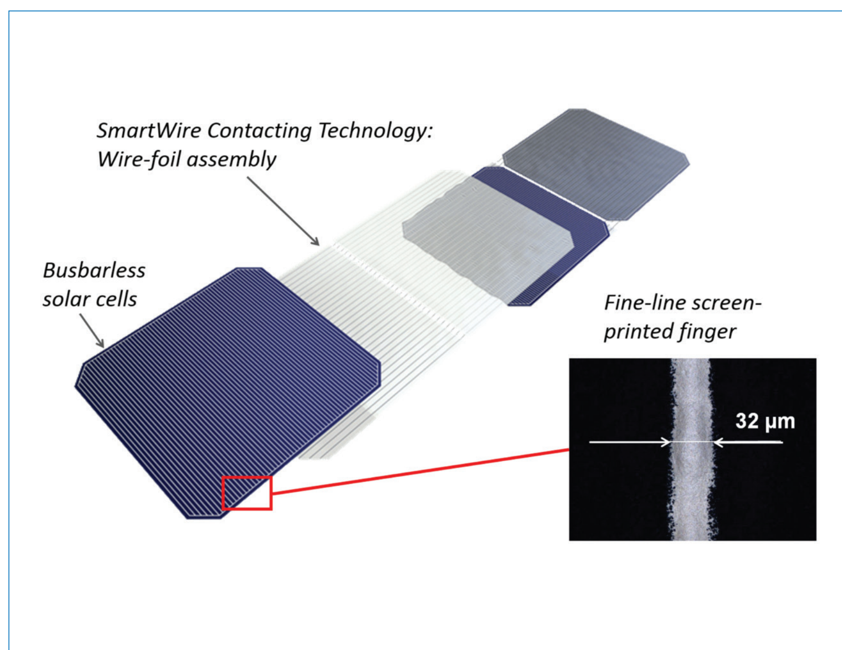

Figure 2. The interconnection concept of using a SmartWire foil-wire assembly for string production. The insert shows a confocal microscope image of a 30μm-wide finger that has been screen printed on a silicon heterojunction solar cell using low-temperature-cured Ag paste, allowing the high performance of SmartWire modules [12].

coated with a thin alloy layer that has a low melting point; this melts during the module lamination process and builds up a solder contact with the cell metallization fingers, thereby keeping the temperature budget low, which is perfectly suited to SHJ cells and to thin-wafer cell–module integration. This approach replaces state-of-the-art busbar and ribbon technology, and is applicable to cells having front metallization without busbars and solely fingers (see Fig. 2), referred to as *busbar-less cells*. First introduced by Day4 Energy [14], the technology is today mass produced by the Meyer Burger group with automated production equipment [12,13].

Because of a low wire optical dimension and the direct interconnection to the neighbouring cell, SWCT allows the use of more distributed current extraction paths perpendicular to the cell metallic fingers than with standard busbar technology. Wires with a diameter of 200µm are typically employed, exhibiting an optical dimension of about 140µm as a result of the re-collection of part of the light reflected onto the circular wire surface [12–15]. This allows the passage from standard interconnection schemes using three or five busbars/ribbons to interconnections with more than 18 wires, without increasing the shadowing losses of the interconnections.

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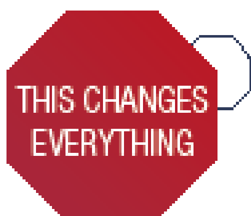
The use of multiple-wire connections means that the ohmic losses in the cell metallization fingers are significantly decreased. By using 18 wires (the standard arrangement for SWCT), the power loss (P_f) in the cell metallic fingers can be divided by 13, compared with a 5BB design, provided the other parameters are kept constant (Equation 1). This because the power dissipation losses in the fingers, P_f, is inversely proportional to the square of the number of busbars:

$$P_f \propto \frac{J^2 L}{12\, n_f} \frac{R_f}{n_{BB}^2} \propto C \frac{R_f}{n_{BB}^2} \qquad (1)$$

where J is the current density, L is the width of the cell, n_f is the number of fingers, R_f is the finger line resistance, n_{BB} is the number of busbars and C is a constant [12,16].

The increase in the number of interconnection wires (busbars) therefore enables the implementation of more resistive fingers than in the case of state-of-the-art busbar cells. Similar power losses can be achieved with a 5BB design and an 18-wire design having a finger line resistance 13 times higher than that of the 5BB case. Consequently, while fingers with a line resistance of less than 1Ω/cm should be implemented in 5BB cells to achieve optimum performance, the SWCT method with 18 wires allows the integration of fingers with a line resistance of up to 10Ω/cm, to realize similar electrical losses in the fingers.

The use of SWCT therefore significantly relaxes the constraints on the conductance of the printed fingers; this, in turn, completely changes the way of thinking when optimizing the metallization of the fingers. The challenge in the printing technology thus shifts from making the high aspect ratio fingers required for sufficient conductance and minimum shadowing (for instance achieved by multiple printing), to printing continuous fingers that are as fine as possible in order to reduce the silver



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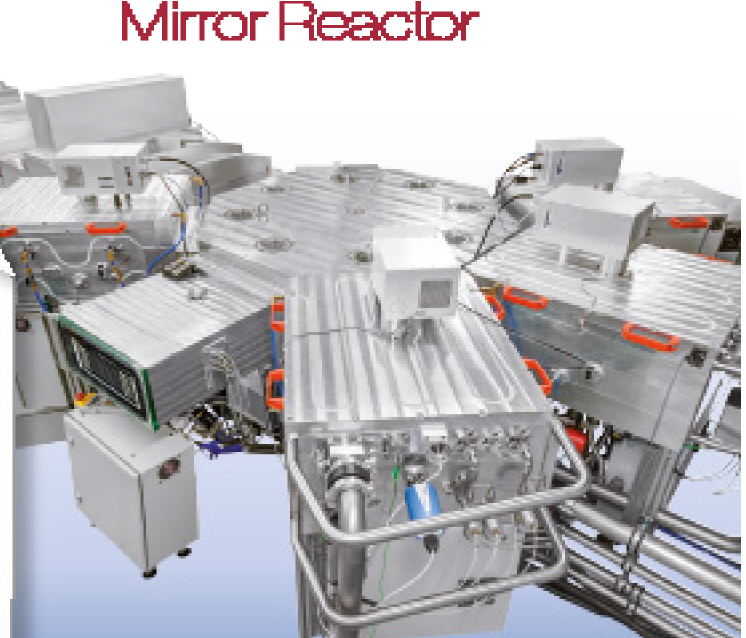

Figure 3. Semi-transparent facade of the renovated CSEM building in Neuchâtel, Switzerland, which comprises bifacial silicon heterojunction solar cells that are interconnected using SmartWire Contacting Technology [17].

lay-down (cost reduction) and to increase the current density (efficiency enhancement).

Recent developments in the fine-line printing of low-temperature cured Ag pastes have demonstrated the possibility of printing low-temperature cured Ag lines with sufficient conductivity using minimum screen openings down to 20µm; this has resulted in approximately 30µm-wide fingers with a line resistance of 5Ω/cm, which is sufficient for module integration using SWCT without adding electrical losses from the fingers [12,16]. This represents a double benefit: first, since only 30mg of Ag is necessary per side, considerable savings in metallization costs are realized; second, thanks to the reduced shadowing of the finer printed fingers, an increase in performance is achieved, with a relative gain of about 1% possible [12,16].

When SWCT is used, the consideration of a typical lay-down mass of Ag of 30mg per side represents a metallization cost of 1.33$cts/cell (for an assumed Ag price of $460/kg). Compared with a 22.5% cell efficiency obtained using standard printing, an efficiency of 22.7% can be achieved using fine-line printing, yielding finger metallization costs of ~0.23$cts/Wp, which is around one-sixth the cost of the standard case. SWCT technology therefore demonstrates how an initial weakness of SHJ technology can be turned into a strength, as record low usage of Ag is made possible, resulting in an ultra-low cost of the printed Ag and an increased cell performance.

In 2014 the high-performance potential was demonstrated with a 327Wp module which integrated 60 silicon heterojunction solar cells, corresponding to a total-area module efficiency of 20% [15]. In addition, high reliability with this technology can be demonstrated: a degradation of less than 5% after undergoing more than three times the IEC standard test criteria for accelerated degradation has been reported [8].

At the R&D level, there have been further developments in order to profit from the relaxed constraints provided by SWCT. For instance, the printing of copper lines was demonstrated to yield sufficient line conduction for use in combination with SWCT, and reliable modules were also demonstrated [16]; moreover, the cost-reduction potential of SWCT has been shown by implementing an alternative coating material for the wires [16]. Yet further advancements have been demonstrated in the form of the first bifacial single-cell modules with an efficiency of 19.9% without any cell metallization on the front side or the back [16]. Direct contacting is realized between the wires and the conductive front surface of SHJ solar cells; this, however, necessitates the implementation of a large number of wires.

> “By switching to copper-electroplating processing for the formation of the electrical grid, the use of silver can be suppressed and the metallization process maintained at room temperature.”

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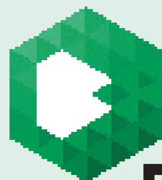

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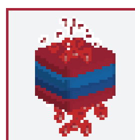

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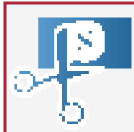

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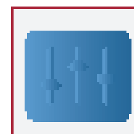

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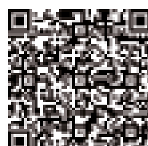

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Finally, the aesthetics of SWCT modules are today highlighted by the CSEM PV facade, which comprises spaced bifacial SHJ solar cells that are interconnected using SWCT, as shown in Fig. 3 [17].

Copper electroplating

In the third approach, certain technologies that enable the application of silver-free metal stacks with improved line conductance can be implemented. By switching to copper-electroplating processing for the formation of the electrical grid, the use of silver can be suppressed and the metallization process maintained at room temperature. The plated copper lines typically demonstrate a low resistivity of down to $2\times10^{-6}\Omega\cdot cm$, which is only slightly higher than the resistivity of pure bulk copper ($1.7\times10^{-6}\Omega\cdot cm$).

Copper electroplating is a possible alternative to the screen printing of silver paste that is currently used for diffused-junction silicon solar cells. In this case, the dielectric anti-reflection layer can be used as a plating mask by opening it by, for instance, laser ablation. The standard process then consists of the growth of a nickel–copper stack by plating. The nickel layer will form a nickel silicide barrier to copper diffusion after annealing, while the copper acts as the conductive layer. Such metallization technology was recently demonstrated on commercial equipment to enable low resistivity contacts on lightly doped emitters as well [18].

For the application of copper electroplating to silicon heterojunction solar cells, the situation is different: the plating is performed on the conductive front TCO layer of the SHJ solar cell [19–20]. This TCO layer will already act as an efficient barrier to copper migration towards the silicon, and therefore limit potential degradation. Since the layer is conductive, however, it requires the application of additional protective layers and processes in order to achieve the definition of a patterning mask to permit the selective plating. The development of the application of copper electroplating to SHJ solar cells therefore focuses on achieving low contact resistance and high adhesion of plated materials onto TCO layers, as well as on cost-effective patterning technologies.

Electroplated copper front-contact metallization has been successfully demonstrated for silicon heterojunction (SHJ) solar cells [19–20]. One patterning technique that potentially offers cost competitiveness with screen-printed metallization is the inkjet printing of a hot melt ink using a sophisticated process with significantly reduced ink consumption, as presented by Hermans et al. [21].

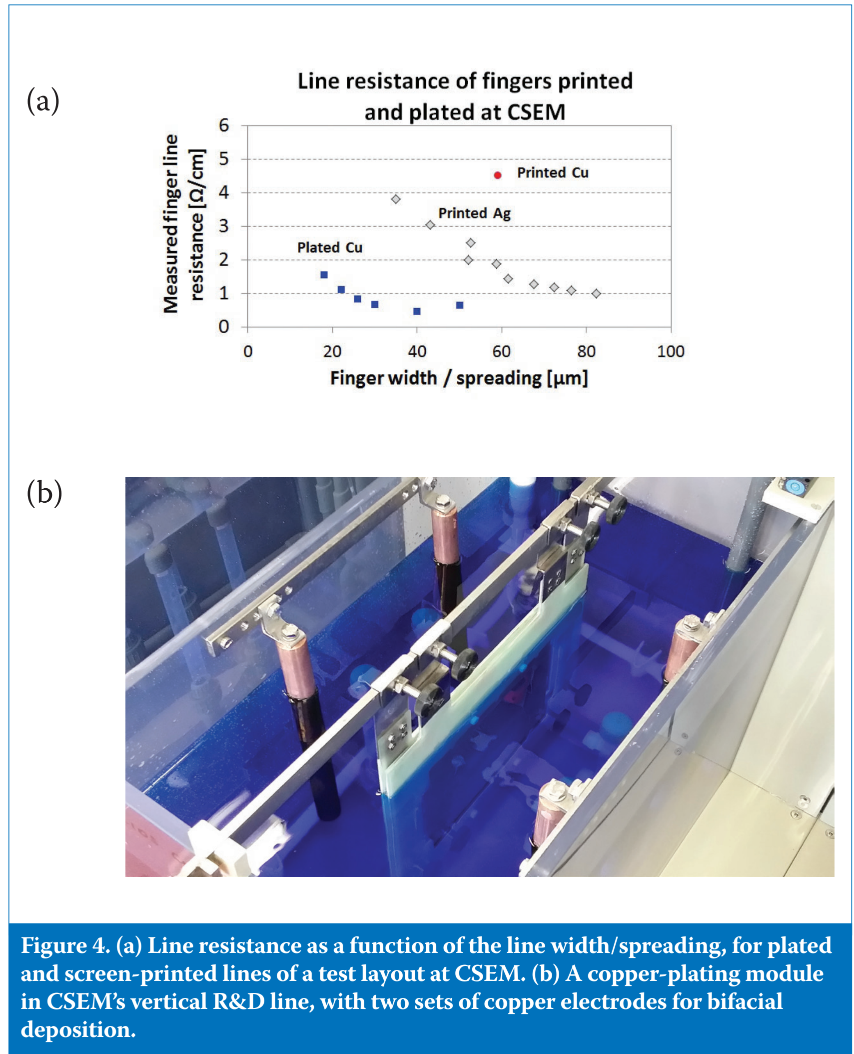

Figure 4. (a) Line resistance as a function of the line width/spreading, for plated and screen-printed lines of a test layout at CSEM. (b) A copper-plating module in CSEM's vertical R&D line, with two sets of copper electrodes for bifacial deposition.

The possibilities of achieving fine-plated lines with low line resistance are illustrated in Fig. 4, in comparison to the use of low-temperature cured Ag paste; 20µm-wide copper-plated fingers can be produced with a line resistance of about 1Ω/cm. This therefore allows the achievement of high performance to be considered with silicon heterojunction solar cells that also use a three- to five-busbar H-pattern design, the fine, conductive plated fingers yielding low electrical and optical losses. Furthermore, the high finger conductivity may offer additional advantages for low-concentration solar devices, as well as in new interconnection technologies, such as shingling, also referred to as *dense cell interconnection* [22].

"20µm-wide copper-plated fingers can be produced with a line resistance of about 1Ω/cm."

Conclusions

Various technological approaches have been purposefully developed during the last few years to completely overcome the initial limitation in performance and cost originating from the requirement of a low-temperature-cured silver paste for silicon heterojunction solar cells. A switch to copper-plating processes permits fine, highly conductive fingers to be realized, with today's established processes guaranteeing high adhesion and performance.

Further work is under way by the different industry players to determine their own cost-effective patterning technology. With some of the commercially available solutions, plating already offers the prospect of improved cost compared with screen printing in the case of busbar and

ribbon interconnection; moreover, plating facilitates alternative module technologies.

Importantly, multiple-wire interconnection was shown to be a paradigm shift in technology; the method relaxes the constraints of the metallization finger conductivity to the same level achieved by today's low-temperature-cured silver paste. Ultra-low Ag consumption has been demonstrated (down to 30mg per cell side), yielding a significant reduction in metallization costs, which is even more pronounced in the case of bifacial modules.

In conclusion, the different alternative metallization and interconnection technologies developed in recent years are now further advancing silicon heterojunction solar cell technology as a cost-competitive high-performance technology.

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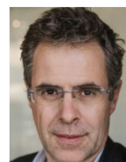
About the Authors

Matthieu Despeisse received his Ph.D. in 2006 for his work on advanced detectors at CERN in Geneva, Switzerland. He then joined EPFL in 2009 as head of the thin-film silicon photovoltaics research team. Since 2013 he has led research activities at CSEM concerning crystalline silicon photovoltaics and metallization, with a special focus on silicon heterojunction technology, passivating contacts, metallization and interconnection.



Christophe Ballif received his Ph.D. from EPFL, Switzerland, in 1998. In 2004 he became a full professor with the Institute of Microengineering at the University of Neuchâtel, where he directs the Photovoltaics and Thin-Film Electronics Laboratory, which is now part of EPFL. Since 2013 he has also been the director of the CSEM PV-center. His research interests include materials for PV, high-efficiency c-Si solar cells, module technology, BIPV and energy systems.

Antonin Faes received his Ph.D. in 2006 for his work on solid oxide fuel cells at the Interdisciplinary Center for Electron Microscopy (CIME) and the Industrial Energy System Laboratory (LENI) at EPFL. In 2012 he joined the CSEM PV-center in Neuchâtel, where he is responsible for c-Si solar cell metallization and interconnection activities, with a particular focus on silicon heterojunction solar cells.

Agata Lachowicz studied chemistry at Heinrich Heine University Düsseldorf, and worked initially on the development of processes for manufacturing printed-circuit boards, such as final finishes, copper plating and conductive polymers. She worked at Schott Solar and Meyer Burger Germany, focusing on PERC processes, before joining CSEM PV-center to work on the development of plating for silicon heterojunction solar cells.

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