Heterojunction technology: The path to high efficiency in mass production

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Abstract

Heterojunction technology is currently a hot topic actively discussed in the silicon PV community. Hevel recently became one of the first companies to adopt its old micromorph module line for manufacturing high-efficiency silicon heterojunction (SHJ) solar cells and modules. On the basis of Hevel's own experience, this paper looks at all the production steps involved, from wafer texturing through to final module assembly.

Introduction

In recent years, many solar cell and module producers in the silicon PV industry have been forced to adapt their existing production lines to new technologies in order to be able to deliver highly efficient and low-cost modules to the market. The most popular transfer has been from Al back-surface field (Al-BSF) to passivated emitter and rear cell (PERC) technology, since the latter is compatible with existing production lines used for standard technology. Nevertheless, excellent crystalline silicon (c-Si) surface passivation by hydrogenated amorphous silicon (a-Si:H) offers the possibility to employ the most expensive part of silicon thin-film production lines, namely plasma-enhanced chemical vapour deposition (PECVD) systems, for silicon heterojunction (SHJ) technology, as recently realized by Hevel LLC.

The simple structure of SHJ solar cells, in combination with their high efficiency and low-temperature processing, makes them very attractive to the PV industry. This is the reason why Hevel has decided to start a project on modernizing and transforming its micromorph module production line, which includes a large number of PECVD systems (KAI-MT PECVD reactors from TEL Solar), into a new SHJ line. The successful conversion of Hevel's production line for the manufacture of SHJ solar cells and modules was completed in April 2017 using an in-house SHJ solar cell technology developed by its R&D Center for Thin Film Technologies (TFTE – an R&D unit of Hevel).

The annual production capacity was increased from an initial 97MWp (for the micromorph line) to 160MWp during the first phase of the project, with an average SHJ cell efficiency of 21% being demonstrated in mass production. Meyer Burger's SmartWire Cell Technology (SWCT) was chosen for interconnection in SHJ module assembly. During the second phase of the project (June 2017–May 2019), the production capacity of Hevel's production line was increased to 260MWp, with an average cell efficiency of 22.8% obtained in mass production.

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Technology development

As can be seen in Fig. 1, SHJ cells have very simple structure and it takes only six process steps to fabricate them. Typically, the SHJ cell is composed of an n-type c-Si wafer coated on both sides with thin intrinsic and doped a-Si:H layers. The ultrathin intrinsic a-Si:H layers, with typical thicknesses of a few nanometres, have a crucial effect on the performance of SHJ cells. The aim of these layers is to suppress surface recombination by chemical passivation of dangling bonds on the c-Si wafer surface with the formation of Si-Si and Si-H bonds, as well as to prevent defect generation by dopant atoms during the deposition of doped layers. The doped layers are fully covered with indium tin oxide (ITO) films, followed by screen-printing of contact metal grids for current collection using a low-temperature conductive (LTC) Ag paste. To enhance the properties of the ITO layers and contact grids, low-temperature annealing is required.

Wafers for SHJ cells

As in the case of all high-performance c-Si solar cells, wafer quality is key to achieving high-efficiency SHJ cells. Although record efficiency values reported in the literature have been obtained using high-purity float zone (FZ) c-Si wafers, the development of the Czochralski process and the continuous improvement of polysilicon quality have allowed the impurity concentrations in CZ wafers to be reduced while keeping production costs reasonable. As a result, the open-circuit voltage (V_{oc}) of SHJ cells has recently reached values as high as 750mV.

Up to now, only monocrystalline CZ wafers have been used for large-scale manufacturing of SHJ solar cells. The electronic properties of monocrystalline silicon wafers for high-efficiency solar cells are determined by impurities and

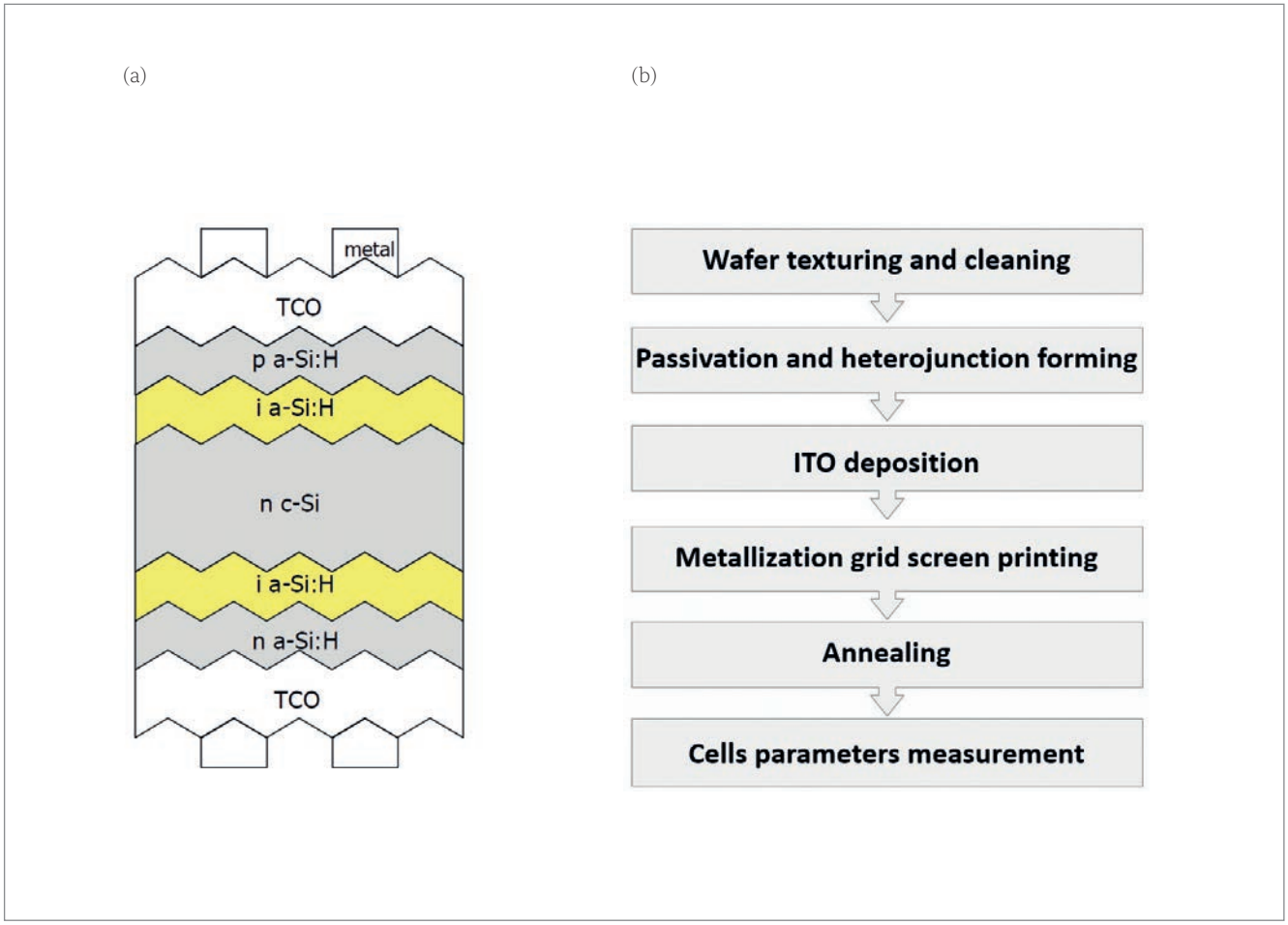

Figure 1. (a) Schematic cross-sectional view of a conventional SHJ solar cell. (b) The main steps of the SHJ cell fabrication process sequence.

dopant concentrations. Since the measurement of these parameters require special techniques that can hardly be used in the mass production process, the minority-carrier lifetime and wafer resistance are usually measured in practice and constitute the main parameters for determining the quality of wafers or ingots. These parameters usually vary along and across ingots, and their profiles depend on the details of the ingot growth process and post treatment. Consequently, it has been proposed to use the measured lifetime/resistance ratio as a cumulative measure of wafer and heterojunction qualities. Recent studies have also shown that for SHJ cells with V_{oc} > 750mV, passivated wafers with a lifetime-to-resistivity ratio above 4ms/Ωcm must be used.

The most significant advantage of SHJ technology in terms of cost reduction is that all process steps are performed at low temperatures (< 250°C), favouring the use of thin wafers for SHJ solar cell production. Recent progress in wafer slicing technology as a result of the implementation of diamond wire technology has resulted in the mass production of low-cost wafers with thicknesses less than 160μm. Wafers with an as-cut thickness of 150μm have recently been successfully implemented in the SHJ production process without module power losses, as illustrated in Fig. 2. Although further reductions in SHJ cell thickness are also possible without significant losses in efficiency, the implementation of thinner wafers in mass production is currently limited by handling issues, resulting in excessive wafer breakage rates.

A slight decrease in I_{sc} here is partially compensated by the V_{oc} gain, leading to a very small (<0.1%) efficiency loss when switching to 150μm as-cut wafer thickness in the cell production. At the module level, the cell efficiency loss is fully compensated by a 10% decrease in cell-to-module (CTM) ratio. The overall benefit of switching to 150μm wafers is on average around 1–1.5W per module.

The latest update to wafers was carried out in May 2019. The existing SHJ production line is able to adapt wafers of size 157.35mm × 157.35mm (M2+ wafer type). The use of such wafers with an optimized contact grid design leads to a power increase per cell of 0.15W (Fig. 3). Hevel's R&D Center is also currently working on further developments using M4 and M6 wafers as well as full square wafers and wafers with lower oxygen concentration.

"An enhanced cleaning procedure is necessary for the production of high-efficiency SHJ cells."

Wafer texturing and cleaning

As with other c-Si PV technologies, wet chemical treatment is the first step in the SHJ cell production sequence. The following steps are usually included:

- Etching of the highly defective surface part of the wafer (surface damage etch – SDE).
- Forming of the special surface morphology (texture) which reduces light reflection from the wafer surface (TEX).
- Cleaning of the wafer surface to remove organic and metal impurities.

While the first two steps based on isotropic (SDE) and anisotropic (TEX) alkali etching are similar to those used in other silicon PV technologies, the last step is significantly different. To obtain high-quality surface passivation, the wafer surface should be extra clean. An enhanced cleaning procedure is therefore necessary for the production of high-efficiency SHJ cells; this includes the removal of residual organic, ionic and metallic contamination (originating from the wet etching/texturing solutions) from c-Si wafer surface. In addition, heavy deionized (DI) water rinse steps are used between each chemical treatment. The wet chemical treatment ends with a short HF dip, which removes native oxide and passivates the c-Si surface with hydrogen atoms prior to the a-Si:H PECVD processes.

Much effort has been devoted at Hevel to stabilizing and optimizing the wafer texturing and cleaning processes. One of the steps of the optimization was a change to a single-component texturing additive; such an optimization enabled an increase in batch lifetime and a reduction in the consumption of chemical reagents.

Surface passivation and junction formation

High-quality surface passivation is key to achieving high values of V_{oc} in high-efficiency silicon-based solar cells. An insertion of thin (< 10nm) hydrogenated amorphous silicon (a-Si:H) layers between the c-Si wafer and the doped a-Si:H layers leads to higher V_{oc} values in comparison to those registered in the case when intrinsic

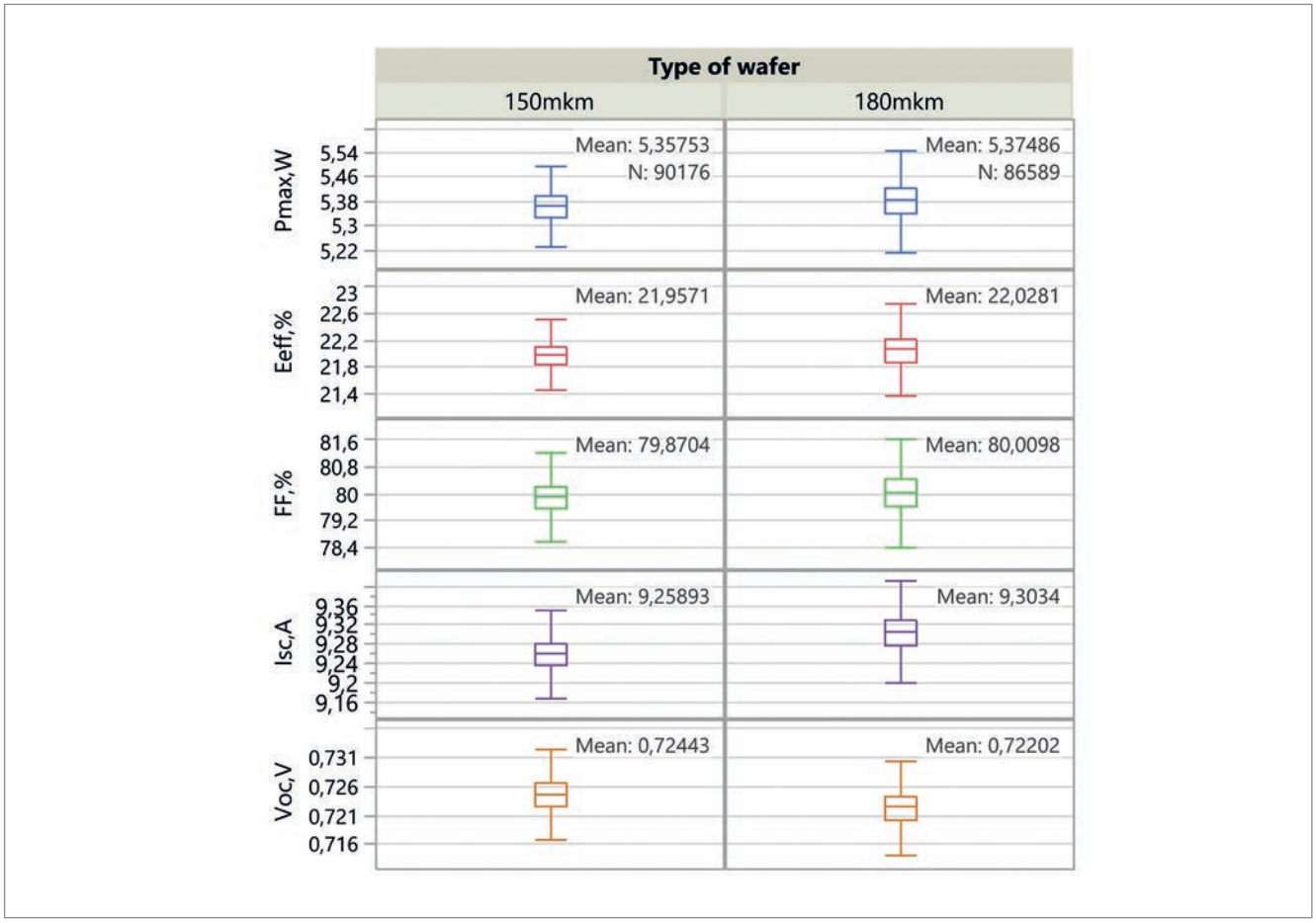

Figure 2. Results of 150µm-thick wafer implementation.

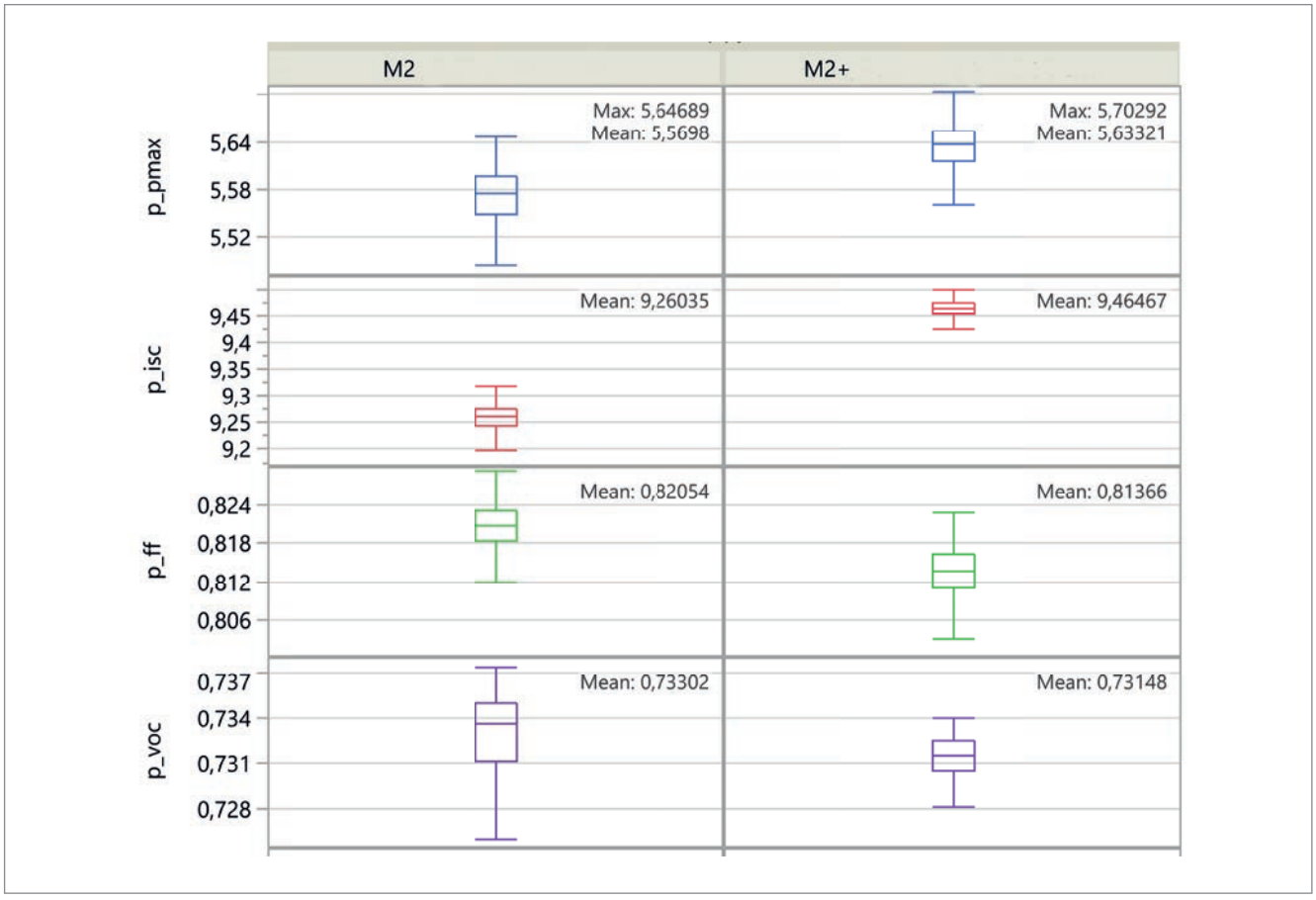

Figure 3. Results of larger-area wafer (M2+) implementation.

"Thinner rear ITO layers with higher transparency could increase the cell efficiency as a result of the better utilization of light in the IR part of the spectrum."

a-Si:H layers are absent. In the last two decades, the surface passivation of SHJ cells has been essentially improved by many research groups, resulting in V_{oc} values close to 750mV; this is approaching the theoretical limit (760mV) and underlines the particular appeal of this technology.

As a rule, a necessary condition for good surface passivation is that the a-Si:H/c-Si interface should be atomically sharp, meaning that silicon epitaxial growth is avoided, i.e. no crystalline material is deposited. This can be achieved by a proper tuning of the a-Si:H film properties during the deposition process. In practice, a-Si:H layers are commonly grown by the PECVD method using parallel-plate capacitively coupled plasma discharge in pure silane or in silane–hydrogen mixtures at temperatures close to 200°C. It appears that the most critical process parameters for surface passivation are the hydrogen-to-silane gas flow ratio and the RF power density, whereas the gas pressure may affect the film thickness uniformity.

The properties of doped layers can also have a big impact on cell performance: for example, an appropriate tuning of the thickness and doping profile of the n layer resulted in a 0.5% gain in cell efficiency, whereas in the case of the p layer the gain was about 0.1%.

Transparent conductive oxides

ITO layers are commonly used in SHJ cells as transparent conductive oxide layers, and it is very important to optimize their properties, in particular for the production of bifacial HJT solar cells. An investigation of the various stoichiometric contents of ITO sputter magnetron targets has been carried out at Hevel's R&D Center. It was found that thinner rear ITO layers with higher transparency could increase the cell efficiency as a result of the better utilization of light in the IR part of the spectrum. Such an improvement resulted in a module power increase of 3.7W because of the lower CTM loss, as well enabling a reduction in the cost of cell production, since 90:10 ITO targets are about 6% cheaper than standard 97:3 ITO targets. The optimized

recipes for ITO layers were implemented at Hevel's production line in Q1 2018.

Another approach taken for ITO layer optimization was the addition of an Ar/H_2 mixture during magnetron sputtering (Fig. 4); this method resulted in a power increase of 20mW per cell. In addition, many experiments are still ongoing with other special magnetron targets having higher Hall mobility. Some of these targets have already been tested at Hevel's R&D Center and showed promising results which justify further testing at the production facility.

To minimize the cost of cell production, the use of so-called *dogbone* targets is now under consideration. Targets of this type could bring about a lower target utilization rate, further decreasing cell production costs. Additional optimizations have been performed whereby the physical vapour deposition (PVD) tray has been changed and contact grid designs have been modified in order to minimize the inactive area losses. The modules assembled with such cells demonstrated an average increase in power of 1.8W.

Metallization

The process requirements for manufacturing SHJ solar cells have several advantages compared with those for conventional homojunction c-Si solar cells. The first advantage is the low thermal budget during the heterojunction formation; the deposition temperature of a-Si:H and ITO layers is usually less than 250°C. Second, the time required to form the a-Si:H/c-Si junctions and contact layers is also shorter for SHJ cells than for conventional c-Si solar cells based on

	Standard BOM	Optimized BOM and cell
P_{max} [W]	304	328
V_{pmax} [V]	34.72	36.66
I_{pmax} [A]	8.76	8.94
I_{sc} [A]	9.4	9.42
V_{oc} [V]	43.34	43.94
FF [%]	74.6	79.3

Table 1. Mean production values for the module *I–V* characteristics with standard and optimized BOM, including cell power optimization.

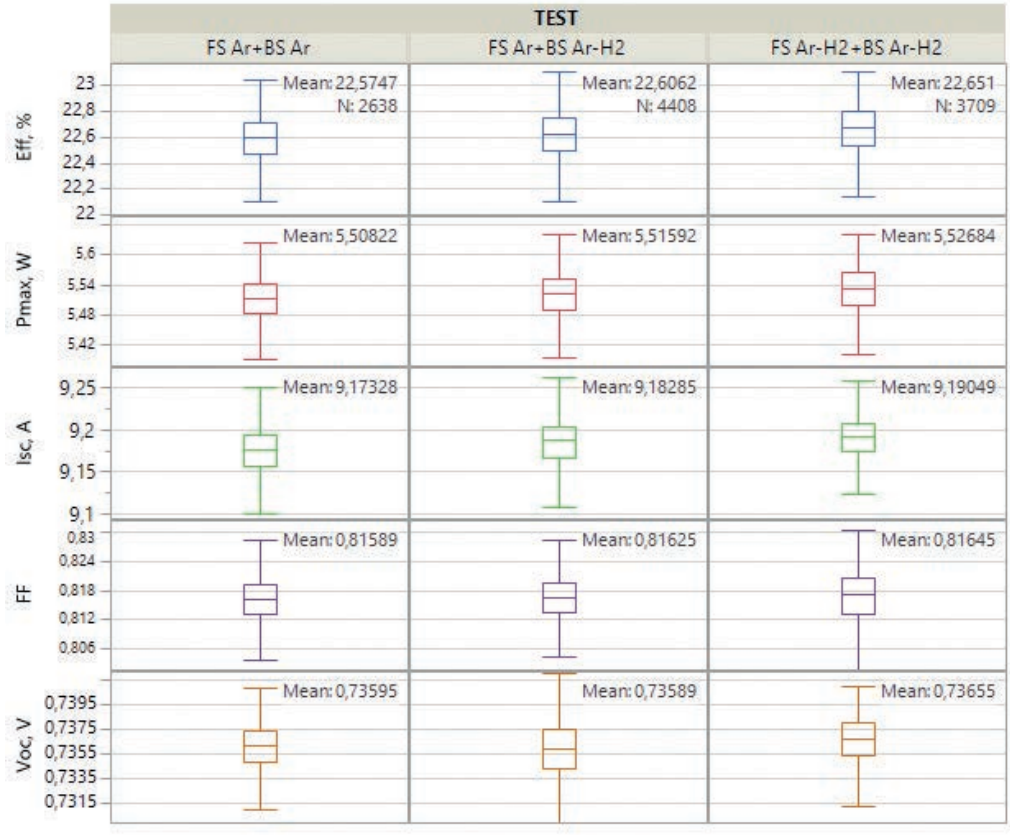

Figure 4. Results of ITO layer optimization by adding an Ar/H_2 mixture during magnetron sputtering.

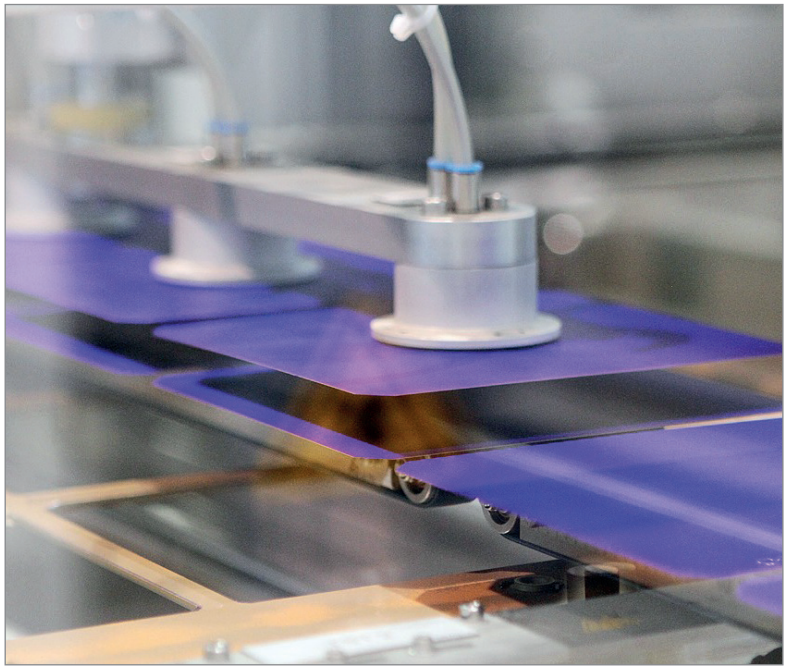

Figure 5. Hevel's production line.

thermal diffusion processes. Third, wafer bowing is suppressed because of the low process temperature and symmetric structure of SHJ solar cells.

There are disadvantages, however, to using low-temperature processes, the main one being that standard fire-through metallization techniques (with firing temperatures in the range 800–900°C) cannot be employed for SHJ cells. This is because the a-Si/c-Si heterojunction cannot withstand process temperatures above 200–250°C, at which point the hydrogen effusion from the internal surfaces of the heterojunction leads to a detrimental effect on cell performance. For this reason, the so-called *low curing temperature (LCT) silver paste* is commonly used for the metallization of SHJ cells via screen-printing, which is currently the state-of-the-art technology for the metal grid deposition.

Cell interconnection and module assembly

The interconnection of SHJ cells is a stumbling block for the whole process chain: soldering, which is used for the interconnection of conventional c-Si cells, is not compatible with LTC Ag paste, which has to be applied instead of the standard fire-through silver paste because of temperature restrictions for the a-Si/c-Si heterojunction. The low-temperature type of paste has higher bulk resistivity (two to three times that of high-temperature pastes) and low adhesion after soldering. Commonly, Ag busbars easily peel off the ITO surface with forces well below 1N/mm.

To overcome this limitation, new cell interconnection technologies have been proposed, such as gluing the ribbons using electrically conductive adhesive (ECA), or multiwire interconnection using the low-temperature attachment of a foil with embedded InSn-coated wires (Meyer Burger's SmartWire Connection

Technology – SWCT). InSn alloy with a low melting point of around 120°C has good adhesion to both the Ag paste and the ITO layer itself; hence a metallurgic contact between the wire and the cell surface is established after temperature treatment. SWCT technology does not require very precise positioning of the ribbons relative to the metallization grid, which is one of the major challenges for multiwire technology. The initial attachment of the cells to the wires in SWCT does not require precise soldering of the wires to the solder pads and is commonly done by an adhesive-layer-containing foil, which allows the use of a large number (up to 24) of relatively thin wires of diameter 200–250µm.

With an optimization of the SWCT module assembly bill of materials (BOM) – by tuning the optical properties of the lamination foils and the electrical properties of the wires – a gain of 9W for a 60-cell module has been achieved at Hevel compared with the standard BOM, with no increase in material costs (see Table 1).

Overall improvements in cell production (higher *FF*, leading to lower CTM) and in module assembly on Hevel's production line have enabled an average increase in power from 300W to 318W during the period Q4 2017 to Q2 2019.

In June 2019 Hevel started the ramp-up of a new assembly line for glass–glass modules using glued five-busbar cells; a full ramp-up is scheduled for July 2019. New bifacial modules will bring an extra gain in production capacity, as they can deliver up to 30% additional module output in power plants.

Another advantage of Hevel's new assembly line is the implementation of special light-capturing ribbon (LCR); its ability to diffuse reflected light can yield a module efficiency increase of up to 4% (according to producer data). The next generation of Hevel's modules will therefore have higher efficiency along with higher durability and stability as a result of a glass–glass configuration that enables lower module degradation.

Conclusions

In a record-breaking project schedule, Hevel has converted its low-capacity (97MWp) micromorph module production line into a moderate-capacity line (260MWp) for the manufacture of high-efficiency SHJ cells/modules by implementing an in-house cell production process developed by its daughter company R&D Center TFTE (Figs. 5 and 6). In less than two years after shutting down the thin-film line, an average cell efficiency of 22.8% has been achieved (with maximum efficiencies above 23.5%), resulting in a 60-cell module power of on average 318W (with a maximum module power of 328W) in mass production.

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About the Authors

Igor Shakhray has been the CEO of Hevel Group since 2015. He studied economics at Irkutsk State Economic Academy and received an MBA in asset management from RANEPA. Under his leadership, commercial operation of Hevel's solar module production line was set in motion and steered to full capacity in 2015, and the thin-film fab line was converted to heterojunction technology in 2017.

Dr. Alexey Abramov has been the head of the solar energy department at Hevel's R&D Center TFTE since 2010. He received his M.S. in quantum electronics from St. Petersburg State Polytechnical University, Russia, in 1993 and his Ph.D. in semiconductor physics from A.F. Ioffe Physical Technical Institute RAS, St. Petersburg, in 2001. From 2004 to 2010 he worked at CNRS and the École Polytechnique, Paris, as a researcher in the field of amorphous and nanocrystalline thin-film semiconductors and their applications in PV and large-area electronics.

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Figure 6. Visual control station on Hevel's production line.

Dr. Sergey Abolmasov has been a senior process engineer at Hevel's R&D Center TFTE since 2013, where he focuses on the development of thin-film silicon and silicon heterojunction solar cells. He received his D.Sc. in plasma physics from Kyushu University, Fukuoka, Japan, in 2003. From 2003 to 2010 he worked in the plasma technology sector as a researcher at Kyoto and Tohoku Universities, Japan, and at Samsung SDI Co. Ltd., Korea. From 2010 to 2013 he was with CNRS, École Polytechnique, France, working on amorphous/microcrystalline silicon solar cells.

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