Epitaxial Si lift-off technology: Current status and challenges

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ABSTRACT

The cost of silicon (Si) continues to be a significant component of the final PV module cost, and thus a major driver towards better Si utilization (g/Wp) in the PV industry. The continuation of this scenario, despite constant reductions in module prices, ensures an ongoing interest in the development of kerfless technologies in general, among which *epitaxial Si lift-off* is one of the more advanced technologies for high-quality monocrystalline silicon (c-Si) wafer production. Since its invention in the late 90s, this technology has been developed by different groups around the world. A number of start-up companies have recently taken on the challenge of commercializing this technology, providing the much-needed fuel for its leap from lab to fab. This paper gives an overview of epitaxial Si lift-off, providing insight into every step of the lift-off cycle and a flavour of the current status of this technology and the challenges it faces.

Kerfless technologies as an enabler of ultra-thin Si

The drive towards better Si utilization (g/Wp) has been an obsession in the Si PV industry over the last few decades as one of the key aspects in making photovoltaic energy production competitive. With the cost of Si still making up a third of the final Si solar module cost, there is continued interest in reducing the cost of Si by producing thinner wafers and reducing kerf losses [1]. However, conventional wafering technologies are hitting a brick wall, as it is increasingly challenging to produce thinner wafers with high yield and low total thickness variation [2]. Moreover, thicker wafers can better withstand automated handling systems in cell and module production lines and are therefore preferred, since yield is a highly sensitive cost factor in PV production [3]. As a result, the average Si thickness has stabilized to around 180µm. In fact, the latest ITRPV roadmap gives a more tempered prediction in terms of wafer thickness reduction in the coming years, compared with previous editions [1].

Numerous alternative technologies to conventional wafer production have been explored in order to eliminate kerf losses and/or to produce ultrathin silicon in a thickness range that is beyond the reach of conventional wafering. Such technologies that allow wafer production with negligible kerf losses are called *kerfless* or *kerf-free* wafering technologies. In many of the kerfless wafering techniques, the Si wafer is detached or released from the surface of a substrate or ingot, in a process called *lift-off*.

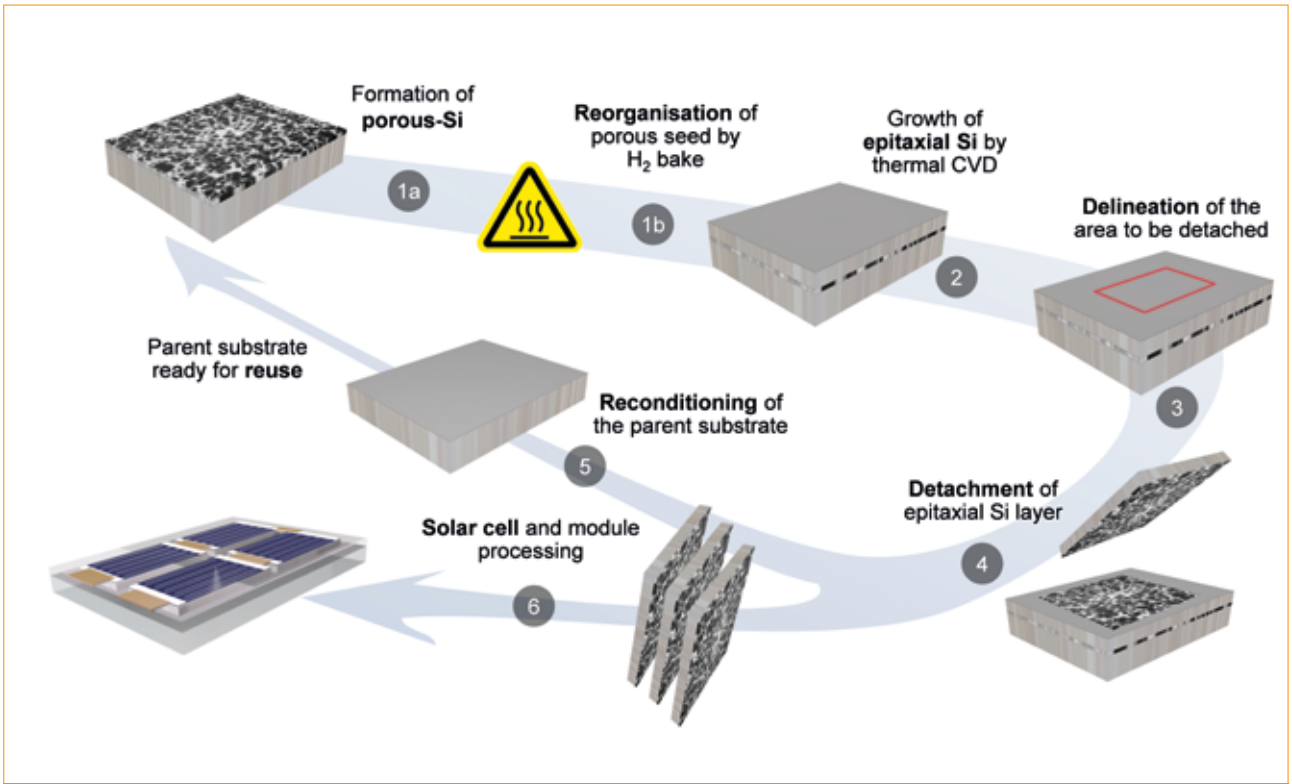

Figure 1. Fabrication of epitaxial Si solar cells and modules from porous-silicon-based epitaxial Si lift-off.

Overviews of various kerfless wafering methods or lift-off processes have been given by Henley [4], Brendel [5], McCann et al. [6], Weber et al. [7] and Bergmann et al. [8]. Currently, an extensive review [9] and a book chapter [10], providing an exhaustive update, are in preparation. Of several dozens of lift-off and kerfless routes investigated, currently one of the most extensively researched and developed routes is the porous-silicon-based lift-off of epitaxial Si. In this paper, an overview of the different technologies underpinning the potentially successful commercial exploitation of epitaxial Si lift-off is presented.

Epitaxial silicon lift-off: the technology, from seed layer to module

The process of porous-silicon-based lift-off of epitaxial Si is shown in Fig. 1. A layer of monocrystalline Si is grown from the vapour phase, using trichlorosilane (TCS) as a precursor, by homoepitaxy. The layer is grown as thin as desired, from a thickness of ~160µm (wafers) down to a few micrometres (foils). The epitaxial growth is performed on a reusable Si substrate, whose surface is porosified and sintered to enable both the growth of epitaxial Si and its subsequent detachment.

"With Si still making up a third of the final module cost, there is continued interest in reducing the cost of Si by producing thinner wafers and reducing kerf losses."

As the solar cell material is directly grown from the gas phase to the required thickness, no wafering is required, and hence no kerf loss is generated. Moreover, as growth is realized using TCS, this lift-off method offers a significant shortcut through the monocrystalline Si PV value chain, by skipping not only wafer sawing but also the expensive and energy-intensive steps of poly-Si rod fabrication (Siemens process) and Czochralski (Cz) ingot pulling. The impact of the parent substrate on the cost is significantly reduced because of its capacity for multiple reuse.

The use of porous silicon to lift off an epitaxial Si layer was pioneered by Yonehara et al. at Canon with the ELTRAN process for SOI wafers [11]; for PV applications, however, the concept was adapted independently and simultaneously by Tayanaka and Matsushita at Sony [12] and Bergmann et al. at IPE [13]. In the following 20 years, the process has seen many different embodiments and is still being pursued by different institutes (e.g. Fraunhofer ISE [14], ISFH [15,16] and imec [17,18]), and companies (Amberwave [19], Crystal Solar [20–22] and NexWafe [23]).

The following subsections explain the various steps in the epitaxial Si lift-off carousel (with reference to Fig. 1): the seed layer formation by porosification and sintering (1) before epitaxial growth (2), followed by the delineation (3) and detachment (4) of epitaxial Si. The parent substrate is then reconditioned (5) for reuse in the next lift-off cycle, while the epitaxial Si wafer/foil is processed into a solar cell (6).

Step 1: Porous silicon as the detachment layer and epitaxial template

Porous silicon (PSi) etching and sintering are at the heart of the lift-off process (Fig. 2). The surface of a monocrystalline Si substrate – the parent – is porosified up to a few micrometres in depth in stacks of different porosities, the simplest case being a double layer with a thick low-porosity layer (~20%) on top of a thin high-porosity layer (~50–60%). When this porosified substrate is loaded into an epitaxial reactor, at a high temperature (>1,000°C) and in a reducing atmosphere (e.g. H_2), its porous microstructure reorganizes. A smooth closed surface with embedded spherical voids forms in the low-porosity layer, while a cavity intermittently interrupted by pillars forms as the detachment plane in the high-porosity layer. In this way, PSi enables the homoepitaxial growth of a high-quality Si layer and its subsequent detachment from the parent substrate. Besides this, the PSi seed layer, with its high internal surface area, is a very efficient gettering centre which captures potential metallic contaminants that could enter the epitaxial Si from the parent substrate or the tool ambient atmosphere [24].

Considering its twofold key role in epitaxial Si lift-off, the porosification step is paramount to the success of the lift-off process and therefore requires tight process control. Porosification is realized by electrochemical etching in an HF-based electrolyte [25]. The Si substrate to be porosified is used as the anode of the electrochemical cell, and a current is applied to create pores at the surface. A surfactant, such as alcohol, is used to achieve

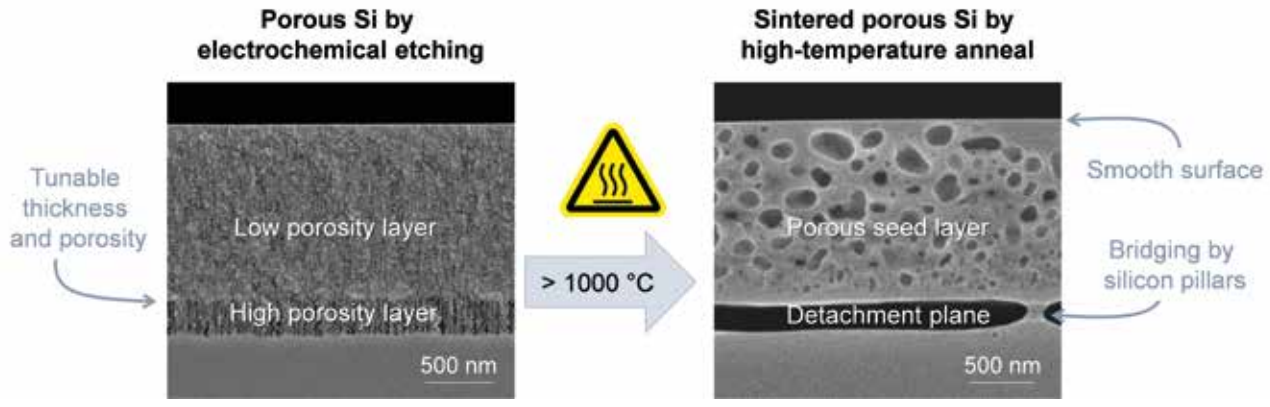

Figure 2. Scanning electron microscopy (SEM) cross sections of a double layer of porous silicon: (a) as-etched, and (b) after reorganization in an epitaxial reactor, offering a smooth epitaxial growth template at the surface and a cavity underneath for the release.

efficient evacuation of the H_2 bubbles produced during the process. The advantage of using electrochemical etching is that the porosity can simply be controlled by the applied current density, while the layer thickness can be controlled by the etch time. However, other parameters influence the pore morphology (dimension, shape, etc.), in particular the substrate doping type and concentration, and the electrolyte composition. In practice, p^{++} substrates are used, as they can be easily contacted electrically and do not require illumination as n-type substrates do. The combination of high current (e.g. 80mA/cm²), flammable compounds (H_2, alcohol) and toxic chemicals (HF) used in PSi fabrication calls for ingenious tool design in order to meet safety and layer quality requirements.

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In common porosification tools, the parent substrate is clamped along the edge using an O-ring, which creates an unporosified rim along the substrate edge. This means that the epitaxial Si on this rim cannot be detached, and will become thicker and thicker with every reuse cycle (see 'Reuse of the parent substrate' section below). In tools that enable etching of the complete substrate area, epitaxial Si over the entire area can be released; however, this requires the removal of the epitaxial overgrowth on the edges to release the layer (see 'Delineation of the epitaxial Si foil' section below).

PSi sintering is as critical as porosification to the lift-off process. Upon sintering, the extremely high surface area causes the pores to transform and merge in order to minimize the total surface energy. Theories based on vacancy diffusion [26,27] and stress minimization [28] have been used to explain this microstructure transformation. Pores smaller than a critical radius (which depends on the vacancy supersaturation and residual stress) shrink, feeding larger ones, and, like connecting vessels, pores and voids in the porous stacks mutually interact, until an equilibrium stack is formed. The dependence of the microstructure transformation on the porosity and thickness of the different layers has been investigated in detail [27,29,30]. In addition, the evolution of the residual stress in porous silicon, before and after sintering, in single and double layer stacks has been studied [31,32]. Understanding, and thus predicting, the evolution of the porous stack during sintering is key to optimizing PSi as an epitaxial seed and detachment layer.

Step 2: Epitaxial silicon growth on porous silicon

The growth of the epitaxial Si layer is performed *in situ* on the sintered PSi, by deposition from the vapour phase. The most commonly employed technique is atmospheric pressure chemical vapour deposition (CVD) with trichlorosilane (TCS) as a precursor. Taking place at 1,000–1,200°C, this method ensures the growth of a high-quality monocrystal on the crystalline porous seed surface, at a high growth rate of up to 10µm per minute. The epitaxial Si layer can be grown as thick as desired (20–160µm reported), by tuning the deposition time, and with n- and/or p-type doping with the desired concentration and depth profile by controlling the dopant gas. What can be produced is therefore not just a bare photoactive layer, but also a partially processed solar cell 'precursor' with integrated emitter, back-surface field and front-surface field all in a single process, and tailored to one's needs (Fig. 3). Other noteworthy assets of epitaxial growth are its potential for a narrower spread in crystalline quality and resistivity than in the case of a Cz ingot, and the natural low concentration of O interstitials, compared with Cz Si [20]. These two characteristics respectively result in a tighter solar cell bin for module assembly, and the absence of light-induced degradation.

The recently reported minority-

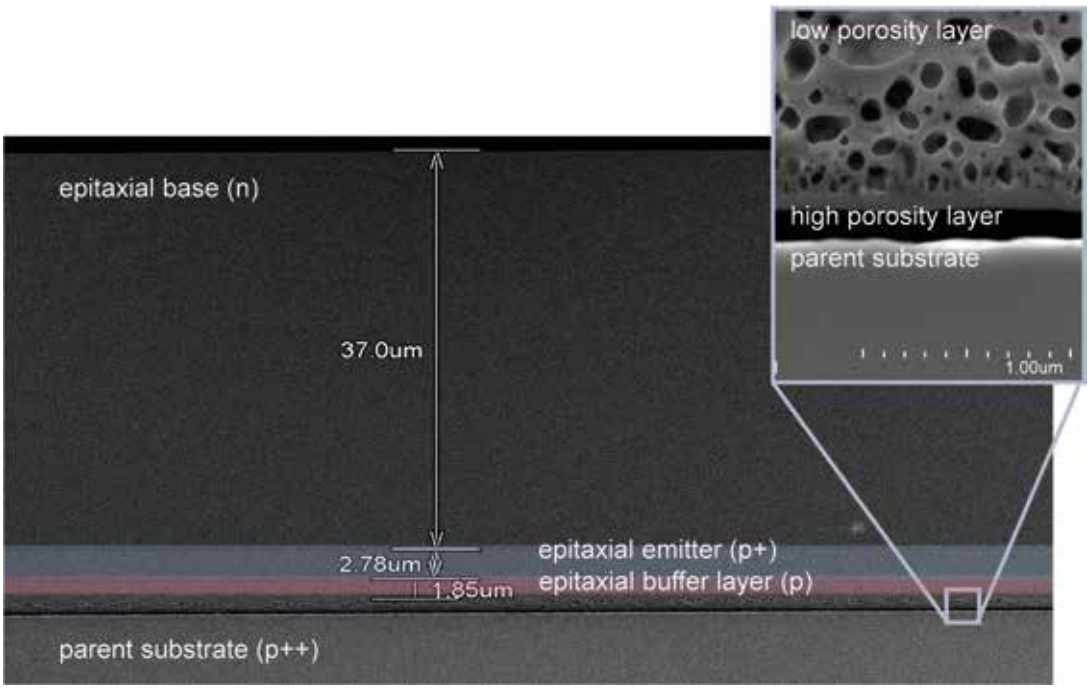

Figure 3. Cross-sectional SEM image of a 40µm-thick epitaxial Si foil with integrated emitter on top of the porous seed layer (inset).

carrier lifetimes in epitaxial Si are spread over a wide range: 30–700µs for epitaxial foils, referred to as *epifoils* (<70µm) [29,33], and 1–4ms for epitaxial wafers, referred to as *epiwafers* (>100µm) [16,21,22]. The wide range illustrates that many factors influence the material quality. While the nature of the incorporated crystalline defects that influence the quality of Cz and float zone (FZ) silicon is well understood, the array of defects that determine the properties of epitaxial Si is still under investigation.

One of the main factors influencing epitaxial Si quality is the condition of the porous silicon seed layer. The presence of pits and bumps or pronounced roughness at the surface will result in the formation of extended crystalline defects, such as nested stacking faults [14], which have been shown to significantly reduce the minority-carrier lifetime. Additionally, the stress state of the porous seed *below* the surface could also affect the epitaxial Si quality. A higher residual stress, in combination with a rougher surface, has been proven to result in a higher defect density and lower minority-carrier lifetime [29].

A second important factor to be controlled is the material purity. All the process steps up to and including epitaxy require very stringent contamination standards. It has, for instance, been reported that Pt, which is a common cathode material for porosification, has been found in the epitaxial Si, resulting in a reduction in minority-carrier lifetime [34]. More and more attention is now also turning towards intrinsic point defects, which seem to be related to the cooling rate in the epitaxial reactor. A fast cooling rate is also suspected to introduce stress, which could affect the material properties. Slower cooling rates and gettering steps are currently being investigated in order to understand their importance in achieving higher minority-carrier lifetime.

Step 3: Delineation of the epitaxial Si foil

Before the epitaxial Si layer can be detached from the parent substrate, the area to be lifted off needs to be delineated in order to release the edges of the soon-to-become kerfless wafer/foil. Delineation is a crucial step because it defines the wafer edge microstructure, which influences the mechanical strength of the resulting epitaxial Si wafers or foils. A delineation method that leads to a high density of edge defects significantly increases the breakage rate during subsequent handling, manipulation and cell processing [35,36]; this cannot be tolerated in the cost-sensitive PV industry, where yield is of utmost importance [3].

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In the conventional Cz wafer production route, the sawn edges of the ingot are polished to ensure defect-free, high-quality edges, which in turn ensures high mechanical strength. For epiwafers or epifoils, the delineation method must be chosen in such a way that high-quality edges are produced, if possible ab initio, while maintaining a high throughput and a low capital cost.

The most common method for delineation is laser ablation (LA) [20,37,38]. During LA, the laser energy is absorbed by the Si and converted mainly into heat, resulting in the localized melting and expulsion of material from the heated spot, which leads to a V-shaped groove, as shown in Fig. 4(a) and (b). The depth can be well controlled so that the laser groove reaches the bottom of the epitaxial Si without damaging the parent substrate. The side wall of the laser groove (which eventually forms the epitaxial Si wafer edge), however, is severely damaged; this defective region is known as the *heat-affected zone (HAZ)*. The extent of the HAZ is strongly dependent on the laser parameters, in particular the duration of the laser pulse, which can be of the order of nanoseconds (ns-LA), picoseconds (ps-LA) or femtoseconds (fs-LA). Shorter pulsed laser sources cause less thermal damage, and could therefore result in higher mechanical strength; however, very short pulsed laser sources, such as fs-lasers, are much more expensive than ns-lasers.

A novel variant of laser ablation is multi-beam laser ablation (mb-LA), developed by ALSI [39]. In this technology, a nanosecond laser source is split using a diffractive optical element (DOE) into an array of smaller beams, each with a lower fluence.

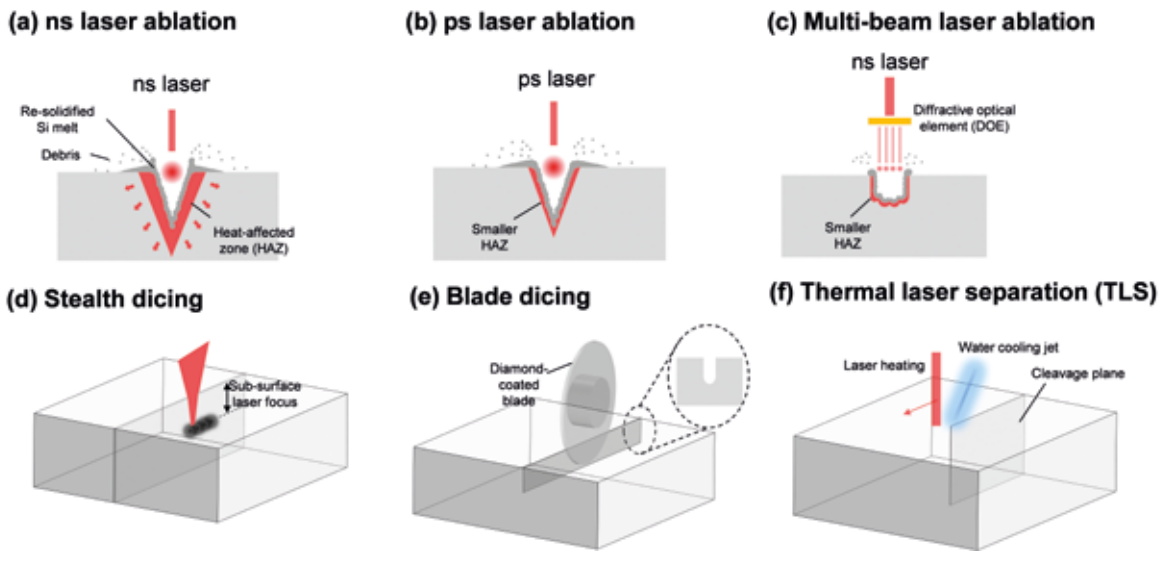

Figure 4. Different delineation methods for defining the area of the epitaxial silicon to be lifted off: (a) nanosecond laser ablation (LA), (b) picosecond LA, (c) multi-beam LA, (d) stealth dicing, (e) blade dicing, and (f) thermal laser separation (TLS).

Since each child beam delivers lower power, the resulting thermal damage is considerably less than in the case of conventional ns-LA (Fig. 4(c)). Moreover, since an array of multiple spatially separated beams are used, the dicing process can be accomplished in a single pass at high speed. Additionally, ALSI has also developed a novel process called *VDOE*, in which the defective HAZ at the top of the laser groove is removed [40]; as a result, the use of this process can result in wafers with higher mechanical strength.

Blade dicing is the workhorse for die separation in the microelectronics industry (Fig. 4(e)), and can be readily applied to the delineation of epitaxial Si. In this process, a circular rotating blade with embedded diamond abrasive particles slices through silicon in a water-cooled environment. The resulting cut shows striations on the side walls and chips at the surface, but is in general much less detrimental to the foil strength than laser-ablated side walls.

Stealth dicing, a novel technique developed by DISCO and Hamamatsu, also for use in the microelectronics industry, utilizes a pulsed infrared laser source that is focused at a depth well below the surface of the Si. When the power density at the focal depth exceeds a critical value, a subsurface-damaged (SD) layer is created. When an external force is applied, cracks propagate from this SD layer towards the surfaces (Fig. 4(d)). The main advantage of stealth dicing is that the defective region can be localized in the middle of the wafer/foil edge, close to the neutral axis, away from the surfaces, where the highest mechanical stresses are experienced while handling or processing.

Finally, another novel technique that has gained attention recently is thermal laser separation (TLS), developed by 3D-Micromac; here, a continuous wave laser source is used to heat Si locally, accompanied by a cooling water jet (Fig. 4(f)). This causes significant localized thermomechanical stresses, which are used to guide a crack from a predefined location along the path of the moving laser and water jet [41]. Since the mechanism is stress-induced cleaving of Si, the wafer edges are defect free. The use of this technique for epitaxial Si lift-off can be quite challenging if the cleavage of only the epitaxial silicon above the detachment plane is desired. However, in the rimless PSi approach (see 'Porous silicon as the detachment layer and epitaxial template' section above) this technique could be readily

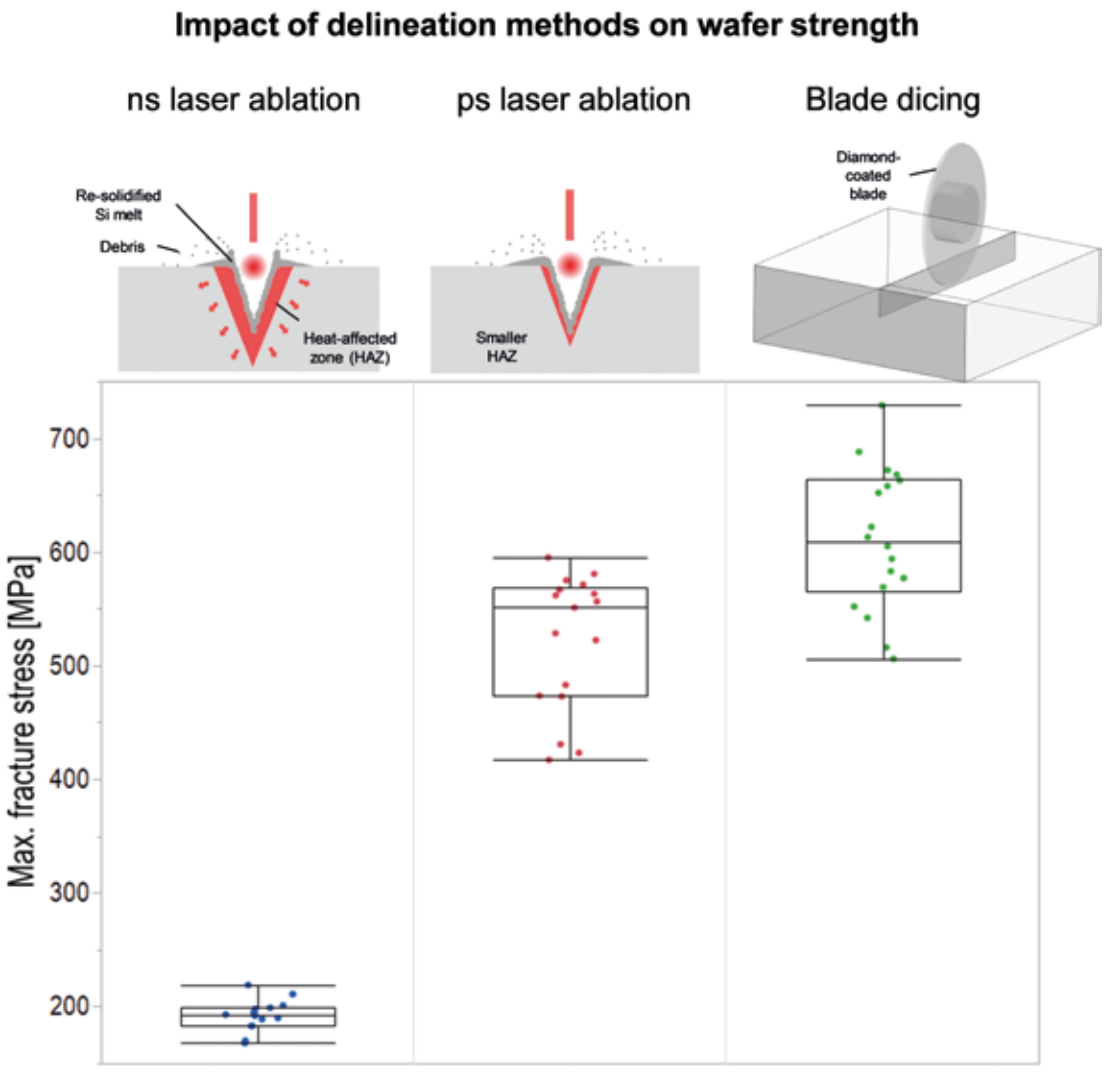

Figure 5. Comparison of the maximum fracture stress of Si diced using three different dicing methods, namely ns-LA, ps-LA and blade dicing (Si thickness: 136µm; size: 6cm × 0.5cm).

employed to simply cut through the epitaxial layer overgrowth at the edges, thus releasing the edges of the epitaxial Si before detachment.

To assess the quality of the edges produced by the different dicing methods, four-line bending tests were performed on 136µm-thick silicon wafer pieces (6cm × 0.5cm), diced using different techniques. A comparison of the mechanical strength of Si resulting from ns-LA (reference process), ps-LA and blade dicing is shown in Fig. 5. As expected, the thermal damage during LA significantly affects the mechanical strength compared with blade dicing. Moreover, the best ps-LA process significantly outperforms the best ns-LA process, owing to the lower HAZ on the side walls [36].

The impact of the dicing methods on the detachment yield and processing yield of thin Si epifoils is currently under evaluation. This should provide information on a set of dicing methods suitable for the Si delineation step, which is not only limited to epitaxial Si lift-off but also more generally applicable for other kerfless methods, as well as for other applications such as the dicing of cells into half cells [41].

Step 4: Detachment from the parent substrate

As described earlier, the detachment layer is a lateral cavity between the parent substrate and the epitaxial silicon layer, interspersed with pillars that connect and hold the epitaxial silicon and the parent substrate together. During the detachment process, these pillars must be broken or dissolved in order to release the epitaxial Si layer from the parent substrate.

While chemical dissolution of the Si pillars may be envisaged, the most common and practical way to rupture the pillars is to simply pull the epitaxial Si and parent substrate apart. Most institutes utilize distributed vacuum chucks to grip and pull them apart in a perpendicular direction to the detachment plane. Since the cross-sectional area of the pillars is only 2–3% of the total area of the wafer surface where the pulling pressure is applied, the stress on them is magnified manyfold, ensuring that the fracture stress of Si is preferentially exceeded at the pillars in the detachment plane, leading to the release of the epitaxial layer [30,38].

A proprietary curved vacuum chuck has been developed at ISFH to implement a peeling force on the pillars, whereby the epitaxial layer is peeled off the parent substrate starting from one corner of the delineated area [38]. This further reduces the external force needed for detachment, since the force is sequentially applied to a small number of pillars at the border of the detachment front, rather than to the entire area of epitaxial silicon. At imec, a similar idea is used, where the detachment front is propagated from one edge or corner of the delineated area, by manually exerting small bending forces. The propagation of the detachment front can be detected using photoluminescence imaging, as shown in Fig. 6.

> "A high detachment success rate close to 100% is crucial for the economic viability of the concept."

Detachment problems occur when defects in the detachment plane prevent the release of the epitaxial Si, often leading to no/partial detachment or breakage. A high detachment success rate close to 100% is crucial for the economic viability of the concept; this is because a failure to detach means not only a reduction in yield in epiwafer production but also a possible yield loss associated with the parent substrate if it cannot be reliably reused. Thus, studying and tackling detachment defects is very important.

The ease of detachment depends on both the density and the size of the pillars [30]. The surfaces of different parent substrates after detachment are shown in Fig. 7. When pillar density is low and the pillars are small (Fig. 7(a)), detachment is easy. However, when either pillar density is high (Fig. 7(b)) or pillars are large (Fig. 7(c)), or both of these are true, detachment is difficult, sometimes leading to partial or no detachment. If the pillar or detachment defect is sufficiently large, the plane of cracking can be deflected into the epitaxial Si, resulting in cracks or holes in the epitaxial layer.

It is possible to differentiate two types of detachment defect: systematic and sporadic. *Systematic defects* can be remedied by control and optimization

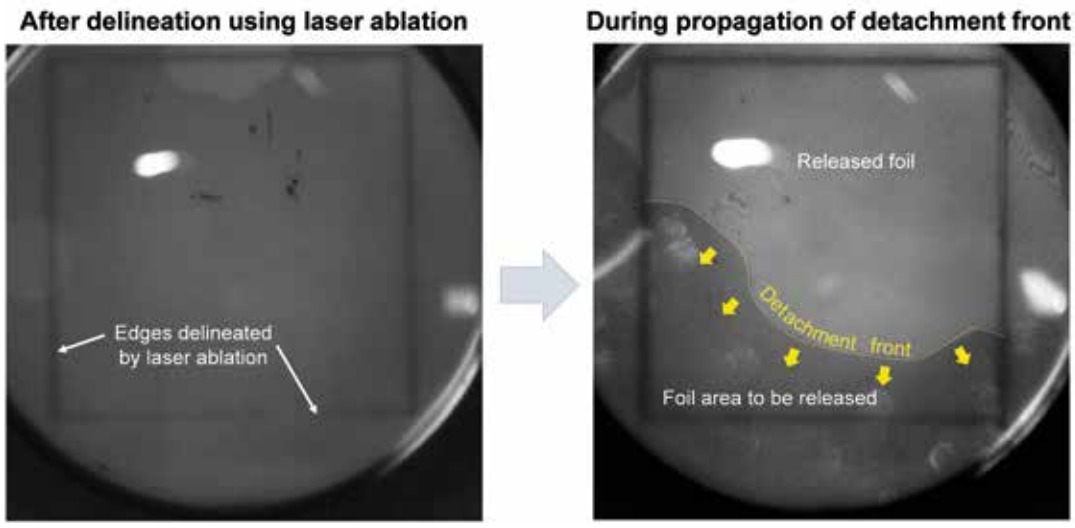

Figure 6. Photoluminescence (PL) images showing the propagation of the detachment front from one edge of the delineated epitaxial Si area to the other edge (the white stains are reflection artefacts).

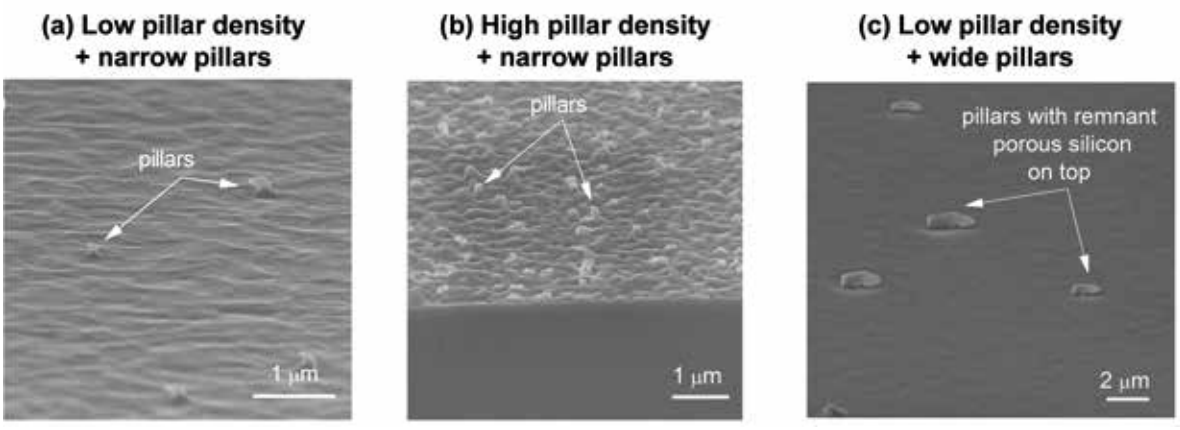

Figure 7. SEM images (tilted view) of the parent substrate surface after detachment [from 30], showing broken pillars, with: (a) low pillar density and small size; (b) high pillar density and small size; and (c) low pillar density and large size.

of the porosification and sintering conditions; for example, high pillar density in the detachment plane can be reduced by increasing the thickness of the low-porosity layer, which acts as a vacancy supply layer for the high-porosity layer during sintering [30]. Another way to deal with these defects is to infiltrate the detachment plane with a liquid, such as water, and use ultrasonication to produce cavitation-induced damage to the pillars, thus weakening them and making detachment easier [30]. High pillar density can also be tackled by using a different detachment method; for example, an extreme case of detachment at a non-reorganized porous silicon layer has been demonstrated in the ELTRAN process, using a high-pressure water jet [42].

Sporadic defects, on the other hand, are a statistical occurrence and can be much more detrimental to detachment. For example, the presence of a large particle on the parent substrate surface prior to porosification could prevent the formation of PSi underneath this particle, leading to a large zone where the detachment plane is absent. Such defects may be dealt with by stringent statistical process control of surface defect density prior to porosification. Other novel methods to address these defects are currently under consideration.

Step 5: Reuse of the parent substrate

After detachment of the epitaxial Si, the parent substrate enters the next cycle of epitaxial Si wafer/foil production. This repeated use of the parent substrate is the cornerstone of the cost savings that the epitaxial Si lift-off concept promises. Rough estimations show that the number of cycles that a parent substrate undergoes is a key parameter in the cost advantage of epitaxial Si wafers over Cz Si wafers [43].

Successful reuse means delivering epitaxial Si with a stable lifetime and detachment yield, cycle after cycle. The parent substrate properties, however, become altered along the process sequence: its surface doping is modified by the high-temperature anneal in H_2 [44], and the detachment process leaves various defects, such as pits and bumps, or possible delineation traces. Moreover, epitaxial Si remnants, such as 'flaps' (detachable epitaxial Si outside the delineated area) connected to the undetachable rim, are left behind after delineation. The parent substrate must therefore be recovered by a reconditioning step, which removes these imperfections to a large extent, with minimal material losses and risk of breakage.

The first report of reuse appeared in the literature in 2001 [45]; since then, there have been reports of more than 50 reuses with stable material quality, indicating that the challenge of multiple reuses can be overcome [20,46,47]. However, little has been communicated on the reconditioning methods. In the documented works, acidic and alkaline wet chemical etching and cleaning have been proposed [44,46,48], to remove a few micrometres of the defective surface and restore sufficient surface smoothness. Some works, however, have reported a degradation of epitaxial Si quality over time, corresponding to increases in surface roughness and defect density, and consequently to decreased minority-carrier lifetime [48,49].

The main concerns for parent substrate reuse are threefold. First, the pits and bumps that result from inevitable defects in the detachment layer may be too large to be smoothened out, at least without extensive parent substrate dissolution during polishing. If this is the case, the next generation of epitaxial Si will be affected by the same defect, and the parent substrate will eventually become unusable (Fig. 8). The solution here is to avoid formation of wide defects in the first place, by achieving a nearly perfect detachment plane, as discussed in the section on detachment from the parent substrate.

Second, the non-porosified wafer rim (see 'Porous silicon as the detachment layer and epitaxial template' section above) leaves, cycle after cycle, a thicker and thicker step, since epitaxial Si that is grown on the rim cannot be detached. Such a large step may prevent processing in certain tools or lead to non-uniformities during porosification or epitaxial deposition. On the other hand, this rim offers a strong support while the substrate is becoming thinner and thinner, further extending the number of reuse cycles. If the step at the edge is to be avoided, then a rimless porosification system is necessary.

Third, and finally, it is important to note that the parent substrate is being cycled through many processes – involving several chemical, thermal and stress cycles – until the detachment of the foil. Any extra step adds to the wafer history: thermal stress upon annealing, mechanical stress upon fixture, potential contaminant in-diffusion, and risk of breakage while handling or processing. The simpler and fewer these steps, the longer the lifetime of the parent substrate could be.

Step 6: Processing of thin Si

As mentioned earlier, recent technological developments have

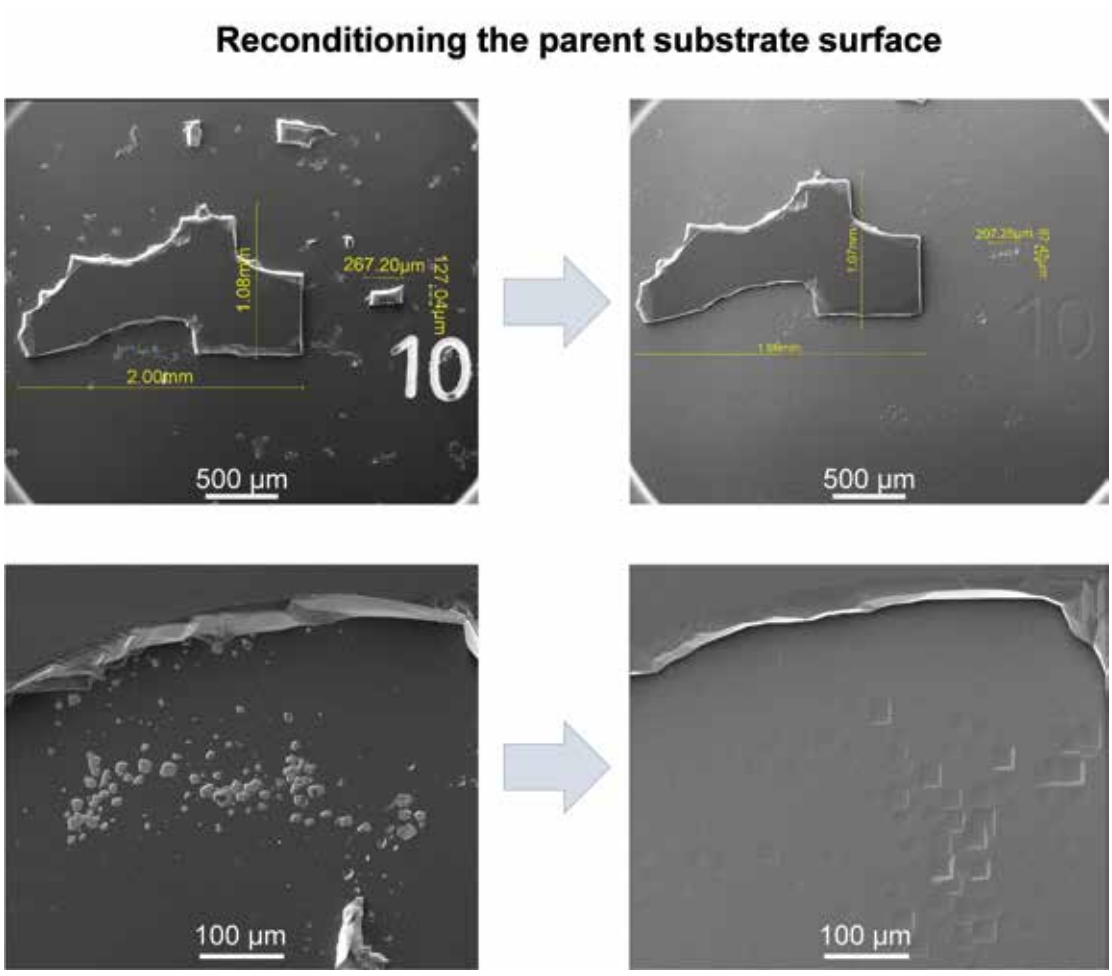

Figure 8. Upon reconditioning by wet chemical etching (here 5µm was removed by TMAH), micrometre-scale defects (such as pillars) are easily dissolved and the surface smoothened out, while larger detachment defects (leading to undetachable epitaxial silicon remnants) remain. Specific markers, such as '10', were used to locate the same region before and after reconditioning.

enabled extremely high epitaxial Si deposition rates of 5–10µm per minute [20,50,51]. This opens the door for growing epitaxial Si wafers of up to ~160–180µm, giving considerable flexibility in the choice of epitaxial Si thickness. Above 100µm, the epitaxial silicon is reasonably rigid and is referred to as an *epiwafer*; below 70µm, the increased flexibility suggests the use of the term *epifoil*.

Epiwafers, by virtue of their rigidity, can be directly used as drop-in wafers in a cell production line, as a replacement for Cz wafers, and sequentially processed into cells, assembled, interconnected and laminated into modules. However, processing thin Si epifoils is a challenging endeavour, owing to their fragility, light weight and high degree of flexibility, and the general consensus is that the mechanical yield loss during handling and processing of Si wafers increases exponentially with decreasing wafer thickness [52–54].

Handling has been reported to be the major cause of mechanical yield loss for thin Si [52]. Automated handling systems in the PV industry are designed and optimized to handle rigid wafers. Foils, however, are highly flexible and bend easily during handling operations, leading to errors and slowdowns in automated handling systems; these issues will impact throughput in an industrial production line. Thus, novel solutions that take into account the unique properties of thin foils must be investigated.

Similarly, different cell process steps entail their own set of challenges when applied to thin foils. For example, during wet processing in cassettes, the electrostatic charges on foil surfaces result in an attractive force between neighbouring foils, causing them to bow and stick together; as a result, the spacing between neighbouring foils must be increased, which translates into lower throughput. Another example is that the asymmetric deposition of dielectrics or metals can cause foils to bow or warp, which is an issue for further processing of these foils.

The challenges of processing freestanding thin Si foils can be completely circumvented by layer transfer of thin Si foils onto a foreign carrier. This type of transfer process has been demonstrated on a variety of rigid foreign carriers, such as ceramic substrates [55–57], metal substrates/metal foils [58,59], highly-doped low-cost conductive Si substrates [60] and superstrates such as glass [18,61–63] or plastics [12]. A detailed overview of the various efforts will be given in forthcoming publications [9,10].

A survey of the various studies conducted by different groups in

Institute [Reference]	Thickness [µm]	η [%]	Cell area [cm^2]	Si sample area [cm^2]	Configuration during processing
Epifoils					
Amberwave/UNSW [58]	18	16.8	4	NR	On parent + steel substrate
ZAE Bayern [67]	25	15.4	3.9	78.5 / 4	On parent + freestanding
IPE [68]	41.6	16.9	2	NR	On parent + glass superstrate
ISFH [15]	42.9	19.1	3.98	6.25	Freestanding
Solexel [47]	43	20.6	243	243	Bonded
imec [64]	47	17.0	16	156.3	Freestanding
imec [63]	47	16.0	4	156.3	Bonded to glass
Epiwafers					
ISE/NexWafe [14]	150	20.0	4	78.5	Freestanding
Crystal Solar/Choshu [22]	150	23.0	243.4	243.4	Freestanding
Crystal Solar/imec [21]	180	22.5	238.45	240	Freestanding

Table 1. Examples of solar cells on epifoils (<70µm) and epiwafers (>100µm), achieved by handling using various configurations. (NR = not reported.)

Strengths: kerfless high-quality silicon at lower costs	Weaknesses: the chasm between lab demos and industrial production
1. Kerfless production of wafers/foils. 2. Shortcut in the PV value chain: no Siemens process, Cz pulling and wafer sawing. 3. Independent from poly-Si supply and cost. 4. Use of lower temperatures than with Cz pulling. 5. Value-added wafers: grown-in junctions, deep junctions. 6. Excellent dopant control allows low wafer-to-wafer variations and unique dopant profiles. 7. Thickness can be tuned as desired. 8. Tuneable wafer area/shape.	1. Development of epitaxial reactors and porous silicon etchers with ever-increasing throughput targets is challenging. 2. TCS-to-epitaxial Si conversion rate (i.e. TCS utilization rate) is not 100%. 3. Purification and recycling of exit gas mixture are crucial. 4. Logistically challenging, since epitaxial reactor must be in close proximity to the TCS manufacturer. 5. Multiple reuse of the parent substrate is critical for cost savings. 6. Porosification in large quatities raises safety concerns.
Opportunities: paradigm shift towards thin wafer adoption in industry	**Threats: the comfort zone**
1. Higher Si utilization (thinner wafers, minimal kerf loss) keeps driving the PV industry. 2. Light-induced degradation is a major issue for Cz wafer modules. 3. Development of novel thin wafer handling technologies and systems opens doors for thin Si. 4. Development of advanced optical confinement methodologies enables use of thin Si. 5. Requirements of flexible or curved modules in building-integrated PV (BIPV) systems raises need for thin Si. 6. Epitaxial lift-off is one of the more advanced kerfless technologies in terms of Si quality and technological maturity.	1. Cost advantage of epiwafers over Cz wafers is decreasing. 2. PV manufacturing is highly sensitive to yield loss, and higher breakage rate of thinner wafers is a discouraging factor. 3. There may be resistance to adopting novel handling technologies for thin wafers/foils if cost advantage is not sufficiently high. 4. Successful technological advancement and investments in other kerfless technologies compete with epitaxial Si lift-off as the next-generation kerfless technology of choice.

Table 2. SWOT matrix.

processing epitaxial Si foils and wafers into solar cells is summarized in Table 1. A variety of different solar cell technologies have been employed: heterojunction solar cells [64], PERC/PERL solar cells [15,65] and interdigitated back-contact (IBC) solar cells [66], in both freestanding and bonded configurations. In all these efforts, the maximum area of thin Si foil processed in a freestanding configuration is limited to 156.25cm^2, in order to reduce mechanical yield losses. Thick epitaxial silicon wafers, on the other hand, do not have such a size limitation. With supported processing, size is not a constraint and large-area Si foils can be readily processed into cells, keeping in mind the constraints of processing a complex bonded stack.

SWOT analysis of epitaxial Si lift-off technology

Epitaxial Si as a replacement for Cz wafers implies a wealth of changes to PV module manufacturing. This section discusses, in the form of a SWOT (strengths, weaknesses, opportunities and threats) analysis, the unique selling points as well as the Achilles' heels of this technology, in relation to the present and future technologies that will continue to shape the PV industry. Table 2 presents the SWOT matrix, according to the authors' best knowledge.

> "The struggle is now to establish the industrial viability of the epitaxial Si concept."

Conclusion and outlook: at a watershed

Epitaxial Si lift-off technology is currently a top candidate for the production of kerfless and low-cost monocrystalline Si wafers in the PV

industry. It offers wafers as thin as desired, with inbuilt doping profiles, at substantial cost and energy savings compared with Cz wafers.

Beginning with efficiencies of 12.5% in 1998, to today's record cells yielding 20.6% on foils [47] and 23.0% on wafers [22], several institutes and companies have demonstrated the high quality of their epitaxial Si. The struggle is now to establish the industrial viability of the epitaxial Si concept. The contest is, however, very difficult, with critically low margins for PV manufacturers, and the decreasing Cz wafer cost further narrowing the economic advantage. With one company having left the game (Solexel) and three companies still pursuing this concept (Amberwave, Crystal Solar and NexWafe), epitaxial Si lift-off technology is at a watershed. Whether the remaining participants will now find their place in the PV sun or fade away is strongly dependent on whether PV manufacturers and investors will be able, and willing, to take the risk of leaving the comfort zone of Cz wafer processing and integrating in the near future a longer-term solution.

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