

Failure analysis of design qualification testing: 2007 vs. 2005

G. TamizhMani, B. Li, T. Arends, J. Kuitche, B. Raghuraman, W. Shisler, K. Farnsworth, J. Gonzales, & A. Voropayev, Arizona State University Photovoltaic Testing Laboratory (ASU-PTL), Mesa, Arizona, USA

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ABSTRACT

Design and performance qualification testing of PV modules consists of a set of well-defined accelerated stress tests with strict pass/fail criteria. ASU-PTL is an ISO 17025-accredited testing laboratory and has been providing photovoltaic testing services since 1992. This paper presents a failure analysis on the design qualification testing of both crystalline silicon (c-Si) and thin-film technologies for two consecutive periods: 1997-2005 and 2005-2007. In the first period, the industry was growing at a slower rate with traditional manufacturers, with qualification testing of c-Si technologies being primarily conducted per Edition 1 of the IEC 61215 standard. In the second period, the industry was growing at an explosive rate with new manufacturers joining the traditional manufacturers, while qualification testing of c-Si was primarily conducted per Edition 2 of IEC 61215. Similar failure analysis according to IEC 61646 has also been carried out for thin-film technologies. The failure analysis of the test results presented in this paper indicates a large increase in the failure rates for both c-Si and thin-film technologies during the period of 2005-2007.

Introduction

The design qualification certification (per IEC 61215/1646 or IEEE 1262 standard) is a market-driven requirement and the safety certification (per IEC 61730 or ANSI/UL 1703 standard) is a regulatory-driven requirement. The design qualification testing is a set of well-defined accelerated stress tests – including irradiation, environmental, mechanical and electrical tests – with strict pass/fail criteria. The qualification testing does not, as anticipated, identify all the possible reliability issues in the actual field; however, it does identify the major/catastrophic design quality issues. The qualification

testing may be considered as the minimum requirement for the reliability testing. The type, extent, limits and sequence of the accelerated stress tests of the qualification standards have been stipulated with two goals in mind. The goals are to accelerate the same failure mechanisms observed in the field without causing failures that do not occur in the field, and to induce these failure mechanisms in a reasonably short period of time, usually 70-120 days.

ASU-PTL has issued more than 300 design qualification and type approval certificates for manufacturers worldwide. Studies have been carried out in relation to accelerated qualification testing for

crystalline silicon technologies per IEC 61215 standard [1,2,3]; accelerated reliability testing (for example, prolonged accelerated stress testing until failures are induced) for crystalline silicon (c-Si) technologies [4]; and accelerated reliability testing for thin-film technologies [5].

In the case of thin-film technologies, the qualification testing was conducted per IEC 61646 in both periods under discussion in this paper. Since there was no second edition of IEC 61646 at the time of this study, the change in failure rates for the second period relate only to the combined influence of new and traditional manufacturers.



Figure 1. The ANSI/UL 1703 Temperature test is performed in ASU-PTL's test field.

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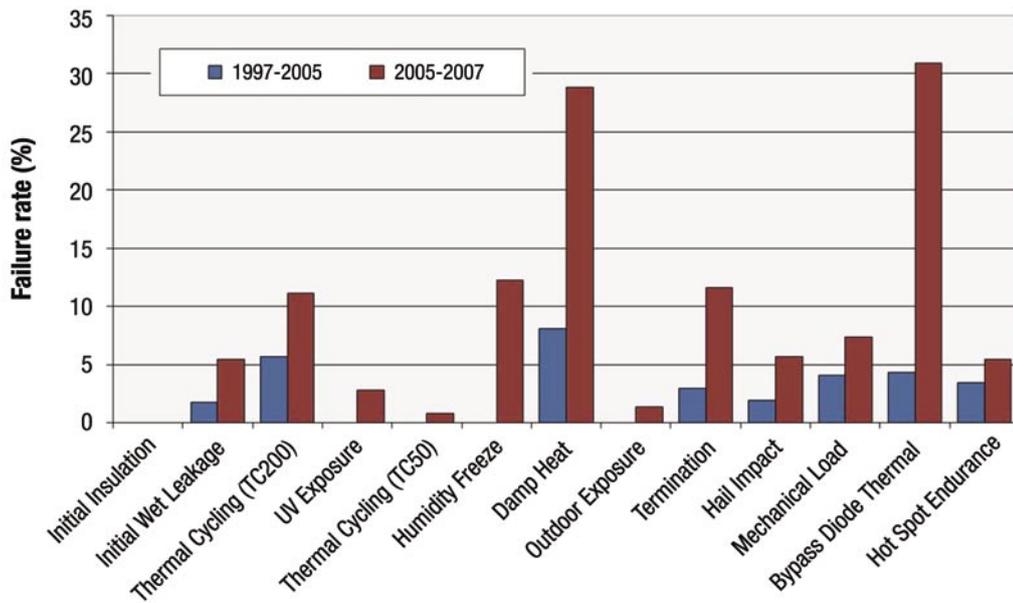


Figure 2. Failure rate comparison of crystalline silicon modules for the 1997-2005 and 2005-2007 periods.

Methodology

In the 1997-2005 period, approximately 1200 modules were tested, while the 2005-2007 period saw the testing of approximately 1000 modules. About 90% of the modules tested were crystalline silicon modules and were tested according to the IEC 61215 and IEEE 1262 standards (mostly according to the IEC 61215 standard as the IEEE 1262 standard was withdrawn in 2000). About 10% of the modules in question were thin-film (amorphous-silicon, cadmium telluride and copper indium selenide) modules and they were tested according to the IEC 61646 standard. The results are presented and discussed in the following two sections.

Results and discussion

Failure rates: 2005-2007 vs. 1997-2005

The failure rates of crystalline silicon modules and thin-film modules in various accelerated and non-accelerated tests of the qualification standards are presented in Figures 2 and 3 respectively. As shown in these two figures, the failure rate has dramatically increased in the 2005-2007 period as compared to the 1997-2005 period. For example, in crystalline silicon technology, the failure rates of the key tests are (2005-2007 vs. 1997-2005): initial wet resistance (5% vs. 2%); diode thermal (31% vs. 4%); damp heat (29% vs. 8%); humidity freeze (12% vs. 0%); and 200 thermal cycles (11% vs. 6%). In the thin-film technology, the failure rates of the key tests are (2005-2007 vs. 1997-2005): initial wet resistance (20% vs. 1%); damp heat (70% vs. 28%); humidity freeze (17% vs. 6%); and 200 thermal cycles (20% vs. 0%).

A disturbing find is that the modules fail at an alarming rate (5% for c-Si and 20% for thin-films) even in the initial, out-of-the-box wet resistance test. These out-of-the-box,

non-accelerated test failures can be easily avoided by the manufacturers via inline- or spot-checking of the production modules. Another major observation is that the failure rate for the major accelerated tests such as damp heat, thermal cycling and humidity freeze tests has more than doubled or tripled for the current modules. On one hand, for c-Si, the majority of the damp heat or humidity freeze failure is related to the post-wet resistance test (an additional post-test in Edition 2) rather than post-visual and post-performance tests combined.

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On the other hand, for c-Si, the majority of the thermal cycling test failure is related to the post-visual and post-performance tests rather than the post-wet resistance test. The post-wet resistance test failure occurs primarily around the junction boxes. The post-performance failures in the thermal-cycling and ultraviolet chamber tests are significantly influenced by the shorting problems related to the bypass diodes. The shorting problems of the bypass diodes appear to be associated with the prolonged thermal stresses of the diodes in the chambers. The diode failures, even in the ultraviolet chamber maintained at 60°C over a few weeks, warrant a pre-screening or pre-qualification of the diodes before they are installed in the modules. Because of this diode problem, the module manufacturers are penalized by having to repeat the entire test sequence or the entire test program with new diodes.

The proposed pre-qualification of diodes is expected to reduce the testing time and cost for the module manufacturers. The most severe test for the thin-film modules is the damp heat test at a failure rate of 70%. About 86% of this failure is related to the post-wet resistance test rather than the post-visual and post-performance tests.

Failure rates: IEC 61215 (edition 1) vs. IEC 61215 (edition 2)

The major differences between Editions 1 and 2 of the accelerated tests of the IEC 61215 standard lie in the thermal cycling (200 cycles) test and bypass diode thermal test.

Thermal cycling test

The purpose of the thermal cycling test is to determine the ability of the module to withstand thermal mismatch, fatigue and other stresses caused by repeated changes in temperature. The test in Edition 2 of the standard is the same as that in Edition 1 except that the new edition requires application of peak power current during thermal cycling when the module temperature is above 25°C. For a set of manufacturers, ASU-PTL had conducted tests according to both Editions 1 and 2 of the standard. Table 1 compares the Edition 1 and Edition 2 thermal cycling test results obtained for nine different manufacturers. All of the thermal cycling failures presented in Table 1 are related to the post-performance test. Out of nine manufacturers' modules, four manufacturers' modules failed in the Edition 1 thermal cycling test, whereas only one manufacturer's modules failed the Edition 2 thermal cycling test. Interestingly, it appears that almost all of the traditional manufacturers had effectively addressed the thermal cycling failure issue during the first period itself. This analysis indicates

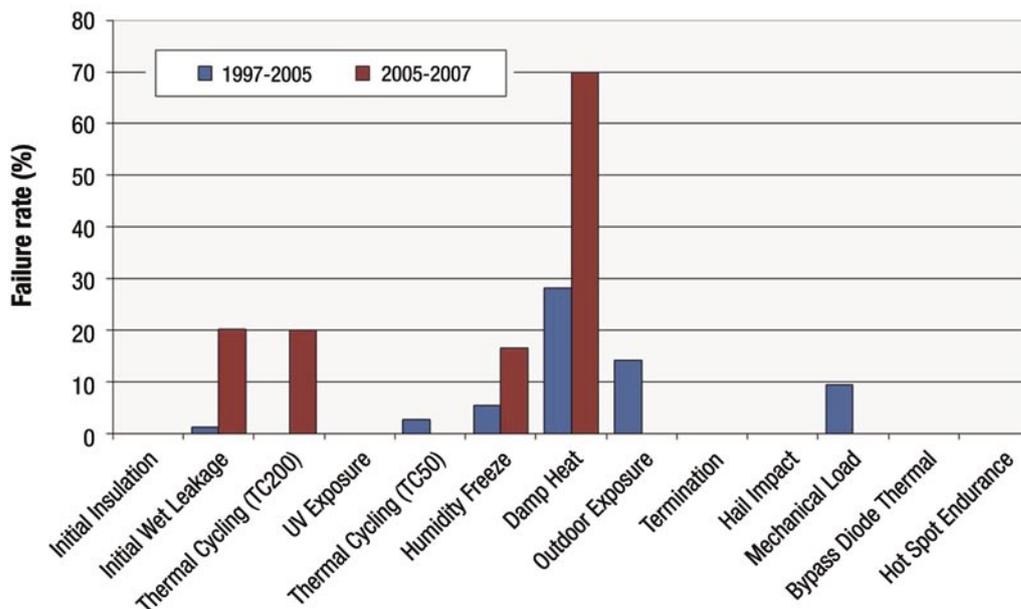


Figure 3. Failure rate comparison of thin-film modules for the 1997-2005 and 2005-2007 periods.

that the Edition 2 thermal cycling test is not more stringent than Edition 1 test for eight out of nine manufacturers' modules investigated in this study.

Bypass diode thermal test

The purpose of the bypass diode thermal test is to assess the adequacy of the thermal design for the hot-

spot susceptibility. This test was not required in Edition 1 whereas it is required in Edition 2. The diode failure is caused by overrating of the diode (diode manufacturer issue), and/or by inappropriate electrical configuration and short circuit current of the module (module manufacturer issue).

The proposed pre-qualification of diodes is expected to reduce the testing time and cost for the module manufacturers.



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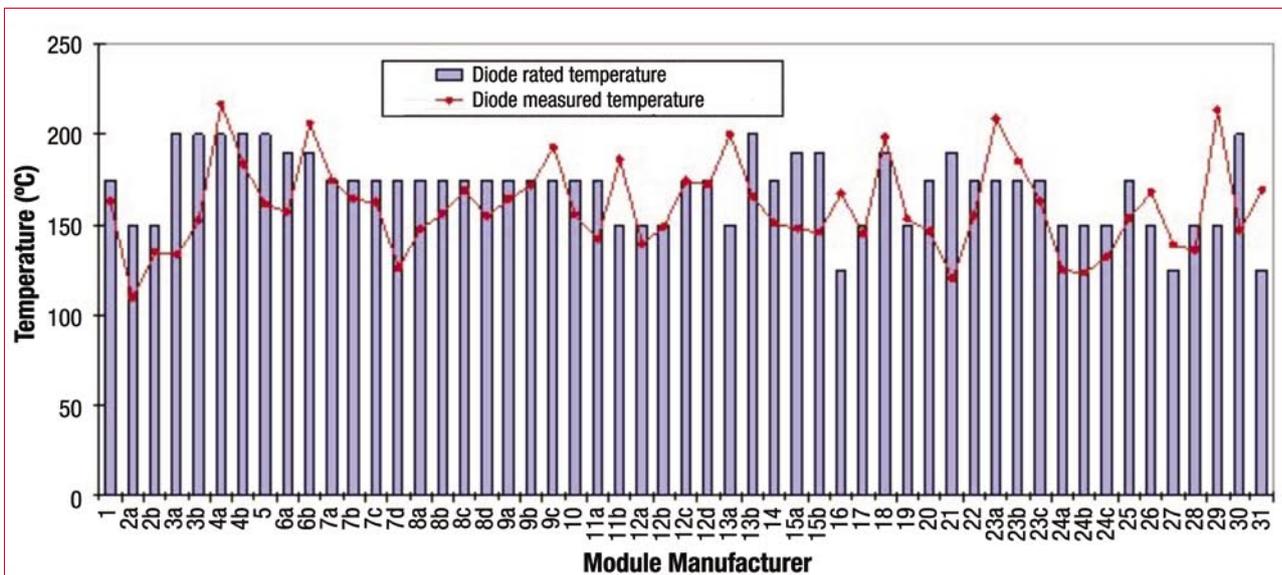


Figure 4. Diode thermal test failure: red dot above the blue column indicates failure.

Manuf. Code	Number of Ed. 1 Modules	Number of Ed. 2 Modules	Post-TC200 Perf. Failure Rate in Ed.1	Post-TC200 Perf. Failure Rate in Ed.2
2	68	8	7%	0%
29	14	4	7%	50%
4	14	4	21%	0%
7	14	12	14%	0%
9	16	6	0%	0%
15	12	4	0%	0%
24	4	4	0%	0%
32	22	2	0%	0%
25	12	8	0%	0%

Table 1. Thermal cycling test failure rate comparison between Editions 1 and 2 of IEC 61215.

Surprisingly, the highest failure rate (31%) for the crystalline silicon modules is related to the bypass diode test (see Figure 2). More than 90% of these bypass diode thermal test failures were related to the higher measured/calculated temperatures of the diodes as compared to the rated temperatures. Less than 10% of the diode failures were related to either the post-visual inspection test (diode touching and melting the junction box casing) or the post-performance test (diode short circuiting). As shown in Figure 4, all the diodes with 125°C rating failed in this test. Out of 31 different manufacturers' modules tested (Figure 4), 19 manufacturers' modules consistently passed the diode test (61%) and the other 12 manufacturers' modules consistently or randomly failed the diode test (39%).

Conclusions

The failure analysis of the qualification test results of ASU-PTL indicates a large increase in the failure rates for the 2005-2007 period as compared to the 1997-2005 period. In both crystalline silicon and thin-film modules, the higher percentage of failure observed in the

2005-2007 period is primarily attributed to the market entry of a large number of new manufacturers, the wet resistance test after damp heat and humidity freeze tests, and the performance test after thermal cycling test. The Edition 2 thermal cycling test of the IEC 61215 standard does not seem to be more stringent than the Edition 1 test. A large fraction of the modules fails due to the bypass diode failures in the chamber and diode thermal tests, suggesting that a pre-qualification of bypass diodes may be warranted.

References

[1] Ossenbrink, H. & Sample, T. 2003, 'Results of 12 Years of Module Qualification to the IEC 61215 Standard and CEC Specification 503', 3rd World Conference on Photovoltaic Energy Conversion, May 2003, Osaka, Japan.

[2] Dunlop, E. & Halton, D. 2006, 'The Performance of Crystalline Silicon Photovoltaic Solar Modules after 22 Years of Continuous Outdoor Exposure', Progress in Photovoltaics: Research and Applications, 14:53-64.

[3] Li, B., Arends, T., Kuitche, J., Shisler, W. Kang, Y. & Tamizhmani, G. 2006, 'IEC and IEEE Design Qualifications: An analysis of test results acquired over nine years', 21st European Photovoltaic Solar Energy Conference, September 2006, Dresden, Germany.

[4] Wohlgemuth, J. H., Cunningham, D. W., Nguyen, A. M. & J. Miller, 'Long Term Reliability of PV Modules', 20th European Photovoltaic Solar Energy Conference, June 2005, Barcelona, Spain.

[5] McMahon, T. J. 2004, 'Accelerated Testing and Failure of Thin-film PV Modules', Progress in Photovoltaics: Research and Applications, 12:235-248.

About the Author

Dr. Govindasamy Tamizhmani (Mani) is the Director of the Photovoltaic Testing Laboratory at ASU. Dr. Mani has over 20 years of research, development, and testing experience related to photovoltaics, fuel cells and batteries. He is currently teaching several graduate-level courses related to alternative energy technologies. Dr. Mani has over 30 publications in peer-reviewed scientific journals and conferences. He is a member of ASTM, ANSI, and the IEC working group for flat-plate photovoltaics, IEC TC82 WG2.

Enquiries

Arizona State University Photovoltaic Testing Laboratory (ASU-PTL)
7349 East Unity Avenue
Mesa, AZ 85212
USA

Tel: +1 480 7271220
Fax: +1 775 3146458
Website: www.poly.asu.edu/ptl