i-PERC technology enables Si solar cell efficiencies beyond 20%

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ABSTRACT

A cost-effective and industrial version of the well-known passivated-emitter and rear cell (PERC) concept has been developed by imec. The imec i-PERC technology comprises a large-area p-type monocrystalline Si solar cell with, on its front, a homogeneous emitter, a thin thermal oxide layer and fine-line Ag screen-printed contacts; on its rear, the cell has a chemically polished surface, low-cost rear dielectric stack layers and local Al contacts. Yielding certified efficiencies of up to 20% and fill factors of 80%, these cells clearly outperform aluminium back-surface field (Al-BSF) cells. During the development stages, process complexity and additional tool investment were kept to a minimum. It is therefore believed that this technology can be picked up by companies in a straightforward way as the next-generation industrial solar cell technology.

Introduction

Today's workhorse of the Si PV industry is the Al-BSF Si solar cell, a cell with screen-printed full Al back-surface field and screen-printed, fired-through Ag contacts on the front. When produced from large-area wafers, these cells demonstrate efficiencies typically in the range of 18.3–18.8%, but the technology offers little room for further improvement. Issues such as wafer bowing, low internal reflectance and limited surface passivation restrict the production of cheap and highly efficient thin Si solar cells. In times of aggressive competition in the PV sector, the adoption of advanced solar cell concepts can however be highly beneficial from an economic perspective. Besides yielding higher efficiencies, such new technology must allow mass production of solar cells in a cost-effective way, with only limited additional investment.

Providing high conversion efficiency and limited Si consumption, the passivated-emitter and rear cell (PERC) concept shows great promise for one such next-generation industrial solar cell. This technology was pioneered by imec in 2005; since then, the first cells have emerged in industrial solar cell production, and record solar module efficiencies have been reported [1]. In order to promote widespread acceptance, imec has further optimized the process steps of this solar cell concept. The result is a highly efficient, cost-effective and industrial version, referred to as the 'i-PERC' solar cell. With this technology, the above-mentioned disadvantages of Al-BSF cells have been addressed, and thinner – hence cheaper – wafers can be used for production. i-PERC cells demonstrate fill factors of up to 80% and certified best efficiencies of up to 20.04%. Using this technology, a company can significantly increase the capacity of its production line in terms of W_p and reduce the cost per W_p. Moreover, the processing and capital expense differences in manufacturing i-PERC cells have been kept to a minimum. This paper presents the key elements of cost-effective i-PERC technology in terms of process step optimization and cell results.

> "i-PERC cells demonstrate fill factors of up to 80% and certified best efficiencies of up to 20.04%."

i-PERC technology

i-PERC technology comprises a large-area p-type monocrystalline Si solar cell with a homogeneous emitter, fine-line Ag screen-printed front contacts and local rear contacts. Local rear contacts are formed by laser ablation of the dielectric layer prior to the Al deposition and the firing step. A generic process sequence for fabricating i-PERC-type cells is shown in Fig. 1 (right). Compared to the Al-BSF sequence, shown in Fig. 1 (left), i-PERC technology involves four new processing steps: (1) rear-surface polishing, (2) low-temperature thermal oxidation, (3) rear plasma-enhanced chemical vapour deposition (PECVD) of SiO_x/SiN_x, and (4) laser ablation of rear dielectrics. Cells produced this way have a higher efficiency potential than Al-BSF solar cells. To exploit that potential, it is equally important to develop a simple and cost-effective process flow.

In the next section it will be shown how the optimization of these key process steps leads to cost-effective solar cells with improved efficiencies. The manufacturing

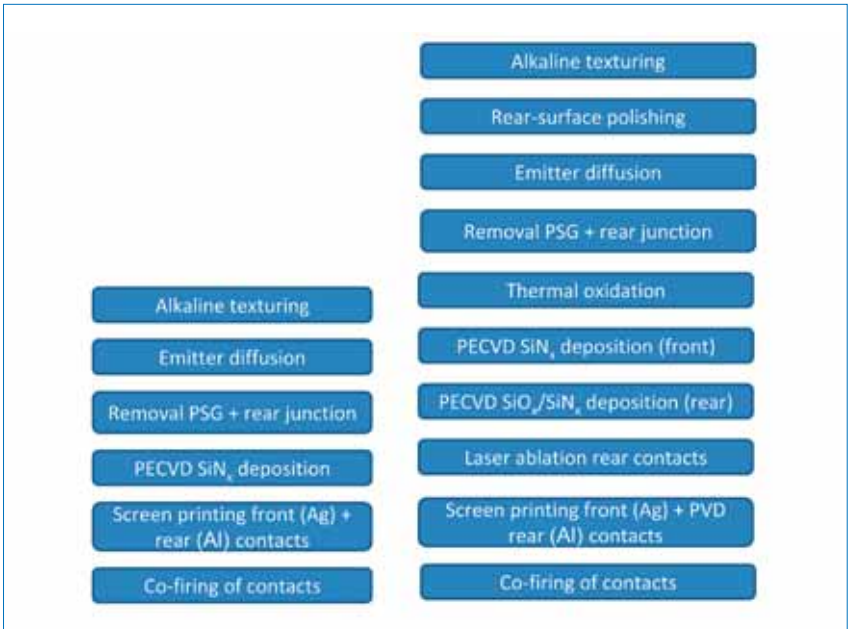

Figure 1. Generic process sequences: Al-BSF (left) and i-PERC (right).

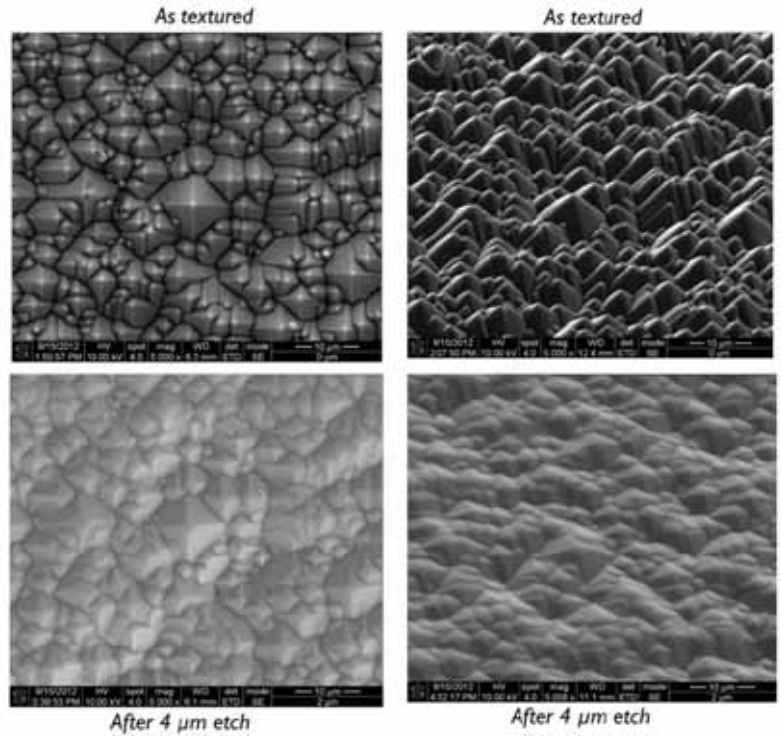

Figure 2. Scanning electron microscope (SEM) images after random pyramid texturing (top) and after a 4µm polishing etch (bottom). The view from above is shown on the left and with a 45° tilt on the right.

processes have been developed within imec's state-of-the-art Si solar cell pre-pilot line using industrially compatible equipment.

Process step optimizations

Rear-surface polishing – key to improved efficiency

Unlike for Al-BSF solar cells, the rear-surface topography plays an important role in the fabrication of PERC-type solar cells: it affects, to a large extent, surface recombination, light trapping and the local rear-contact formation process. As wafers become thinner and thinner, the effects of rear-surface conditioning will become ever more pronounced.

Take surface recombination as an example. When using random pyramid textured surfaces, a high degree of unwanted electrical recombination at the surfaces is observed. An extra polishing step to reduce the surface roughness significantly improves the electrical properties of the surface. But to what extent does this rear polishing step have an effect on light-trapping performance and contact formation? And what is the impact on process complexity and processing cost? To answer these questions, the optimum rear polishing process has been determined that, overall, leads to the best results, keeping in mind that, in an effort to minimize the material costs, the amount of Si consumption during the polishing step should be kept as low as possible.

The rear polishing step is applied to the textured rear surfaces by means of an in-line single-side wet-etch tool. An acidic solution, based on a HF/HNO_3 mixture, is used for the chemical etching. A progressive smoothening of the surface is observed as chemical etching is applied to the textured surface (Fig. 2). As the etch depth is increased, the residual roughness of the surface is reduced. Cells with different degrees of rear roughness were fabricated to study the impact of the polishing step on light trapping, surface recombination and contact formation.

The lowest values for the open-circuit voltage (V_{oc}), fill factor (FF) and short-circuit current density (J_{sc}) were observed in the case of the rear textured surfaces. With increasing Si etch depth, rear-surface recombination velocity decreases and, in general, V_{oc} increases. However, the V_{oc} correlation is not necessarily monotonic. As the roughness of the rear surface is modified, the dynamics of the local contact formation can differ substantially, which can influence the quality of the local Al-BSF, thereby influencing V_{oc}. This is not surprising, as mass exchange between Al and Si takes place all over the rear surface. It was observed for instance that, with Al sputtering metallization, V_{oc} can decrease as the polishing etch depth is increased above a value of 5–6µm. In addition, light-trapping performance was seen to improve as pyramids became smoothened. To maximize light trapping, however, a full planarization of the rear surface was not necessary [2]. This is reflected in the plot of J_{sc} vs. etch depth shown in Fig. 3 (note that the reduction in J_{sc} for etch depths greater than 5µm is only partially attributable to the reduction in total thickness).

> "A moderate smoothening, corresponding to a Si etch depth of around 5–6µm, results in the best cell performance."

Overall, it can be concluded that a moderate smoothening, corresponding to a Si etch depth of around 5–6µm, results in the best cell performance. When combined with other improvements, cell efficiencies above 20% can be achieved. On the other hand, a complete planarization of the rear surface can be detrimental, besides being uneconomical. While surface recombination generally benefits from a

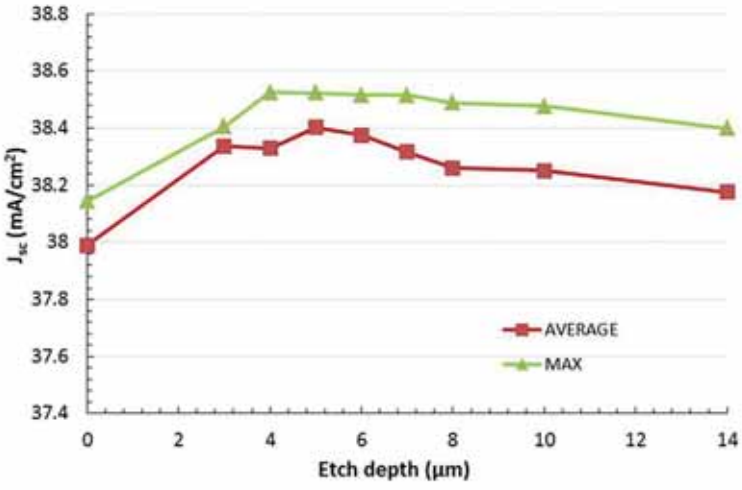

Figure 3. Short-circuit current density (J_{sc}) of i-PERC cells vs. polishing etch depth.

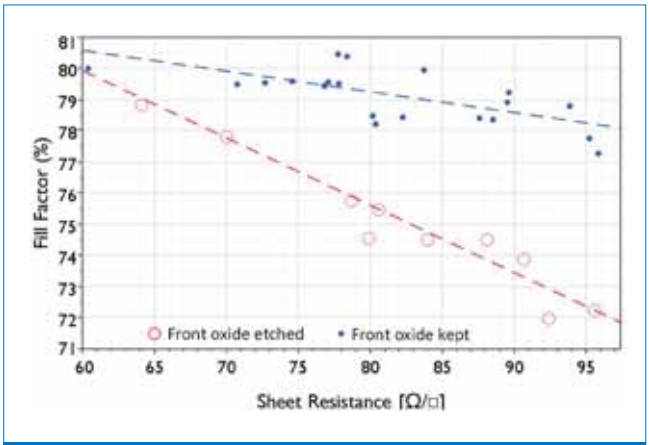

Figure 4. Fill factor vs. sheet resistance for cells with and without thermal oxide.

flat rear surface, light absorption and contact formation are more effective with moderate smoothening.

Thermal oxidation on the front – key to improved fill factor and reduced Ag consumption

An easily implementable way of increasing cell efficiency without incurring too much cost is to introduce thermal oxidation. Thermal oxide is well known to the microelectronics industry as one of the best dielectrics for passivating Si surfaces. A thermal oxidation step has the advantage that surface cleaning and passivation happen to both the front and rear surfaces at the same time. Surprisingly, it was observed that the thermal oxide as a passivation layer on the front and rear surfaces leads to, on the front, a significant *FF* improvement for screen-printed Ag contact formation (Fig. 4). This enhancement was observed for a homogeneous emitter solar cell subjected to a thin thermal oxidation performed at 800°C, before further passivation and subsequent metallization [3].

Further investigations have revealed that this gain in *FF* is mainly due to the contact resistance improvement in conjunction with enhanced passivation. During the low-temperature oxidation step, electrically inactive phosphorus is incorporated from the topmost emitter region into the growing oxide. These high P concentrations in the oxide film help the contact formation for screen-printed Ag contacts. They allow homogeneously diffused, high-resistance emitters (~80–90Ω/sq.) to be contacted with industrially available pastes, with *FF* values exceeding 79%.

Another advantage of the improved contact resistance is the possibility of using less Ag without compromising the cell's efficiency. Such a reduced Ag consumption is highly desirable, as the Ag paste's share of the total cell processing cost has dramatically increased in recent years. Emitters with high sheet resistance require the effective finger width of the Ag to be reduced and the number of fingers to be increased. When this is done properly, modern Ag pastes allow excellent conductivity to be obtained while a significant reduction in overall Ag consumption is realized. The authors believe that a simple processing sequence of this type for emitter and contact formation has cost advantages over approaches that make use of, for example, selective emitters. The latter involve a higher number of processing steps and require a higher degree of accuracy during the metallization step.

Rear-surface passivation – key to enhanced efficiency

The evolution towards thinner, and hence more sustainable, Si solar cells comes with an inherent decrease in efficiency. This decrease is due to the recombination of minority charge carriers at the surfaces and interfaces, an effect that begins to play a bigger role in thinner cells. Yet, as the wafer thickness decreases, it is possible to maintain cell efficiency with better surface passivation than with full Al-BSF. Rear passivation by dielectric layers is therefore essential in the i-PERC process flow. Besides passivation, the dielectric layers have additional functions: they have to serve as a rear reflector

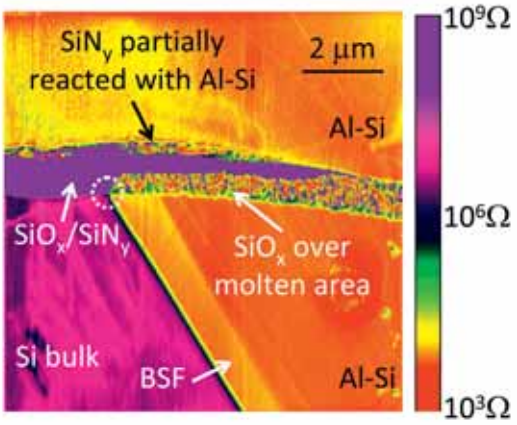

Figure 5. SSRM analysis of a local contact point, showing local BSF, Al-Si eutectic, dielectrics and possible reactions of the dielectrics with Al during the firing process.

Figure 6. A solar cell made using imec's i-PERC technology.

Description	J_{sc} [mA/cm^2]	V_{oc} [mV]	*FF* [%]	*Eff* [%]
125mm Cz-Si, SCP Ag	38.6	662.8	78.3	20.0
156mm Cz-Si, SCP Ag	38.2	650.1	79.7	19.8

Table 1. Solar cell performance for two large-area i-PERC cells, as confirmed by ISE CalLab.

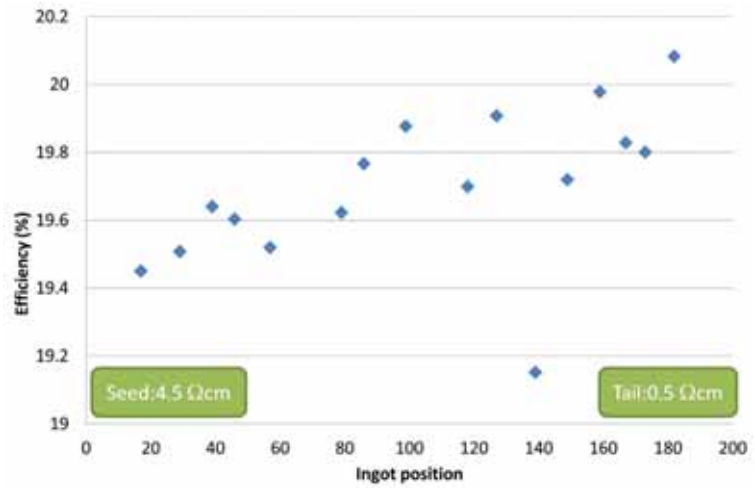

Figure 7. Efficiency distribution across a Ga-doped ingot for the i-PERC screen-printing process applied to Si wafers.

and prevent unwanted contact spiking at areas where the layers have not been laser-opened for rear-contact formation. Optimizing the dielectric stack design for these purposes should additionally take into account the need for low cost of ownership in order to be industrially applicable.

One of the routes followed by imec is to apply the thermal oxide layer for rear-surface passivation purposes as well. This thermal oxide layer does not have to be thicker than a few nanometres to be beneficial and serve several purposes. The overall rear passivation stack should, in the authors' view, also comprise a low-cost Si oxide layer of thickness greater than 100nm that serves, for optical purposes, as the rear reflector, and reduces the negative impact from the unwanted interaction with Al during rear-contact formation. Finally, the rear dielectric stack is covered with a SiN_x layer. During contact firing, this layer prevents the Al rear from spiking through the dielectric stack and from consuming SiO_x in unwanted regions [4]. PECVD is used to deposit both the SiO_x layer and the SiN_x layer.

Rear-surface metallization – trade off between improved fill factor and open-circuit voltage.

In i-PERC technology, the local rear Al contacts are formed by opening the dielectric layers with laser ablation, followed by a deposition of the Al layer over the whole rear surface and subsequent annealing. Typically, the laser openings follow a dot pattern with a specified pitch. Initially, screen printing was used to deposit the Al layer on the rear surface. On the whole, this metallization process flow is fairly simple. To further enhance cell performance, imec is examining different ways of depositing Al. Screen printing of Al-based pastes, and methods based on physical vapour deposition (PVD), such as sputtering, e-beam evaporation and thermal evaporation, are all being examined. It is possible to obtain outstanding solar cell performance with these two technologies: so far, they have both led to excellent *FF* values (even exceeding 80%), while PVD depositions allow the best V_{oc} values (of up to 664mV) to be realized. The use of PVD to deposit Al can result in large cost savings in respect of materials, but will lead to a higher investment cost in terms of equipment.

The optimized rear-contact pattern strongly depends on (i) the base resistivity of the wafer, (ii) the laser-ablated dot size, (iii) the nature of the metal layer, and (iv) the annealing temperature to form the contacts. At imec the rear-contact formation has been analyzed by using in situ microscopy. Although the analysis is still ongoing, these measurements, in combination with a cross-sectional scanning spreading resistance microscopy

(SSRM) analysis, have already revealed a lot of information about the phenomena occurring during rear-contact formation (Fig. 5). The measurements will help to further improve the process flow for rear-surface metallization [4].

Impact of process optimization on cell efficiency, process complexity and cost

By using the optimized process steps discussed earlier, it has been possible to fabricate solar cells that considerably outperform Al-BSF solar cells. The best cell made from 125mm Cz-Si shows a solar efficiency of 20.0%; the best cell made from large-area 156mm Cz-Si has an efficiency of 19.8% (Fig. 6 and Table 1). Both results have been confirmed by ISE CalLab. More recently fabricated cells from 125mm Si well exceed the 20% efficiency mark. Fill factors of 80% have been achieved for screen-printed solar cells with low-cost rear dielectric stack layers.

The improved i-PERC screen-printing process has been applied to many different wafers. In Fig. 7 the efficiency distribution is shown for Si wafers taken across a Ga-doped ingot from seed side to tail side. The efficiency on the seed side is lower, mainly because of a higher base resistivity, which affects the internal resistance and hence the fill factor. This difference in base resistivity is a consequence of the low segregation coefficient of Ga in Si. Ideally, for these types of wafer, the contact pitch needs to be adapted to changes in resistivity, which was not done for this particular experiment. An advantage of these cells is that they do not suffer at all from light-induced degradation (LID).

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Depending on the case, the increase in cell efficiency may be up to 1.5% absolute compared with conventional Al-BSF cells. Of course, this higher efficiency level comes at the cost of an increased process complexity. Although the processing and capital expense differences have been kept to a minimum, four extra tools have to be anticipated for the additional process steps: an in-line polishing wet bench, thermal oxidation equipment, a PECVD system for rear dielectric deposition (which can potentially be combined with front antireflection coating (ARC) deposition) and a laser platform for ablation. However, because of the significant increase in efficiency, the capacity of a company's production line in terms of W_p will largely increase and the cost per W_p will fall. A payback of the additional investments has been calculated to happen in an acceptable timeframe. It is therefore envisaged that the new i-PERC technology could be picked up by industrial companies in a straightforward way with only a limited investment. And, besides the increase in efficiency, it should not be forgotten that the i-PERC process allows the use of thinner and hence cheaper wafers, while maintaining the high efficiency level and production yield.

Conclusion

Key improvements to imec's PERC technology have been presented which allow the manufacture of large-area solar cells with efficiencies of up to 20%. This is a significant leap in efficiency compared to traditional Al-BSF solar cells. The improved cell performance is a result of a polishing of the textured rear surface, a thermal oxidation of the front and rear surfaces, a rear passivation with a dielectric stack and an improved rear metallization process. Additional investment needed to manufacture these optimized cells has been kept to a minimum. The real advantage for industrial companies is a significant decrease in the cost per W_p, allowing the payback of additional investment within a reasonable time frame.

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The results were achieved within imec's Si solar cell industrial affiliation programme (IIAP), a multi-partner R&D programme that explores and develops advanced process technologies aimed at sharply reducing Si use while increasing cell efficiency, and hence substantially lowering the cost per W_p even further. Industrial partners who wish to integrate innovative processes into their solar cell production are welcome to join imec's R&D programme.

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