Griddler: The handy 2D solar cell calculator

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ABSTRACT

Actual solar cells are large-area, two-dimensional (2D) devices with lateral variations in internal voltage, but most of the time they are represented by simplistic equivalent circuits consisting of a few lumped elements. Griddler© is a finite-element-method (FEM) simulator that constructs and solves the full 2D distributed network representation of a metallized solar cell. Not only is this approach far more versatile and adaptable to real-world problems, accurate in predicting subtle device characteristics, and compatible with mapping data, but it can also be implemented in a way that is as easy and quick to use as a handy calculator. This paper covers a broad range of applications related to full-area 2D modelling and introduces Griddler 1.0 – a compact freeware computer program that places much of that power at the fingertips of any solar cell engineer with a PC.

Introduction

Photovoltaic engineers are no doubt familiar with the H-pattern metallization on the front side of silicon wafer solar cells. The simplicity and elegance of the H pattern lends itself to analytical determination of the power losses due to shading and series resistance, enabling one to derive equivalent circuit parameters to predict the cell performance with reasonable accuracy. But in the manufacturing environment, where every 0.1% absolute efficiency gain is worth fighting for, the simple equivalent circuit model has some severe limitations in terms of resolution. For example, the model is unable to provide the answer to the question of how much ohmic power loss originates from the rear side of the aluminium back-surface field (Al-BSF) cell, which features blanket metal rather than an H pattern. Moreover, it cannot assess the impact of metal finger breaks or striations, or of local shunts and highly recombinative regions across the wafer, created by process or wafer non-uniformity. The equivalent circuit approach becomes rather unwieldy at evaluating segmented busbars, and is not amenable to the design of metallization patterns with even a slight deviation from an H pattern, let alone more complex patterns such as those in metal-wrap-through (MWT) solar cells.

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It is obviously advantageous to tackle the innately two-dimensional problem of the solar cell with a wide net that is adaptable to all metallization patterns and spatial distributions of diode characteristics. To this end, SERIS has developed Griddler©, a two-dimensional (2D) finite-element-method (FEM) mesh generator and solver optimized for steady-state solar cell problems [1]. The following discussion will cover some examples of real-world problems that a 2D solver such as Griddler is designed to handle. While some of the more sophisticated features are still being optimized in-house, the core mesh-builder and solver for the 2D voltage distribution in solar cells is now freely available as Griddler 1.0, which will be introduced later in this paper.

Example 1: H-pattern solar cell

Griddler is equally effective as a solution for solar cells of all kinds of metallization geometry, including simple ones like the H pattern. Since Griddler simulates an I–V curve reasonably quickly for an FEM solver (typically within 40s on a laptop PC), it can still be the calculation tool of choice for analysing the H-pattern solar cell. There are two advantages in choosing Griddler over the equivalent circuit model in this case: 1) the simulated I–V curves take on a more accurate shape; and 2) Griddler enables an impact analysis on cell performance to be carried out for a wide range of scenarios. Fig. 1 shows a multicrystalline silicon wafer solar cell and its Griddler-simulated voltage distribution near the 1-sun maximum power point (MPP), in the case of current extraction from the bottom ends of ribbons soldered to the three busbars.

Fig. 2 compares the current density–voltage (J–V) as well as aggregate series resistance–voltage (R_s–V) curves derived using the double-light

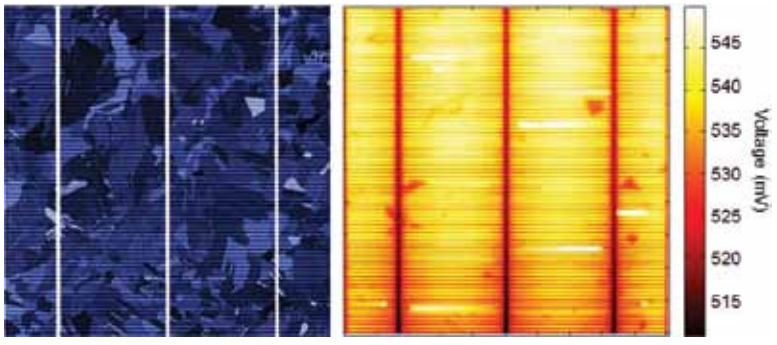

Figure 1. An example of a multicrystalline silicon wafer solar cell and its simulated voltage distribution near the maximum power point (MPP), showing underlying features such as grain quality, metal shading and recombination, edge recombination, and finger breaks. Current is extracted by soldered ribbons at the busbar ends.

method [2], generated by an equivalent circuit model and by Griddler. For the J–V curves, it is only upon close examination that differences can be found in the MPP and V_{oc} points predicted by the two models (discussed in more detail below), and the curves appear more or less similar in shape.

In contrast, the R_s–V characteristics generated from the J–V curves for Griddler and the equivalent circuit model diverge sharply. Griddler is able to capture the nuances one finds in a distributed network of diodes and resistors that are far more representative of a solar cell; as a result, the derived R_s–V is highly voltage dependent, as would be observed in reality. By comparison, the equivalent circuit model generates an R_s–V curve that is flat, thus revealing its over-simplified treatment of the device characteristics. This highlights a fundamental limitation of the equivalent circuit model: while it may suffice for predicting the MPP of an H-pattern solar cell with reasonable accuracy, it does not model the voltage or light intensity dependence well enough to predict R_s–V, Suns–V_{oc}, ideality factor and other in-depth characteristics that shed light on the inner workings of the solar cell.

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A 2D simulator, such as Griddler, is a far more accurate tool for finding the causal link between the solar cell structure and device output characteristics. The resolution at which structural details are fed into a simulator to predict output, and at which measurement data is exhaustively examined to pinpoint power loss mechanisms in the solar cell, must be raised by taking into account the 2D nature of the solar cell device plane. This cannot be more true today, when all sorts of mapping data – such as photoluminescence (PL)/electroluminescence (EL) imaging, light-beam-induced current (LBIC), sheet resistance, and microwave photoconductance decay (μ-PCD) – have become commonplace or even routine.

Next, to illustrate how Griddler facilitates a quick analysis of cell performance for a wide range of real-world scenarios, Table 1 chronicles the evolution of the open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (FF), and efficiency (η), as different recombinative elements and other imperfections are progressively incorporated in the 2D model. The current density J_{sc} is held constant in the simulation in order to focus on V_{oc}, FF and η.

In scenario 1, the J_{01} and J_{02} values across the wafer are taken to be averages and spatially uniform, whereas in scenario 2 they take on local values as would be found in mapping data. The difference is not trivial: in scenario 2, where the low-quality regions are highly concentrated and localized, both the V_{oc} and η improve, because the low-quality regions are now connected to the rest of the solar cell via a metallization network of finite conductance that reduces the diode current sunk into these regions.

Next, in scenario 3, edge recombination at the wafer edges is added to the solar cell model, in the form of a second diode (ideality factor n = 2). Obviously, this leads to significant reductions in FF and η, but again the impact of the edge recombination is to some extent dampened by the spatially localized nature of this diode current sink, compared with the case if it were evenly distributed across the wafer. This scenario is also simulated using the equivalent circuit model, which simply uses as inputs the average values of J_{01} and J_{02} across the wafer; R_s is subsequently derived using standard formulae applicable to the H pattern. The equivalent circuit model is observed to fare reasonably well compared with Griddler, but neglects

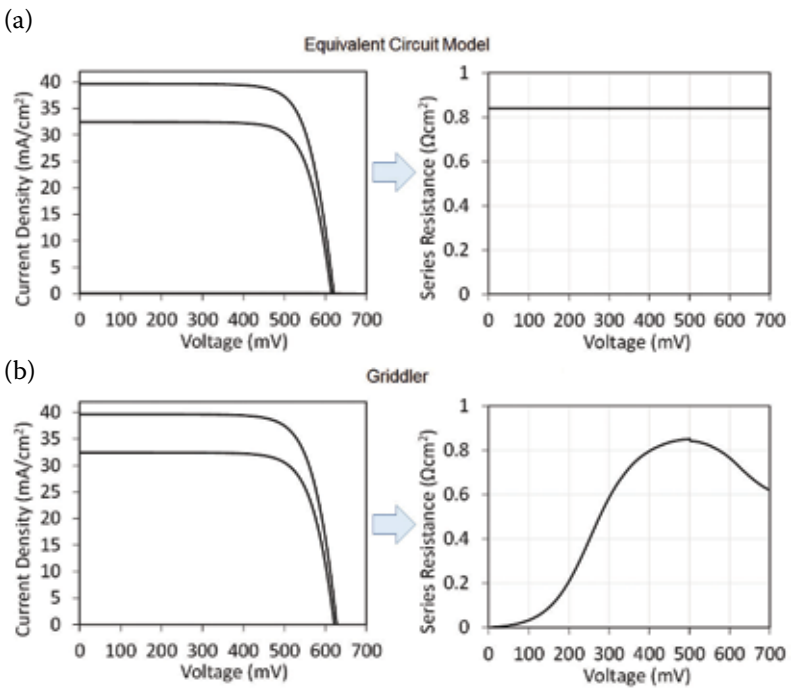

Figure 2. Current density–voltage (J–V) curves and series resistance–voltage (R_s–V) curves simulated by (a) the equivalent circuit model, and (b) Griddler.

	V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]
Griddler scenario 1	617.5	36.04	76.50	17.03
Griddler scenario 2	625.4	36.04	76.09	17.15
Griddler scenario 3	624.8	36.04	75.82	17.07
Equivalent circuit model for scenario 3	617.6	36.04	76.05	16.93
Griddler scenario 4	624.7	36.04	75.65	17.03

Table 1. Griddler-simulated J–V parameters of the multicrystalline silicon solar cell for the different scenarios discussed. The parameters predicted by the equivalent circuit model for scenario 3 are also shown for comparison.

a few subtle effects, namely 1) the localized nature of the low-quality regions and edge recombination, and 2) the localized metal recombination and metal shading. As already discussed, the first effect impacts V_{oc} and η less than the case of uniform recombination across the wafer; in contrast, the second effect impacts these parameters more than would a uniform distribution, because the local dips in voltage under the metal regions influence the terminal voltage. Overall, for this particular simulation, the equivalent circuit model underestimates V_{oc} and η, and overestimates *FF*, both by significant degrees.

Not only is Griddler more accurate in finding the MPP, V_{oc} and the overall shape of the *J–V* curve, but it can also simulate situations that are completely beyond the reach of the equivalent circuit model. For example, scenario 4 simulates the same solar cell with striations in the metal finger height throughout the wafer plane, which introduces a number of finger breaks, as can be seen in the voltage map of Fig. 2. These metallization imperfections are fairly commonplace in practice, and Table 1 shows that they have a subtle impact on device performance. With 2D simulation, it becomes quick and easy to explore a myriad of situations that occur in solar cells – including partial shading, local shunts and wafer breaks – thus opening up a world of possibilities in the assessment of device performance to aid cell design and optimization.

Example 2: Solar cell rear metallization

While the solar cell H pattern is relatively carefully optimized and analysed in research and industry, the rear-side metallization is often more of an afterthought. This is partly because there is no routine way of calculating the influence of series resistance in the rear Al metal plane of a standard Al-BSF solar cell, since the current flow pattern is highly two-dimensional rather than strictly parallel to the wafer sides as in the case of the H pattern. The problem is further compounded by a fair degree of arbitrariness in the rear-contacting scheme during cell measurement: many lab *I–V* testers place the rear of the solar cell in intimate contact with a large-area metal chuck, thus rendering the cell-rear ohmic loss practically zero.

The lack of measurement and calculation standards obscures the understanding of the contribution of rear metallization to cell series-resistance losses. Indeed, the H-pattern solar cell in the previous section is itself a story half told: the Griddler simulations thus far have assumed an infinitely conductive rear metal, corresponding to the case of measurement in the lab. In order to gain a comprehensive picture of how the cell performs after interconnection in the module, Griddler is used to assess the impact of cell rear ohmic losses on performance.

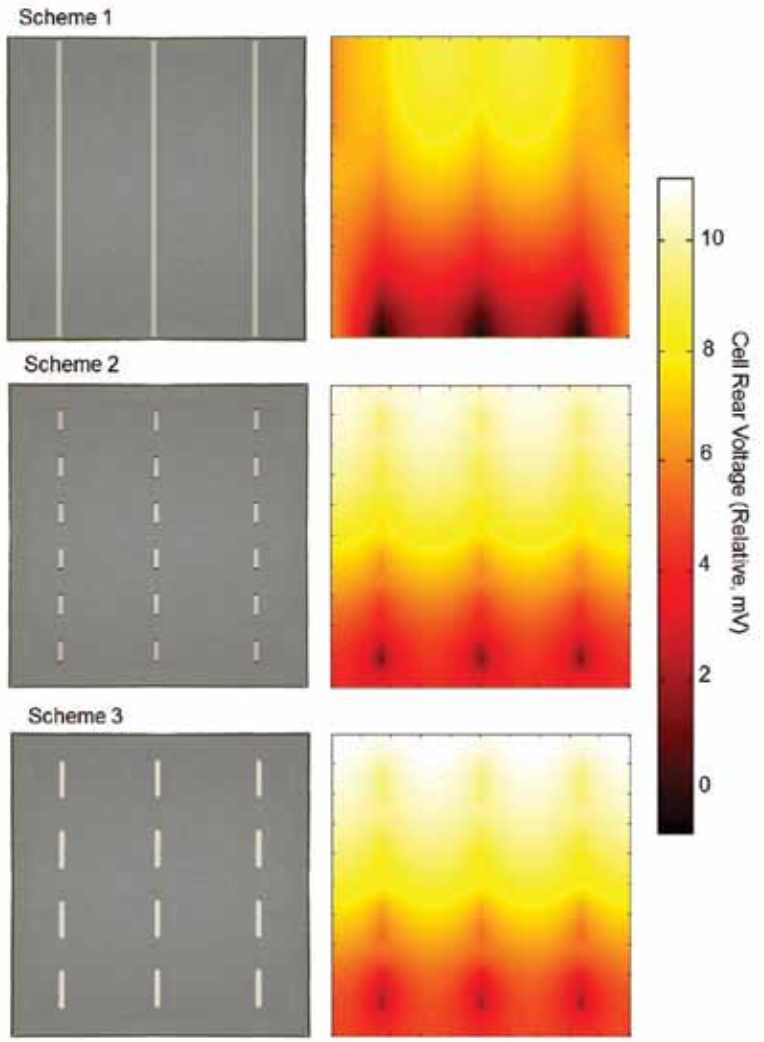

Figure 3. Simulated rear-cell voltage distribution (relative), for three different rear solder pad layout schemes.

Fig. 3 shows a few Al-BSF solar cell rear schemes with different solder pad layouts and the corresponding relative voltage distributions across the cell rear near the MPP. For quickness, a non-rigorous approach is adopted for predicting the overall interconnected solar cell *J–V* parameters. First, Griddler simulations are redone for the front H pattern, still assuming an infinitely conductive rear, but taking into account the higher recombination regions introduced by the rear solder pads. Next, Griddler simulations are carried out for the rear-metallization schemes, assuming an infinitely conductive front, to determine the *FF* drop relative to the case of negligible series resistance. Finally, the relative *FF* drop in each case is subtracted from the *FF* of the front H-pattern simulation. Admittedly, this method is not as ideal as a full bifacial simulation, which is still in the developmental stages, but nevertheless it yields sufficiently accurate insight into the impact of the rear metallization.

Table 2 shows the estimated *J–V* parameters of the solar cell after interconnection with front and rear ribbons. The message is clear that the rear metallization makes a significant difference to the performance of the final device. Relative to the case of the simulation of the front H pattern only while assuming an infinitely conductive rear (which produced the parameters of scenario 4 in Table 1), the additional series resistance on the cell rear induced a further 0.6–1.0% (absolute) drop in *FF* and up to 0.2% (absolute) drop in efficiency. Evidently, V_{oc} is also slightly reduced when the high-recombination regions introduced by the rear solder pads

	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	η [%]
Rear scheme 1	623.9	36.04	75.03	16.87
Rear scheme 2	624.4	36.04	74.76	16.82
Rear scheme 3	624.3	36.04	74.72	16.81

Table 2. Estimates of the final solar cell *J–V* parameters, with ribbons connected to both the front and rear sides of the cell, and current extracted from the ends of the cell. The rear solder pad schemes correspond to the ones illustrated in Fig. 3.

are accounted for, but in this case the impact is negligible. This may not be the case, however, for solar cells with higher V_{oc}s, which are more sensitive to additional recombination sources.

Example 3: The fine-line screen-printed grid

Screen printing is the industry standard for solar cell metallization. As manufacturers push for finer and finer silver fingers using this technology, it also becomes increasingly challenging to print uniformly conductive silver fingers. At a certain point, the non-uniformity of fingers – in the form of striations, bottlenecks and finger breaks – begins to erode cell performance in a measurable way. Fig. 4 shows 3D microscopy data of different silver fingers, printed using three different screens that produce fingers with respective nominal widths of 80, 70 and 60µm. The same figure also shows 2D simulations of the ohmic losses in these fingers. Clearly, the narrower the nominal width, the greater the rates of striations and bottlenecks.

With the use of the microscopy data, combined with line resistance and busbar-to-busbar (B2B) resistance measurements, it is possible to build up adequate statistics about the distribution of finger segment conductance. This statistical model can then be fed into Griddler to simulate a realistic fine-line-printed solar cell with an uneven distribution of silver. As an example, four sets of statistics – starting with zero variations in line conductance in case A, then with increasing variations as one progresses from cases B to D – are input into Griddler for the simulation of a monocrystalline silicon wafer solar cell. In all cases the fingers have a width of 70µm and a nominal metal sheet resistance of approximately 3.3mΩ/sq. Fig. 5 maps the cell voltages near MPP, and Table 3 shows the corresponding *J–V* parameters. It is apparent that, even between cases A and B (which is in a way comparing perfect metallization to a level of imperfection that resembles what is found in industrial cells), there can be significant differences in *FF* and efficiency. Obviously, at the

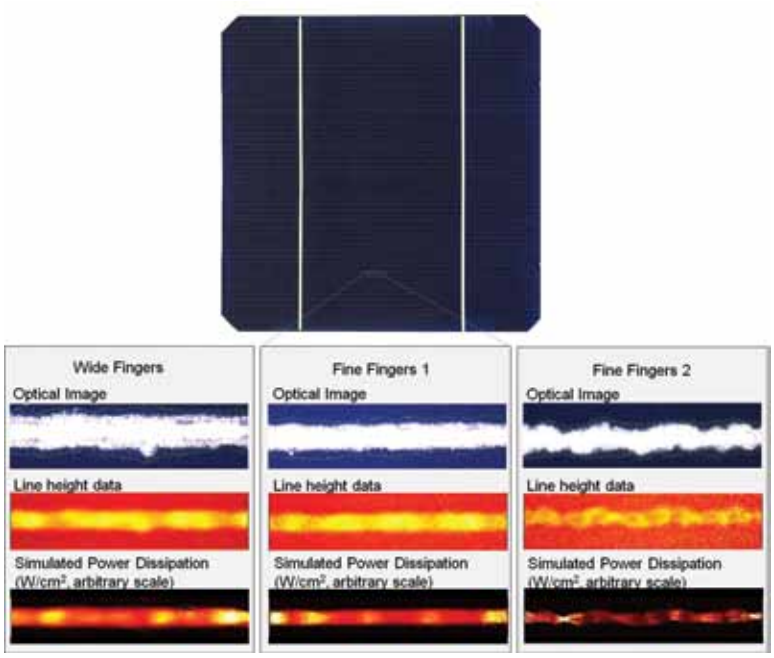

Figure 4. 3D microscope data of different screen-printed metal fingers, and for each case the simulated power dissipation during current flow.

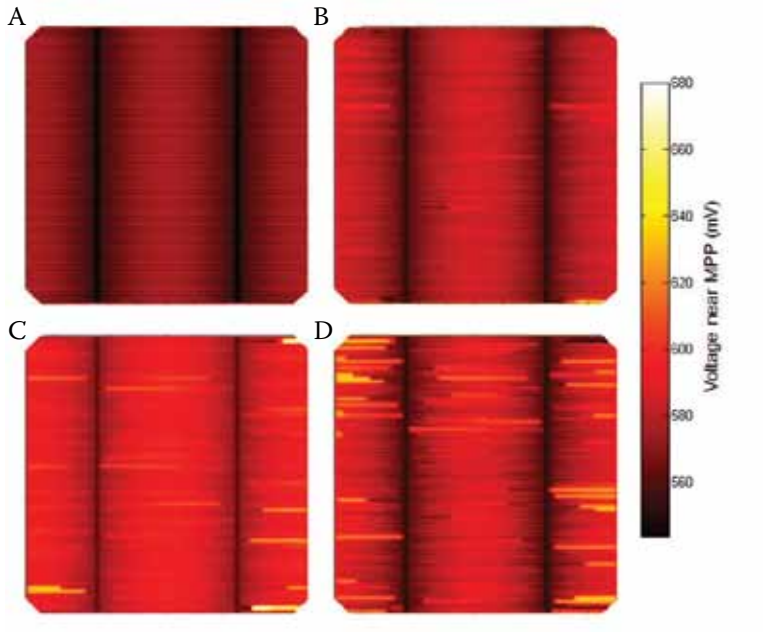

Figure 5. Simulation of the voltage distribution near MPP for a monocrystalline silicon wafer solar cell, with increasing severity of conductance variations in the metal finger segments. Case A represents the perfect cell with no variations in the metal conductance.

	V_{oc} [mV]	J_{sc} [mA/cm^2]	*FF* [%]	η [%]
Case A	640.7	37.92	80.40	19.53
Case B	640.5	37.92	79.89	19.40
Case C	640.3	37.92	79.53	19.31
Case D	640.2	37.92	78.27	19.00

Table 3. Simulated *J–V* parameters for the four cases of metal finger striations severity, corresponding to Fig. 5.

rates of defects found in cases C and D, the erosion of efficiency reaches an unacceptable level. In practice, to alleviate the impact of uneven metal line conductance, industry takes several measures, such as the joining of finger ends near the wafer edges to produce redundant current paths, and adopting three-busbar and even four-busbar designs. More advanced interconnection schemes, such as the use of numerous parallel wires in place of ribbons, are yet more tolerant of finger striations and breaks. All of these scenarios are quite straightforward to simulate using Griddler.

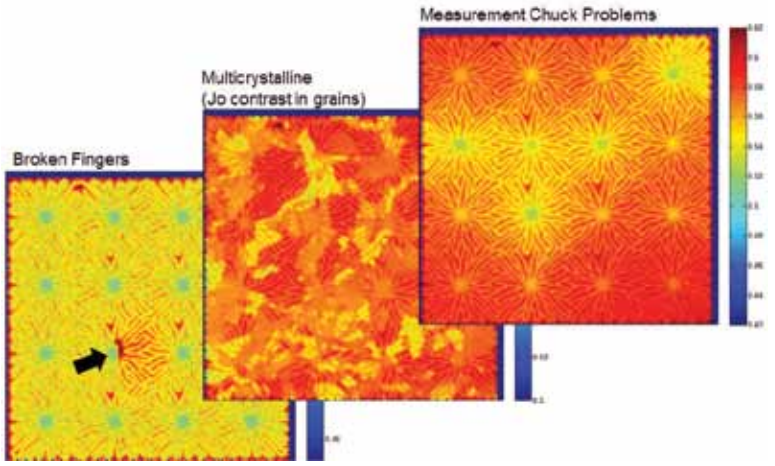

Figure 6. Simulated voltage distributions of a solar cell with the SunWeb metal-wrap-through (MWT) metallization pattern, for different scenarios.

Example 4: Alternative metallization schemes

As its name suggests, Griddler is designed to calculate metallization grids of all kinds. Being a FEM mesh builder and solver, it is undaunted by complex metallization patterns, making it the ideal tool for the study of cell types or metal structures that inherently feature irregular grids. As an illustration, Fig. 6 shows Griddler-simulated voltage distributions on the elegant Solland SunWeb metal-wrap-through (MWT) solar cell [3,4], for three scenarios: 1) the cases of broken fingers; 2) a multicrystalline wafer with different recombination regions under the metal pattern; and 3) the interesting situation where the voltages at the current extraction points are unequal. The last case is actually quite commonly encountered during the measurements of MWT and other rear-contact solar cells, because the test jigs for these cells must rely on suction force to hold the cell down against the probe pins, and the relatively weak pin spring-force can lead to significant and uneven contact resistance. The resultant uneven voltages at the current extraction points may lead to non-repeatable measured fill factors that tend to be underestimations. By simulating this effect, Griddler can be a useful tool for error analysis in the test lab.

Griddler is equally adept at calculating the conductance of complex metal networks, such as the one shown in Fig. 7. This is a nanoparticle

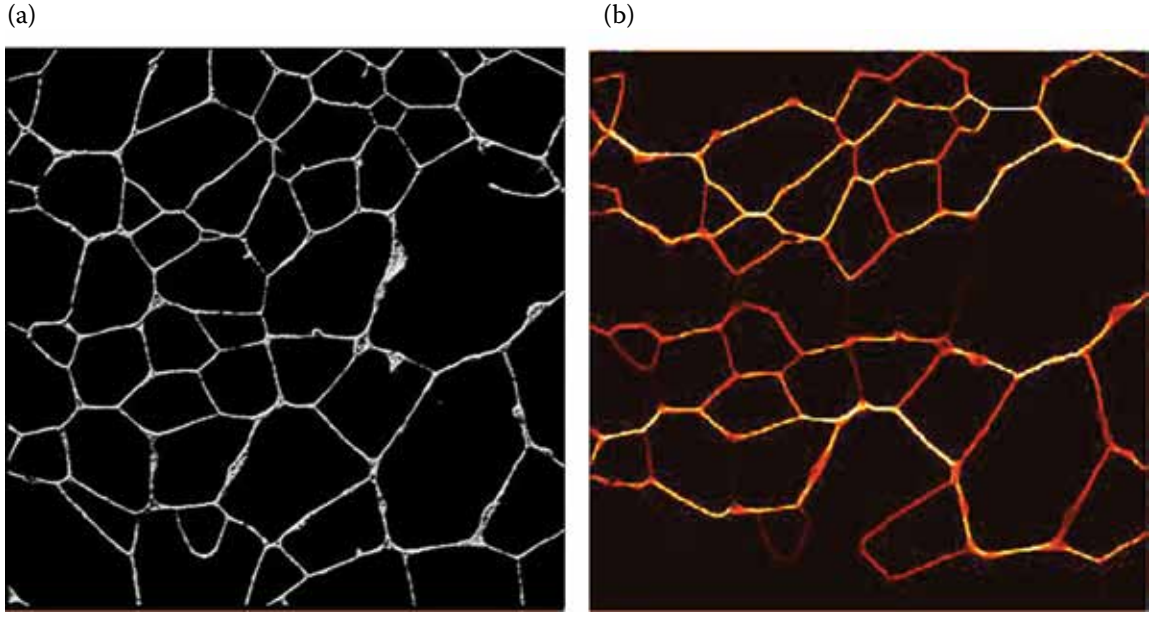

Figure 7. Metallization that consists of a random mesh-like network: (a) SEM image; (b) simulated current density, when a voltage difference is set up between the left and right edges of the image.

conductive coating that self-assembles into a random mesh-like network when coated onto a substrate, and is currently in the research phase for solar cell applications. Fig. 7(a) shows a scanning electron microscope (SEM) image of the network, and Fig. 7(b) shows the simulated current density through the network when a voltage difference is set up between points on the left and right edges of the picture. The simulation of the network conductance versus the network mesh properties enables better solar cell metallization schemes to be designed that can incorporate the nanoparticle conductive coating in place of the traditional transparent conductive oxides (TCOs).

Griddler 1.0: Two-dimensional power for everyone

The software for implementing the concept of a sophisticated simulation does not necessarily have to be difficult to use. The visualization of the solar cell as a 2D plane is a very intuitive idea for anyone to grasp, and the high degree of automation provided by FEM meshing should make it simpler and more flexible for the user to define the geometry of the solar cell problem compared with, say, keying in parameters in a spreadsheet to perform an equivalent circuit model simulation.

> "Griddler 1.0 is designed to be used by an untrained user having just a basic understanding of solar cells."

In this spirit, Griddler 1.0 was designed as compact freeware that runs on 32- or 64-bit Microsoft Windows machines. Although it does not include some of the more sophisticated features such as the incorporation of mapping data, it incorporates the essential features of mesh building and determination of the 2D voltage distribution across a solar cell with arbitrary metallization patterns. Griddler 1.0 is designed to be used, without any instructions, by an untrained user having just a basic understanding of solar cells, and is built to be very tolerant of faults. The program includes the following key features:

1. Arbitrary grid geometries can be imported from common file types, such as images and CAD files.

2. The user can alternatively design an H-pattern front grid on wafers of any size and format.

3. To study the robustness of the metallization design, finger breaks can be created by clicking on the metal pattern.

4. Visualization of the voltage distribution on the solar cell is possible.

5. The *J–V* curve can be quickly simulated by inputting some common metallization-related parameters, such as metal sheet resistance, metal contact resistance and semiconductor sheet resistance.

6. The ohmic losses of the solar cell at the MPP are broken down into separate components.

Fig. 8(a) shows the Griddler 1.0 interface after loading a particular solar cell design that features wire-connection (an example file that comes with the installation). Fig. 8(b) shows the voltage map near the MPP as current is extracted from the ends of the wires at the bottom edge of the cell. Fig. 8(c) shows the simulated *J–V* curve and the breakdown of ohmic losses as percentages of the cell pseudo-maximum power. Running on a 32-bit 2.67GHz laptop, Griddler takes 10s to generate the mesh

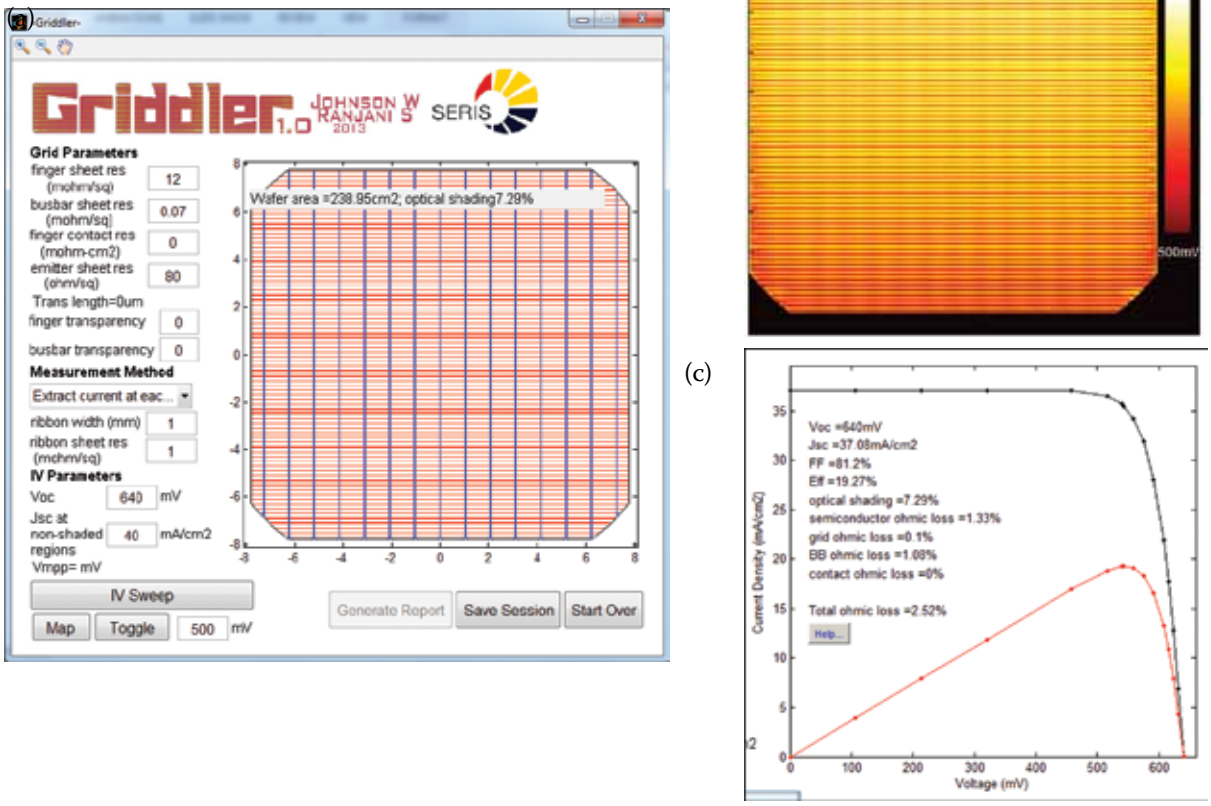

Figure 8. Griddler 1.0 interface: (a) after loading a solar cell example; (b) simulation of the voltage distribution near MPP; (c) simulation of the *J–V* curve and ohmic losses.

for this solar cell design, and completes the *J–V* curve in 30s.

Be it for a simple H pattern or the most complex of metallization problems, it is hoped that Griddler 1.0 (available as a free download [5]) will become the handy calculator that universally comes to mind.

Acknowledgements

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About the Authors

Johnson Wong is the head of PV characterization at SERIS. After receiving his Ph.D. in photovoltaic engineering at UNSW in the area of thin-film silicon on glass solar cells, he joined SERIS as a scientist, engaging in various research topics such as screen-printed and evaporated-metal all-back-contact solar cells, and a-Si:H/uc-Si:H c-Si heterojunction solar cells. His current work includes the development of photoluminescence and electroluminescence detection and analysis methods, the application of solar cell reciprocity relations, and the study of the impacts of solar cell lateral non-uniformity and distributed resistances on device performance. Johnson also heads the effort to set up an ISO17025 test and calibration lab at SERIS.

Ranjani Sridharan began her career in the field of metallization at imec Leuven, where she focused on screen printing and characterization of solar cells. She has been working at SERIS since 2011 as a research engineer, and has extensive experience in lithography, screen printing and other advanced metallization techniques related to the fabrication of silicon-wafer-based solar cells. As well as her involvement in the Griddler project, she currently works on the development of hybrid solar cells, which combine deposited heterojunctions and silicon-doped layers.

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