Diamond wire sawing for PV – Short- and long-term challenges

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ABSTRACT
A shift from free-abrasive/steel wire sawing to fixed-abrasive diamond wire sawing is expected to take place in the PV cell manufacturing industry, with 2018 being the anticipated pivotal point for market dominance. This shift is due to several key advantages of diamond wire sawing, such as higher throughput, less wire per wafer, no slurry and the possibility of kerf recycling. However, in order for diamond wire sawing to realize its promise as the next-generation workhorse for the slicing of silicon PV wafers, inherent fundamental challenges must be properly identified and successfully addressed by the PV industry. As a first step to increasing the current collective understanding of the critical needs/challenges of diamond wire sawing, the c-Si programme of the U.S. PVMC held a workshop on July 8th, 2014 in San Francisco, California. One of the key products of this workshop was an extensive list of short- and long-term challenges. This article expands on some of the most important challenges identified at the workshop through the collective discussions and dialogue among a variety of PV industry experts and stakeholders.

Introduction

Unlike loose abrasive sawing, where abrasives are dispensed within the slurry and pushed against an ingot using a moving steel wire, fixed-abrasive sawing makes use of diamond wire consisting of a steel wire core onto which diamond particles are plated using a metal, usually nickel. Fig. 1 shows the anatomy of a diamond wire – steel core, metal coating and embedded diamond particles. There are several key advantages of diamond wire sawing: higher throughput is achievable, less wire is required per wafer, there is no slurry, and kerf recycling is possible. In addition, diamond wire sawing is expected to result in lower total thickness variation (TTV) of the wafer and in reduced metal contamination of the Si surface [1,2]. Reports also indicate that saw damage depths are lower with diamond wire sawing than with slurry-based sawing [1,3]. As a result, there has been a significant gain in momentum for diamond wire sawing.

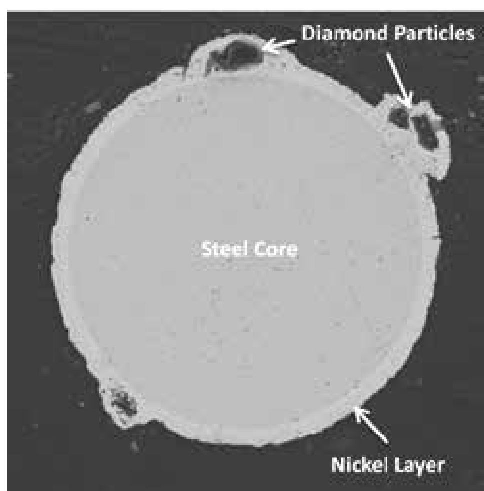


Figure 1. Scanning electron microscope (SEM) image of a diamond wire cross section, showing the core and the metal coating with embedded diamonds.

"There has been a significant gain in momentum for diamond wire sawing"

However, diamond wire saws have been shown to decrease the breakage force for c-Si wafers by as much as a half, because of the formation of elongated cracks on the silicon surface during sawing [4]. The surfaces of slurry-sliced wafers tend to have more pits, while diamond-wire-sliced wafers exhibit scratches. The difference between the surfaces of diamond-wire-based and slurry-based cut silicon is due to the different cutting mechanisms. For slurry-based sawing, the accepted mechanism is the 'rolling-indenting' model, where SiC particles roll across the surface and carve out sections of silicon. In contrast, diamond wire sawing tends to cut silicon wafers by 'plastic ploughing' and 'brittle chip-off' methods [3].

As a result, the surface morphology of diamond-wire-sawn wafers has far-reaching effects, both technological and economical, down the value chain; these must be identified and addressed for diamond wire sawing to be prevalent by 2018. This article identifies the key challenges of diamond wire sawing from the perspective of diamond wire

manufacturers, coolant manufacturers, diamond wire saw manufacturers, metrology manufacturers, solar cell manufacturers and academic researchers.

Current outlook

The aim of the SEMI International Technology Roadmap for Photovoltaic (ITRPV) is to inform suppliers and customers about expected technology trends in the field of crystalline silicon (c-Si) PV and to add to discussions on required improvements and standards. The objective of the roadmap is not to recommend detailed technical solutions for identified areas of improvement, but to emphasize to the PV community the need for improvement and to encourage the effort to identify comprehensive solutions.

The fifth edition of the ITRPV (2014) [5] was jointly prepared by 28 leading international c-Si solar cell manufacturers, module manufacturers, silicon producers, wafer suppliers, PV equipment suppliers and production material providers, as well as PV research institutes. It covers the entire PV value chain, from crystallization, wafering and cell manufacturing to module manufacturing and PV systems. Significant parameters set out in earlier editions are reviewed along with some new ones, and discussions about emerging trends in the PV industry are reported. The following outlined topics specifically focus on diamond wire sawing.

Materials – crystallization and wafering

A significant improvement in cost reductions in the wafering process is expected as a consequence of the introduction of diamond wire sawing, especially for monocrystalline Si (mono-Si) wafers. Diamond wire sawing is expected to become widespread for mono-Si wafering; however, the field is open with regard to multicrystalline Si (mc-Si) wafering. Other new wafer-manufacturing techniques, especially kerfless technologies, are not expected to gain notable market shares, because of the maturity of the established sawing technologies. Fig. 2 shows the expected share of wafering technologies in volume production. The roll-out of diamond wire sawing technology requires a synchronization with cell process development.

Processes – technology

A challenging parameter is the kerf loss from slurry-based and diamond-wire-based technologies, as shown in Fig. 3. Kerf loss must decrease in order to achieve reductions in wafer thickness and silicon consumption.

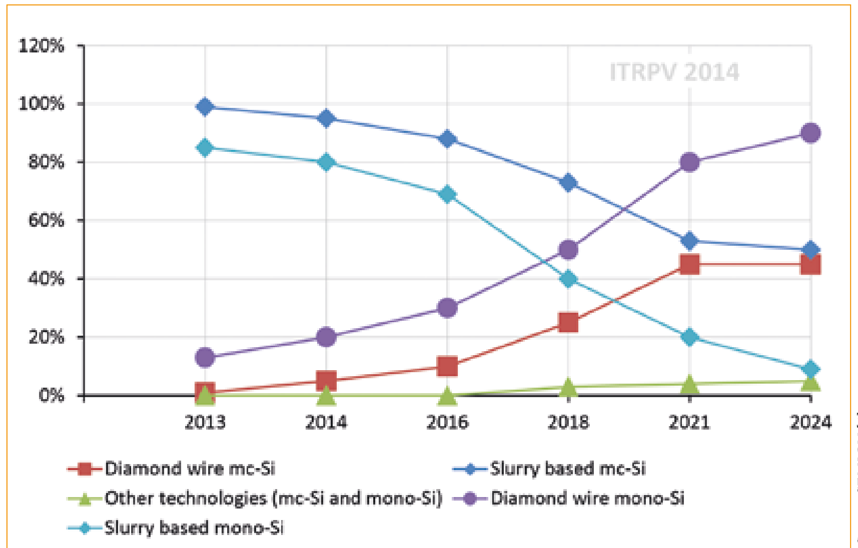


Figure 2. Respective market share of wafering technologies for mono- and mc-Si.

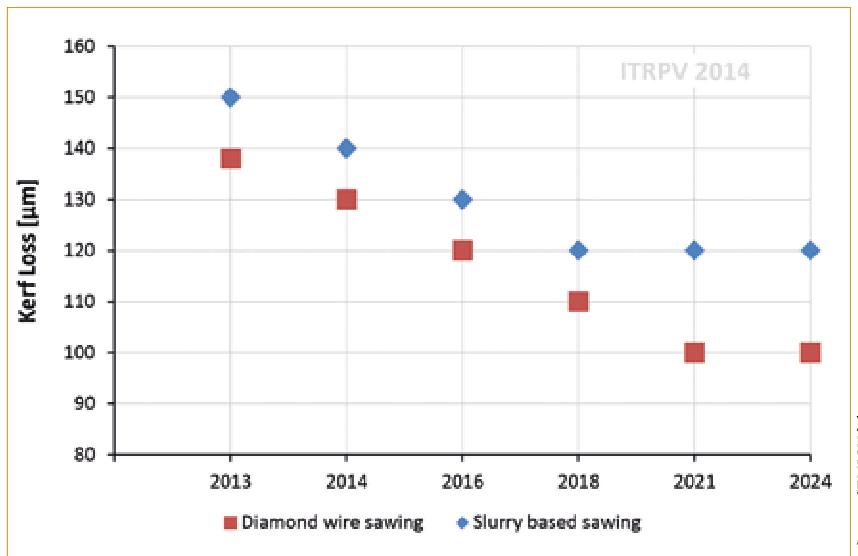


Figure 3. Prediction for kerf-loss reduction trend.

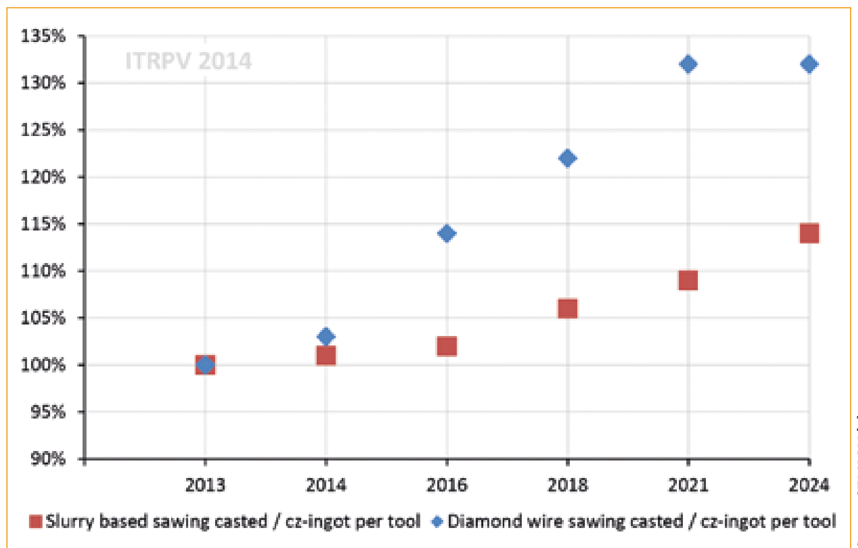


Figure 4. Throughput per tool for diamond wire and slurry-based wafer sawing.

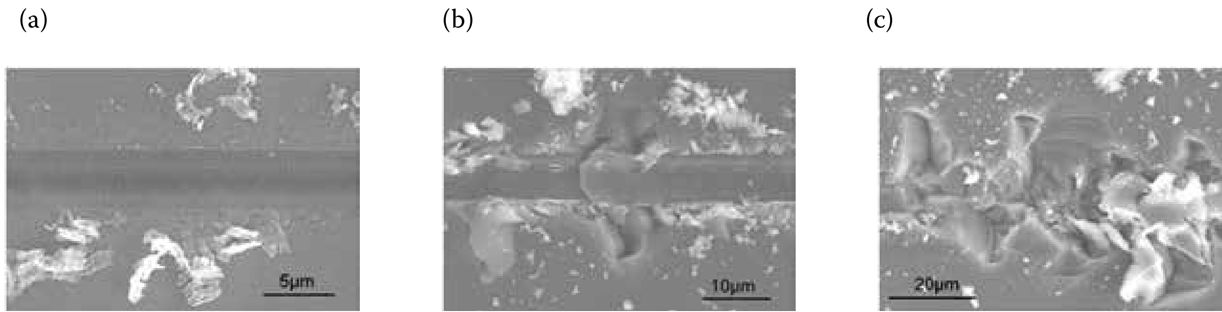


Figure 5. Scratch topography in diamond scribing of (111) mono-Si at different depths: (a) d_s= 0.12µm ductile cut; (b) d_s= 0.72µm ductile-brittle cut; (c) d_s= 1.23µm brittle cut [6,7].

Additional cost savings are expected from the introduction of diamond wire sawing processes as discussed above. Comparing the predictions of wafer thickness and kerf-loss trends beyond 2018, it is unclear if it is economically feasible to have a kerf-loss amount that is greater than the wafer thickness itself.

> "Kerf loss must decrease in order to achieve reductions in wafer thickness and silicon consumption."

Processes – manufacturing

Fig. 4 shows that diamond wire sawing throughput is expected to grow steadily over the next few years, along with the expected appearance of new tools and processes accelerated by the introduction of this technology to the market. Slurry-based wire sawing will continue to improve its throughput over the coming years, but new developments, such as structured wires, demonstrate promising and significant throughput improvements.

Short-term challenges

Increase understanding of the diamond-wire-cutting process in order to reduce damage

Unlike the traditional slurry wire sawing process, which removes material through a combined rolling and indenting action of the SiC abrasives on silicon, the material removal in diamond wire sawing is characterized by a combination of two-body abrasion and indentation mechanisms. Consequently, the surface morphology of a diamond-wire-sawn wafer is distinctly different from a slurry-sawn wafer in that it exhibits clear evidence of ductile-mode cutting in the form of horizontal striations (or saw marks) interspersed with localized regions of brittle fracture.

It is well known that brittle materials such as silicon and other ceramics can exhibit pseudo-plastic (or ductile) behaviour under certain loading conditions that are induced by a combination of the cutting parameters (e.g. ingot/wire feed and speed) and grit geometry. This is the same behaviour that is responsible for the ductile saw marks visible on diamond-wire-sawn wafers. In theory, if the abrasive shape and cutting conditions can be controlled to promote ductile mode cutting behaviour at all points of interaction between the diamond abrasives and silicon, then a damage-free (or crack-free) surface can be achieved. This, in turn, can yield wafers that are mechanically much stronger than those obtained using current wire sawing technology. This section highlights the need and methods for further improving our fundamental understanding of the diamond wire sawing process and related surface/subsurface damage in order to further reduce damage.

Low-speed diamond-scribing studies using idealized indenter (or 'grit') shapes designed to elucidate the fundamental physics of material removal and associated surface/subsurface damage in silicon have shown that ductile-mode cutting behaviour is obtained at very small depths of cut (equivalent to the

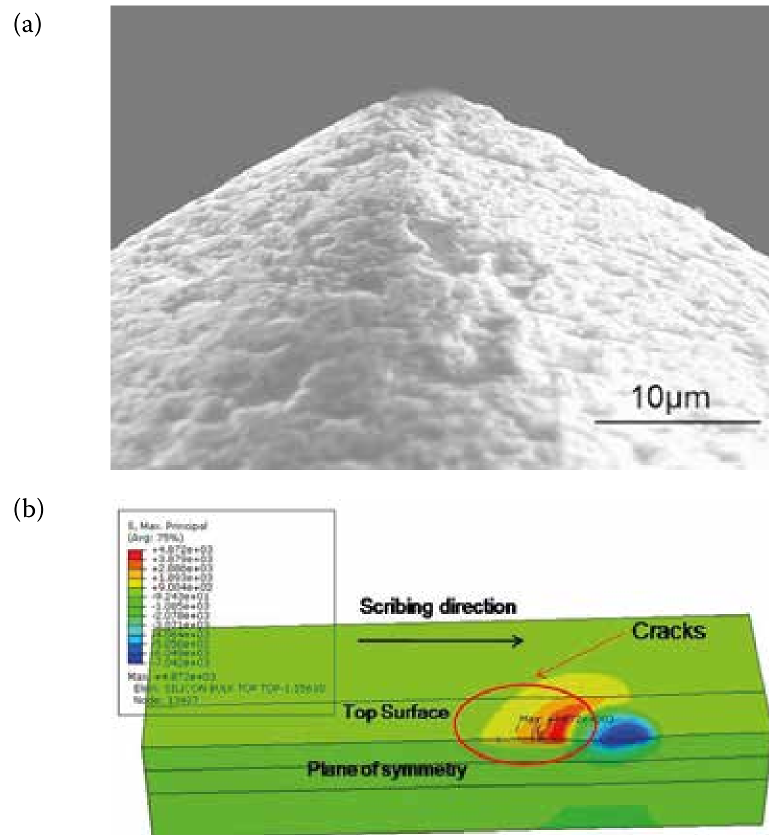


Figure 6. (a) SEM image of 'sharp'-tipped diamond scriber; (b) associated simulated stress state and surface cracking [6].

ingot/wire feed in wire sawing) (see Fig. 5). These studies also show that the abrasive shape plays a major role in determining the surface and subsurface cracking behaviour of the material. Specifically, the stress state produced in silicon during grit–material interaction is strongly influenced by the grit shape, and certain stress states (corresponding to the grit shape) cause ductile-to-brittle transition at lower depths of cut, leading to surface and/or subsurface cracking behaviour.

Fig. 6 shows an example of the simulated stress state and associated surface cracking for an idealized diamond indenter with a 'sharp' tip. Surface and subsurface cracking can also be 'delayed' by lowering the coefficient of friction between the diamond abrasive and the silicon [6], which can be accomplished in practice by suitably engineering the water-based cutting fluid used in diamond wire sawing.

At present, the industry use of diamond wire sawing is mostly limited to the production of mono-Si wafers, for which the process is economical. However, given the microstructural complexity of multicrystalline silicon (arising from the presence of grain boundaries, higher density of dislocations, carbide/nitride inclusions, etc.), the process is not economical for the wafering of multi-Si. Diamond-scribing experiments aimed at understanding the influence of some of the aforementioned crystal defects on the cutting characteristics of multicrystalline silicon suggest that local dislocation density variations (both within the grain and at the grain boundary) cause local mechanical property variations, which lead to local variations in the cutting characteristics and the resulting surface morphology [8,9]. Further work on this material is needed.

Accurately characterize surface and subsurface damage

The surface/subsurface damage produced by diamond wire cutting is the result of stress induced by the diamond particles, the wire, and the dynamics of cutting; the latter includes microcleavage of silicon by diamond chips, forward and reverse movement of the wire, and wobbling and vibrations of the wafer/ingot during cutting. The damage to the silicon lattice is in the form of:

1. Dislocations that remain 'frozen in' close to the surface, because the dislocation propagation velocity at the cutting temperature is very low.

2. Phase transformations (into amorphous silicon, and several possible phases of crystalline silicon).

3. Microcracks.

4. Lattice distortions that do not have accompanying dislocations.

It is important to accurately determine how far these defects reach into the wafer.

Angle polish method

The most common technique for determining surface damage is to angle polish a small section of wafer, followed by defect etching. To do this, a section of a wafer is mounted on a bevelled chuck and typically polished at 10° using progressively decreasing grit size and a final chemical mechanical polish (CMP). The CMP step ensures that the angle-polished region does not have any damage that can interfere with defect delineation by chemical etching.

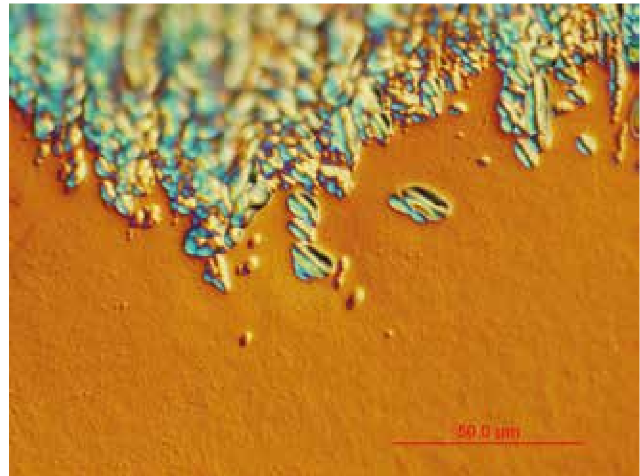
Fig. 7 shows an optical microscope image of a defect-etched/angle-polished sample from a diamond-wire-sawn wafer: it shows the vicinity of the original as-cut and the angle-polished regions. The as-cut surface itself is very heavily dislocated, and some of the dislocations penetrate deep below the surface into the polished region. It should be pointed out that waviness of the unpolished region is due to the roughness of the cut surface. The maximum depth of damage is 5.6µm.

The angle-polishing/defect-etching process detects the mechanical manifestations of the damage and is influenced by surface roughness. Identifying the demarcation between as-cut and polished regions is subjective.

Effective minority-carrier lifetime method

A new method that uses an electronic property (surface recombination velocity – SRV) has been developed and recently modified for use with detection using the measurement of minority-carrier lifetime. This technique is based on measuring the effective minority-carrier lifetime τ_{eff} as a function of depth. The procedure consists of removing thin layers from the wafer surfaces by chemical etching and measuring the minority-carrier lifetime after each etch

(a)



(b)

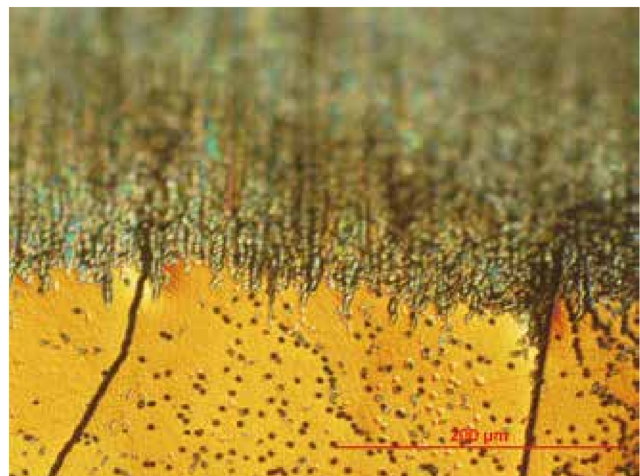


Figure 7. 10º angle-polished and defect-etched (using Sopori etch) diamond-wire-cut silicon samples, showing damage penetration into the bulk: (a) mono-Si wafer; (b) multi-Si wafer.

step. The effective lifetime increases as the thickness is removed and reaches a constant value; the thickness removed when the lifetime reaches the peak value is the damage depth. This new method is very accurate and has many advantages, including the fact that it can be easily adapted in a solar cell facility.

Fig. 8 shows a plot of the measurements of lifetime vs. thickness per side removed for a diamond-wire-sawn wafer. It is seen that there is a rapid increase in lifetime for etched depths below 3µm, followed by a gradual increase from ~3µm to ~5µm, and the lifetime then begins to drop. Since the decrease in surface recombination velocity (S) for $S < 50$cm/s has only a small effect on increasing τ_{eff} (especially for low lifetimes), this increase is small; τ_{eff} then decreases because wafer thickness is reduced. Because S is very sensitive to damage, the highest lifetime (at around 5µm) implies the damage is fully removed. This new method is very versatile and has many advantages, including:

1. It can determine the average damage depth over a large area, which is more appropriate for solar cell fabrication.

2. The measurement system is readily available in most solar cell laboratories.

3. It can be applied to wafers that have significant surface roughness (e.g. diamond-wire-sawn wafers).

Infrared polariscopy method

Residual stresses in the starting wafers and the finished cells can affect the electrical behaviour of devices, as well as eventually leading to the fracture and failure of cells [10,11]. One source of residual stress is sawing. Sawing generates damage in the form of plasticity and cracks on both sides of the wafer surface, and it is the interaction of the dislocations, cracks and other defects that leads to stress [12]. This stress is referred to as *residual stress*, since it exists without any externally applied loads. The level of this residual stress varies over the surface and can easily reach or exceed typical stresses imparted by wafer handling. Residual stress varies with the sawing conditions, such as the type of sawing used (diamond wire vs. slurry), the entry point of the wire, the feed rate and the speed of the wire [13]. This surface damage and the associated residual stress can be removed by etching, but to effectively do so requires an understanding of how the residual stress is produced, its magnitude, its sign (tensile or compressive) and its depth into the wafer.

There are a few suitable techniques available for measuring residual stress; of these, near-infrared (NIR) digital photoelasticity is attractive because of its simplicity, accuracy, sensitivity to localized stress, and full-field, non-contact nature. This technique can generate, in a matter of seconds, full-wafer residual stress maps with an accuracy of 1MPa and at a spatial resolution of just 20µm^2. In NIR digital photoelasticity, polarized light is transmitted through a birefringent material, such as a silicon wafer, as pictured in Fig. 9. As the polarizing optics are rotated to known angles, a digital camera can record the relative phase retardation of the polarized light at each point in the wafer; this retardation can then be associated with the localized residual stress by using well-established techniques. Specifically, the stress measured by this technique is the maximum shear stress. However, the maximum shear stress alone is not sufficient for capturing the true nature of the stresses due to sawing conditions: an additional image-processing algorithm must be applied in order to determine the normal stress components oriented to the wafer edges. To accomplish this task, unique algorithms were developed to extract the normal stress maps, which play a key role in understanding the relation of the sawing conditions to other characteristics of the cells and, of course, to possible failure of the wafers.

As an example, consider the residual stress values shown in Fig. 10, obtained for an as-sawn Cz silicon wafer: Fig. 10(a) shows the maximum shear stress plot, and Fig. 10(b) and (c) show the separated normal stress components. In Fig. 10(a) and (b), note the presence of curvature lines caused by wire sawing. Although some sawing damage is visible in the maximum shear stress map in Fig. 10(a), the x-direction normal stress component seen in Fig. 10(b) clearly indicates significant tensile stresses perpendicular to the sawing direction. By leveraging this measurement technique, both the sawing and the

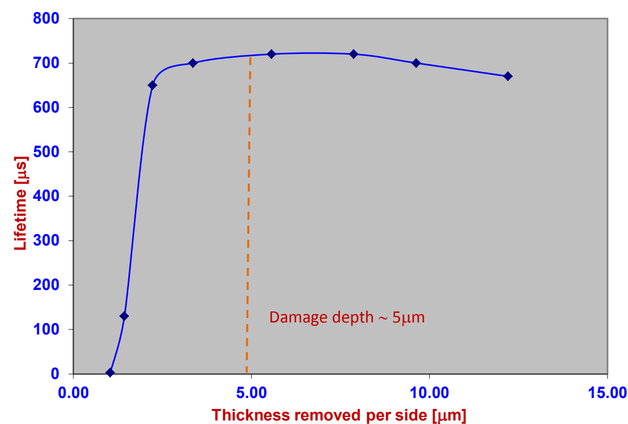


Figure 8. Measured lifetime as a function of depth for a diamond-wire-sawn wafer. The damage depth determined by this technique (4.8µm) agrees very well with the average depth resulting from the angle-polishing/defect-etching technique.

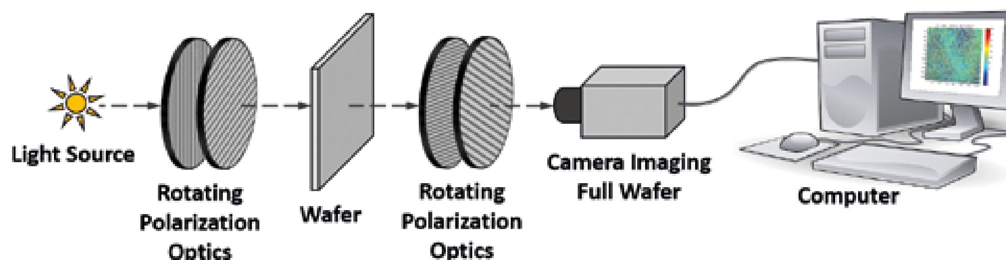


Figure 9. Schematic of the imaging technique used to generate full-field stress maps with NIR digital photoelasticity.

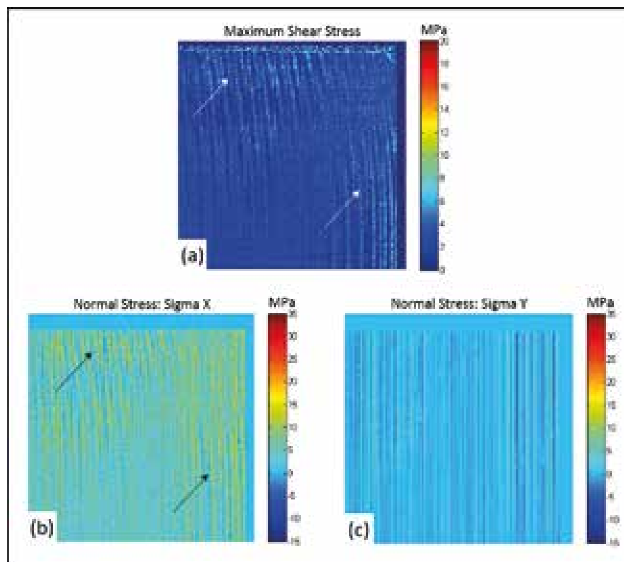


Figure 10. Stress plots of a Cz silicon wafer, generated through NIR digital photoelasticity: (a) maximum residual shear stress; (b) normal stress component σ_x; (c) normal stress component σ_y.

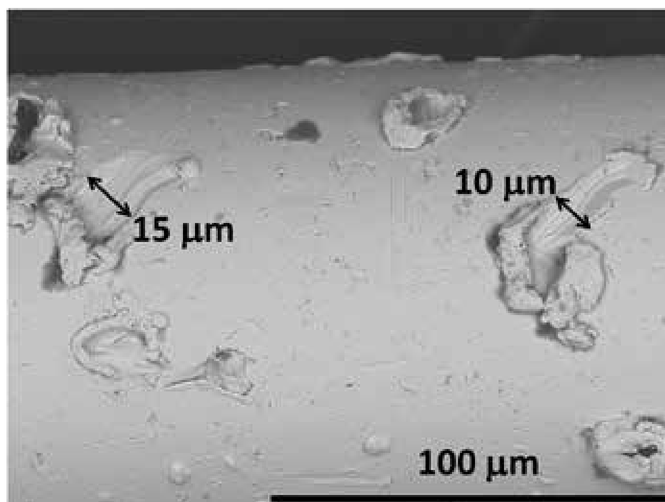


Figure 11. Diamond pull-out.

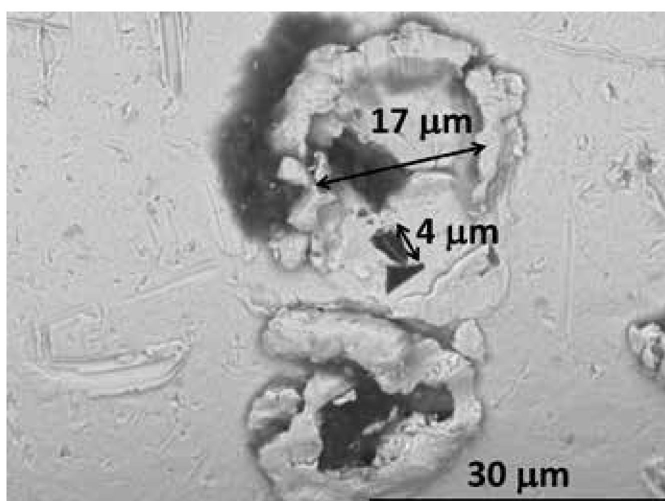


Figure 12. Diamond fracture.

etching process of the wafer can be monitored and optimized.

"The identification of failure modes and wear mechanisms will help increase the wire durability and material lifetime, and may also reduce wire consumption."

Identify failure modes and wear mechanisms

Diamond wire wear and failure during silicon wafer slicing is influenced by a number of factors, including the properties of the diamond wire and its components (steel core, diamond particles, plating metal), wire saw parameters, mechanical properties of the silicon, and coolant chemicals used to aid slicing [14–17]. The identification of failure modes and wear mechanisms will help increase the wire durability and material lifetime, and may also reduce wire consumption.

Diamond wire and components

The diamonds employed in diamond wire saws are attached to the surface of steel cores by means of electroplated nickel; thus, the adhesion of the diamonds depends on the quality of the electroplated metal. Furthermore, the friability of the diamonds will play a crucial role in the diamonds' ability to abrade the silicon. Higher friability will lead to less abrasion and could increase wafer surface damage. SEM images of used diamond wires demonstrate several wear mechanisms of the wires.

First, as mentioned, diamond adhesion to the wire can be poor. As shown in Fig. 11, diamonds can be 'pulled out' of the wire, clearly damaging the wire surface, and possibly damaging the wafer too. Not all pull-outs, however, are accompanied by scratches, as also evidenced by Fig. 11. The hole at the top clearly had a diamond at one time, but this has become detached during use. Factors that influence a diamond pull-out could be manufacturing based or application based. In terms of manufacturing, the effectiveness of the electroplating process in adequately attaching the diamonds will play an important role in retaining the wire's abrasion. However, the speed and force of the wire on the ingot will quite likely also play a role, as will the extent to which the wire is used. The more the wire is used, the less nickel there is surrounding the diamonds and the greater the chances are of diamond pull-outs.

Another wear mechanism of diamond wire is diamond fracturing: in this mechanism, the diamond size is reduced to less than 5µm (see Fig. 12). At this size, the diamonds will again be removed from the wire and the abrasiveness will decrease. This mechanism is a function of the choice of diamond, and should be considered when manufacturing diamond wire.

Some ex situ testing revealed that the adhesion between the steel core and metal coating can be a challenge. In these tests, a wire was drawn in tension until it failed, at which point the fractured ends were examined by SEM. At times, the wires showed some separation between the core and coating, suggesting some adhesion issues (see Fig. 13). The extent to which this failure mode impacts wire performance in the field is unknown.

The surface of the wire also points to the wire dynamics during cutting. Several wires were examined after slicing wafers, and it was observed that scratches were present over the surface. It was also observed that the scratches extended along the length of the wire and in several directions (Fig. 14). These scratches could be the result of diamond or silicon particles damaging the surface of the wire. It is recognized that the nickel surface is much softer than silicon, so the damage to the wire is probably more than what would be observed on the wafer. However, it does indicate to some extent the types of particle that are present during diamond wire wafer slicing.

Wire saw parameters and mechanical properties of the silicon

Numerous wire saw parameters were evaluated during slicing experiments with 156mm silicon ingots. It was concluded that, within typical setting ranges, fresh wire feed rate into the web had the largest effect on wire wear. Diamond wire specifications were fixed, with a core wire diameter of 120µm and electroplated diamond particles in the range 10–20µm; hence there were no significant variations in wire properties that might affect wear. Three different 156mm silicon ingots were sliced:

- Ingot A: monocrystalline Cz p-type boron-doped silicon with <100> orientation.
- Ingot B: monocrystalline MCz p-type boron-doped silicon with <100> orientation.
- Ingot C: p-type multicrystalline silicon.

The slicing coolant for all experiments was Aquaslice, diluted at 2% in city water.

Slicing was performed using a Takatori WSD-K2 R&D-scale diamond wire saw, which allowed the number of wires in the web to be varied from 1 to 29. In most cases, six wires were used, generating five wafers per experiment. Fresh wire feed rate was varied from 1.0m/min to 2.5m/min; typical slicing time was 260min and hence the total wire use per experiment varied between 260 and 650m. Wire tension and speed were kept constant at 20N and 600m/min respectively.

Wire wear was determined by measuring the diameter of the wire at 50m intervals before and after each experiment and expressed as a percentage of the original wire diameter. Wire wear was normalized to percentage of slicing completion; this allowed experiments in which the wire broke during slicing to be compared with successfully completed experiments. A means of comparing wire wear measured under various conditions was required: a wire-to-silicon contact ratio was therefore developed and defined as

$$\frac{\textit{Amount of wire used}\ [\mathrm{m}]}{\textit{Cut depth}\ [\mathrm{mm}] * \textit{Number of wires in web}} \quad (1)$$

Higher values of this ratio can represent low numbers of wires or high wire feed rates, or both; lower values represent high numbers of wires in the web or low wire feed rates, or both.

Normalized wire wear vs. wire-to-silicon contact ratio results for ingots A, B and C are plotted in Fig. 15. As expected, wire wear increased with decreasing wire-to-silicon contact ratio. Apart from single-wire conditions, the wear for ingot B was considerably higher than for ingot A, implying that the MCz silicon was more difficult to slice than

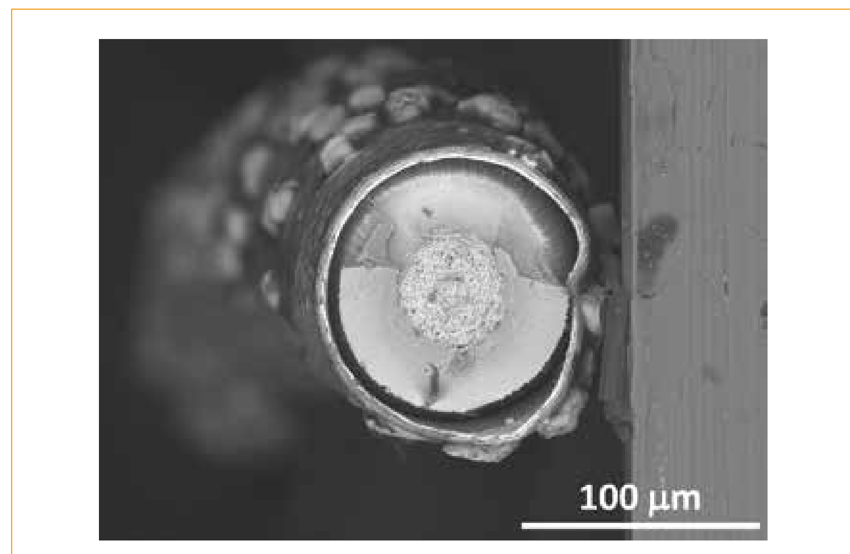


Figure 13. SEM cross section of an ex situ failed wire.

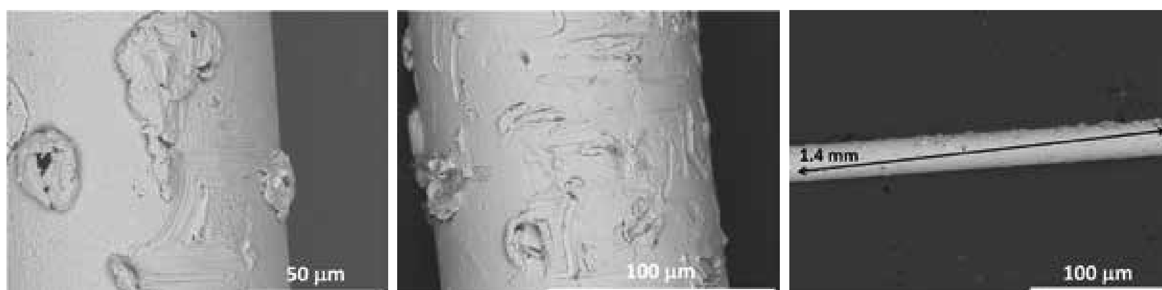


Figure 14. Several scratch directions on used wires.

Cz silicon. These results correlate well with measured Vickers hardness values of 532kg/mm² and 658kg/mm² for ingots A and B respectively. Vickers hardness data were not obtained for ingot C (multicrystalline); however, the slicing of ingot C appeared to cause wire wear somewhere between that for the MCz ingot B and for the Cz ingot A.

"There is a need for real-time inspection of the diamond wire for quality control during diamond wire production and/or for process control during silicon wafering."

Implement non-destructive inspection metrology for diamond wire

There is a need for real-time inspection of the diamond wire for quality control during diamond wire production and/or for process control during silicon wafering (e.g. real-time monitoring of the level of wear of diamond wire during sawing). This section describes novel solutions for an in-line and non-destructive inspection of diamond wire. However, the in-line implementation of these metrology techniques dictates that they operate at certain speeds and within harsh environments.

Optical inspection system

A new optical inspection system capable of detecting defects – down to a few microns in size – that are only on the surface of diamond wires moving at speeds of up to 10m/s was recently reported [18]. This novel non-contact metrology relies on four high-speed cameras that can take 10,000 images per second and process them in real time. An obvious concern is the maintenance of the optics in the harsh wafering environment.

Resonant vibrations of the diamond wire

Another approach, which can be applied at the back-end of diamond wire production and diamond wire silicon wafering, is based on the resonant vibrations (RVs) of the diamond wire. Fundamentally, this method assesses the diamond wire mechanical quality using the physics of a vibrating string, by agitating the diamond wire segment by a non-contact actuator and measuring an RV curve with a non-contact acoustic probe in a selected frequency range. Characteristics of the resonance curve – peak frequency, bandwidth and amplitude – allow a fast non-destructive characterization of the diamond wire quality.

The RV method was initially demonstrated on a stationary diamond wire sample and then expanded to a moving diamond wire, which is a model of a real-time wafering process. The following experimental data validated the RV approach:

- The RV frequency measured on new and used samples of diamond wire from the same vendor shows a shift on the used samples.
- The RV frequency gradually shifts with

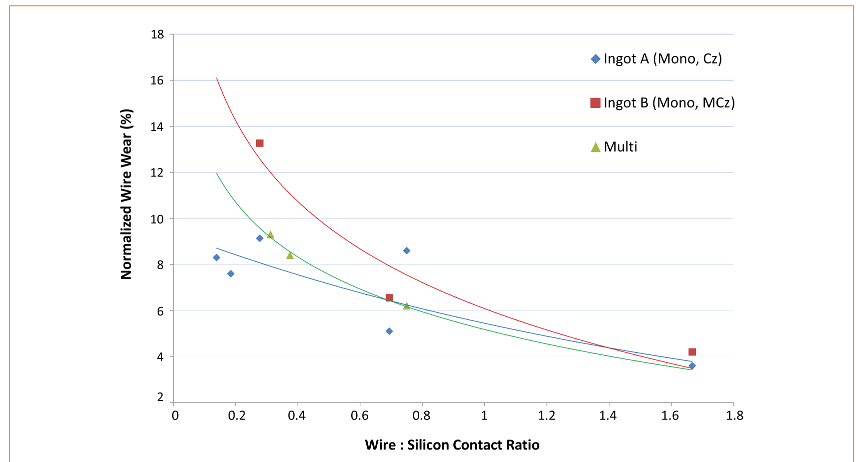


Figure 15. Effect of wire-to-silicon contact ratio on normalized wire wear. (Note: on the basis of a typical fresh wire diameter of 144µm, maximum wire wear (all diamonds lost) would be around 17%.)

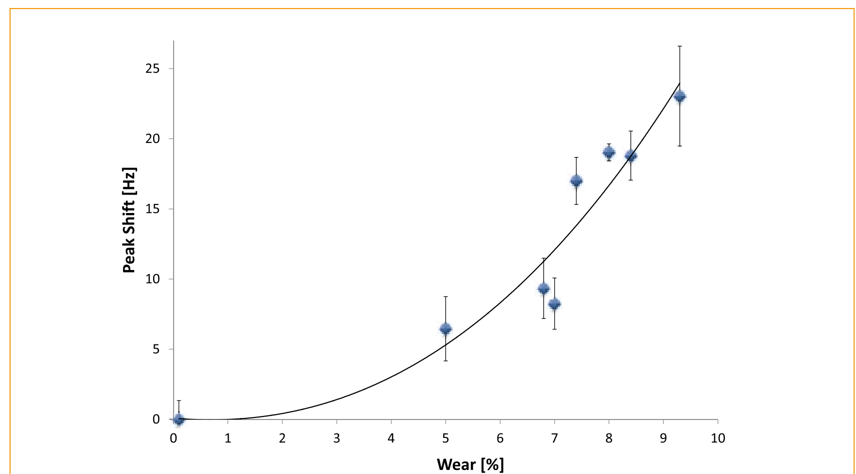


Figure 16. RV vs. wear in % of wire diameter. The error bars represent standard deviations for three samples from each diamond wire.

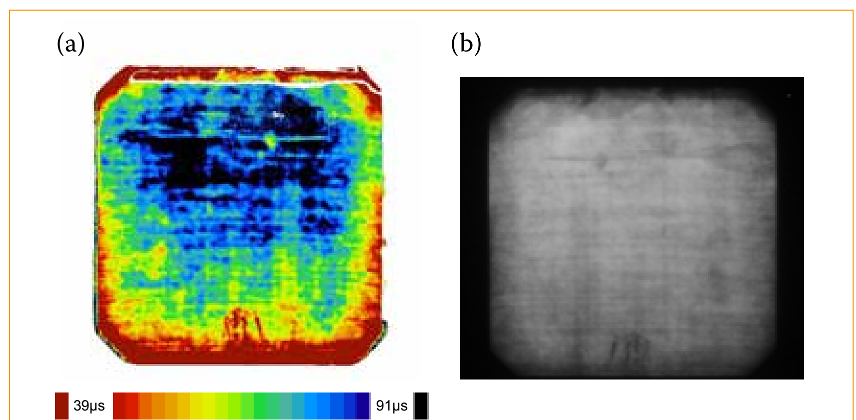


Figure 17. (a) Minority-carrier lifetime and (b) PL maps of a diamond-wire-cut wafer after etching a thin layer from the surfaces in order to sufficiently lower the SRV to enable the making of the maps. (Note the taper in the damage profile, with higher damage towards the bottom edge.)

Source: LIST/UCF

increasing metal plating thickness.

- The RV frequency is reduced with increased density of the diamond particles.
- A correlation exists between the percentage of diamond wire wear and the shift in RV frequency (see Fig. 16).

The RV method is able to detect internal flaws below the surface of the diamond wire components (core, metal layers, etc.) and is compatible with the harsh wafering environment. Theoretically, it has been determined that the characteristics of the resonance curve do not change at speeds upwards of 500m/s, which makes it a viable candidate for monitoring diamond wire during sawing as the wire speed continues to scale up.

Impact of diamond-wire-sawn wafers on solar cell manufacturing

The surface properties of diamond-wire-sawn wafers and slurry-sawn wafers are different, which impacts the entire solar cell production process. Chemical etching of mono-Si wafers by NaOH- or KOH-based solutions is extensively being used for texturing to reduce the surface reflectance and for providing very effective light trapping of wafer-based Si solar cells. The etching is typically done using KOH solutions in a concentration range of 30–40%, at 70°C. Under these conditions, texturing occurs because the etch rate in the <100> direction is very high compared with that in the <111> direction, causing exposure of the (111) faces and a concomitant formation of pyramids. The texturing of (100) wafers reduces the reflectance to about 10%, which can be further lowered by an anti-reflection coating. It is known that texturing of wafers works well only in the presence of surface damage; this is very fortunate because it allows texturing to be combined with the surface damage removal step, yielding a uniform texture on slurry-cut wafers.

However, the surface roughness of diamond-sawn wafers is greater than that of slurry-cut wafers, and the wafer surfaces exhibit striations, which can interfere with texturing. Fig. 17 illustrates the damage and surface roughness effects in a diamond-wire-sawn wafer. Fig. 17(a) is a minority-carrier lifetime map of a wafer, which was chemically etched to remove a thin layer of the damaged surface (to enable lifetime and photoluminescence – PL – measurements); the regions of lower lifetime correspond to higher damage. Fig. 17(b) is a PL map of the same wafer, confirming the effect of striations.

Fig. 18 is a reflectance map of a standard diamond-cut, textured wafer, showing a modulation in the reflectance because of the surface morphology generated by diamond cutting and retained through texturing. This results in a non-uniform texture whose effect is estimated to degrade cell efficiency by at least 0.5% abs. To process diamond-wire-sawn wafers, production lines developed for slurry-sawn wafers need to be adapted. Hence, it is expected that improving the texturing of the sawn wafers can recover the loss in cell efficiency, and will also simplify cell processing (such as metallization).

It has been shown that diamond-wire-sawn wafers have thicker oxide layers than slurry-sawn wafers, and that the surface layer also contains significant amounts of amorphous silicon [19]. These layers have an impact on the wet-chemical processes used for saw damage removal and texturization. It has been reported that the etch rate of amorphous silicon is slower by a factor of 30 in the (001) surface [20], thereby increasing valuable processing time in order to achieve the target wafer surface condition. Moreover, thicker oxide layers might act as a masking layer during texturization, which leads to lower light trapping when compared with slurry-sawn wafers. An example is shown in the SEM image in Fig. 19. When subjected to the same texturization process, the diamond-wire-sawn wafer still has untextured regions, while the slurry-sawn wafer is fully textured.

Long-term challenges

Reduce kerf loss below 80µm

As the solar industry continues to move to higher-efficiency cell performance, it is also focusing on ways to reduce wafer cost, which is still a big portion of the module cost. The main cost contributor is the silicon and can be split into wafer-thickness and kerf-loss categories. While the industry looks to save on cost, wafer manufacturers are investigating ways of reducing wafer thickness and kerf loss.

Kerf loss is determined by the wire core size used by the slicing technology. The limitation for reducing the wire core with slurry-slicing technology is around 110µm; however, with diamond-wire-slicing technology the wire core can be reduced further. The diamond wire core used today is around 100µm, with the trend moving to less than 70µm within the next two years. The use of such a thin wire core, however, introduces key technical challenges: one of these is that, as the wire core diminishes, so does its intrinsic breaking load. The breaking-load curve limitation is illustrated in Fig. 20.

As shown in Fig. 20, a 70µm wire core should have a working tension of around 8N, with a breaking load of 15N, while a 120µm wire core can operate at 25N and have a breaking load of 45N. This provides only a 7N safety margin to operate a 70µm wire core below its physical limitation, while the safety margin is 20N for a 120µm wire core. Consequently, both the working-tension control accuracy and the pulley-inertia management must be improved to accommodate the wire limitation.

The wire management of a new wire saw platform will have to include

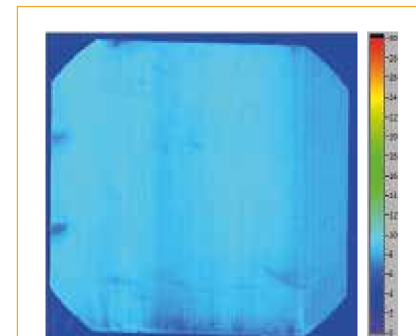


Figure 18. A reflectance map of a textured wafer, showing previous striations after texture etching. (Note: there are other 'marks' on the textured wafer from the holder.)

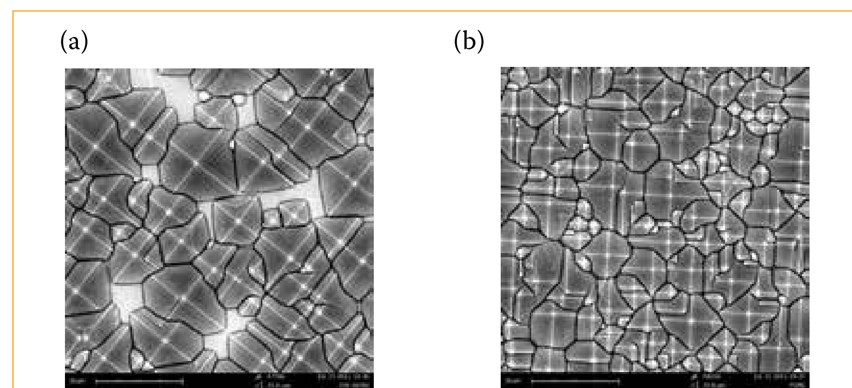


Figure 19. SEM of the texture for (a) a diamond wire cut, and (b) a slurry-based cut.

highly accurate tension control, a low-inertia pulley system, and an innovative cutting movement designed to optimize cutting pressure and silicon removal. These features will compensate for the thin wire core limitations and optimize the slicing trade-offs in terms of cutting feed rate and diamond wire usage. A kerf-loss reduction of 20µm achieved by using a thinner wire core would yield significant silicon cost savings and therefore wafer cost savings. The new wire saw platform addresses these key technical challenges by supporting improvements – such as an innovative cutting motion, accurate wire-tension control and low-inertia pulley systems – resulting in higher wafer quality.

Enable diamond-wire-sawn wafer thickness below 140µm

Another big opportunity for lowering wafer cost is by decreasing wafer thickness. The current monocrystalline wafer thickness is around 180µm, which represents around 60% of the silicon cost. The goal is to drive the wafer thickness below 140µm; at today's cost, a reduction of 40µm can represent a saving of around $0.10 per wafer. This cost reduction can help drive the adoption of monocrystalline advanced cell structures, such as interdigitated back contact (IBC) solar cells and heterojunction (HJT) silicon-based solar cells. An additional, and potentially more critical, motivation for reducing wafer thickness concerns cell efficiency. There is an optimal wafer thickness for which the best cell efficiency can be obtained: according to studies, this is approximately 50µm [21].

However, there exist barriers to producing ultrathin wafers, so an intermediate step is to first reduce wafer thickness from 180µm to 140µm. Even for this level of reduction, there are still barriers, including:

1. At the saw level – motorization, gluing and singulation.

2. At the cell level – mechanical yield and wafer handling.

3. At the module level – stringing and tabbing thermal effects, leading to mechanical and electrical yield issues.

At the saw level, cutting ultrathin wafers with ultrathin kerf loss will require an increase in machine power: the more wafers to cut, the more power required (based on the cutting forces) to remove the silicon materials from the cutting channel. The gluing step will also need to be improved, as the cross section of the wafer reduces the area holding the wafers by the glue. The saw must be equipped with an advanced wafer box to prevent wafers falling during the cut when wafer thickness drops below 180µm. In addition, an innovative cutting motion can improve wafer strength and will therefore help wafer handling as wafer thickness is further reduced. For example, it was recently reported by Applied Materials that a technology called OS2 (oriented synchronized slicing) can increase wafer strength by 6%.

Automatic singulation may be required for handling the emerging fragile ultrathin wafers. Eventually, the singulation can be integrated with the saw to minimize broken wafers and optimize mechanical yield. Cells produced from wafers of thickness below 140µm will require soft handling to prevent breakage, which leads to a mechanical yield issue. It is a well-known fact that the force required to break a wafer decreases as the wafer becomes thinner, while the wafer flexibility increases. In order to accommodate lower thicknesses, screen printers must allow for advanced handling schemes. At the module level, to minimize mechanical yield loss, new and innovative modelling structures, such as the backsheet with back-side cell structures, need to be introduced.

All the above factors are slowing down the rate of industry adoption of wafers below 140µm.

"Increased collaboration on a technical wafer-cost roadmap will be crucial in order to help the industry achieve further cost reductions."

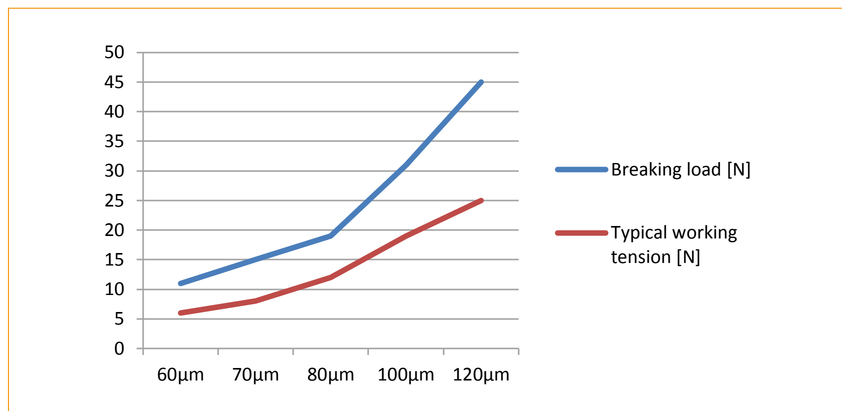


Figure 20. Breaking-load curve limitation.

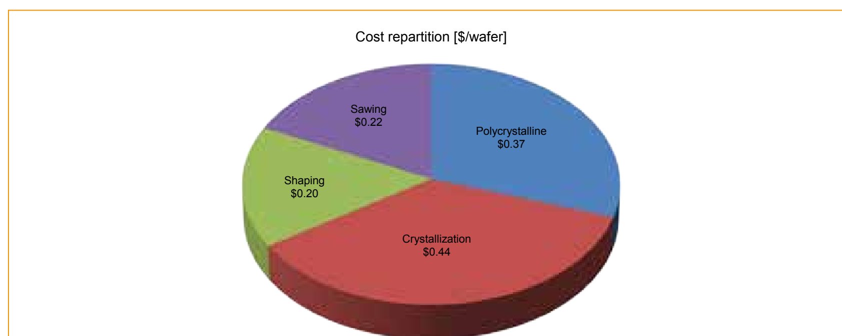


Figure 21. Monocrystalline wafer cost breakdown.

Source: Applied Materials

Enable a wafer price below $0.70/wafer

Increased collaboration on a technical wafer-cost roadmap will be crucial in order to help the industry achieve further cost reductions, at both cost per watt and manufacturing cost per wafer levels. This wafer-cost roadmap should take into account several major inputs in order to reduce the wafer-slicing cost. Different aspects – such as polycrystalline, crystallization, wafer-slicing conversion and consumables costs – can be evaluated separately or in combination. This section discusses a roadmap and the associated challenges for achieving a wafer price below $0.70 and a levelized cost of electricity (LCOE) below $0.06/kWh.

Barriers to achieving under $0.70/wafer

Today's cost of a multicrystalline wafer (156mm × 156mm) is in the neighbourhood of $0.90, against $1.20 for a monocrystalline wafer of the same size. The industry has been able to drastically reduce the multicrystalline wafer cost over the last decade by introducing high-efficiency multicrystallization techniques (higher material efficiency), lowering the wafering cost (leveraging cost of consumables)

and implementing production-scale manufacturing accompanied by market consolidation. These improvements are reaching their limits for multicrystalline wafers; however, there is still room for significant improvements in the case of monocrystalline wafers. A breakdown of the monocrystalline wafer cost is given in Fig. 21.

Improvements are being made in the following areas:

- Polycrystalline cost reduction through the implementation of advanced fluidized bed reactor technology.
- Crystallization cost reduction through the use of continuous Czochralski processes (lower electricity and crucible costs).
- Wafer-slicing conversion costs at the saw level, boosting productivity, lowering wire consumption, decreasing kerf loss, and optimizing pitch for silicon saving. (Slicing-conversion cost benefits are also possible from a consumables perspective; for example, improvements in diamond wire manufacturing can lead to lower diamond wire pricing.)
- Enabling thinner wafers within the next two or three years will also be part of the wafer cost saving equation.

Assuming the industry overcomes the related challenges, and is able to introduce these advanced technologies, Table 1 shows a path to reducing the cost of monocrystalline wafers to less than $0.70.

Impact of wafer cost on cell price and LCOE

A fundamental factor driving the adoption of PV as a viable energy source is the reduction in the LCOE produced from PV. The LCOE target for PV to be competitive with the alternatives has to take into account many complex factors (including site location, module cost and efficiency, climate, interest rates, logistics, balance of systems (BOS) costs, land costs, etc.). In the USA an LCOE target of $0.06/kWh is generally believed to be a critical threshold for PV to be a viable alternative to traditional sources of energy. Two of the critical factors (module cost and module efficiency) influencing the LCOE are directly controlled by a PV (cell and module) manufacturer.

As an example, Fig. 22 shows, for a generic location in the USA (Atlanta, Georgia, with 4.66kWh/m^2/day of average daily insolation), the sensitivity of the LCOE to module efficiency and module cost under two different BOS cost assumptions. As can be seen from the shape of the LCOE contours in Fig. 22(a) and (b), the module cost becomes a more significant factor in moving to a lower LCOE either when the module efficiency is improved (contours become more vertical on the upper halves of the charts) or when the overall system costs are reduced, as evidenced from a comparison of Fig. 22(b) and Fig. 22(a). This implies that, in order to move the LCOE towards the $0.06/kWh value, it would be necessary to significantly reduce module costs, which comprise wafer costs, wafer-to-cell conversion costs and cell-to-module conversion costs. The costs for all three of these components need to be cut through reductions in the bill of materials for wafers (polysilicon costs, consumables, etc.), cells (reduced use of Ag and chemicals in cell fabrication), and modules (lower-cost encapsulant, thinner glass, etc.), as well as through reductions in processing costs. The latter is achievable by means of larger-scale and fully integrated operations through further consolidation of PV manufacturing and improvements in processing equipment (higher throughputs, lower cost of ownership).

Cheaper wafers can significantly impact the module costs and thus help lower the LCOE. In particular, the current average costs of monocrystalline wafers of ~$1.10 to $1.30 equates to a contribution of approximately $0.25/Wp to the module cost. A reduction in wafer price to ~$0.70 (enabled through a wafer thickness reduction in order to increase the wafer yield per ingot) will translate into a module cost reduction of approximately 42%, or $0.104/Wp, in module costs. This further translates into an LCOE reduction of $0.005/kWh, as can be seen from Fig. 22(a) and (b), which is a significant move towards grid parity.

"For diamond wire sawing to overtake loose-abrasive/slurry-based sawing, short- and long-term challenges need to be successfully addressed."

Conclusion

Wire sawing is expected to continue to be the workhorse of the PV industry for slicing silicon ingots into wafers with thicknesses less than 200µm, although various disruptive kerfless wafering technologies are being developed.

Cost component	2014 (slurry)	2016 (diamond wire)	2018 (diamond wire)
Wafer thickness [µm]	180	163	140
Wire diameter [µm]	110	80	60
Kerf loss [µm]	150	100	70
Pitch [µm]	330	263	210
Theoretical wafer yield [wafers/kg]	53 (19g/wafer)	66 (15g/wafer)	83 (12g/wafer)
Productivity [MW/year]	11.8	14.3	12.7
DW usage [m/wafer]	-	1.3	1.44
Yield [%]	95	98	98
TTV [µm]	< 30	< 20	< 15
Est. cost (poly) [$/wafer]	0.37	0.25	0.22
Est. cost (cryst.) [$/wafer]	0.44	0.27	0.19
Est. cost (shaping) [$/wafer]	0.20	0.12	0.09
Est. cost (sawing) [$/wafer]	0.22	0.17	0.16
Total est. cost [$/wafer]	1.23	0.88	0.66

Source: ITRPV, Applied Materials

Table 1. Monocrystalline (156mm × 156mm) cost roadmap, illustrating that a wafer cost under $0.70 is possible.

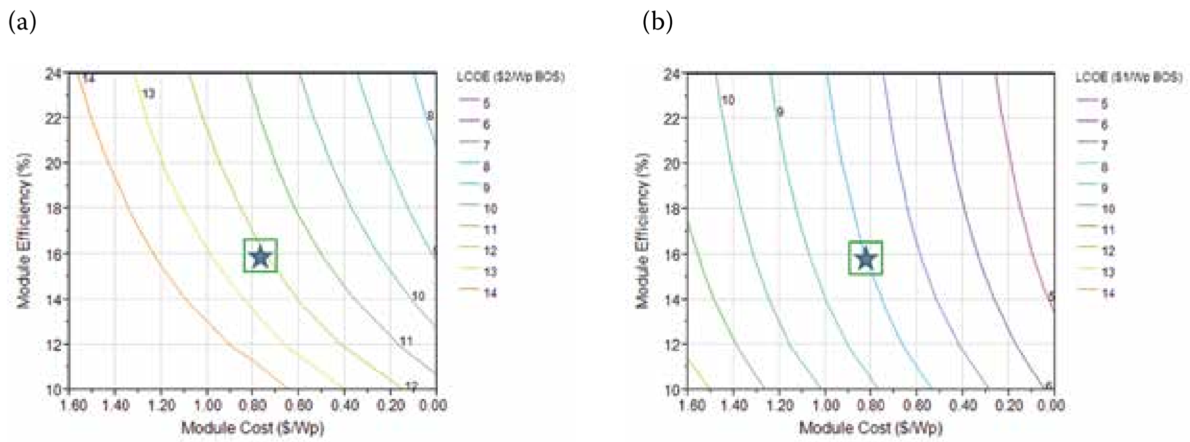


Figure 22. LCOE contours for Atlanta, Georgia, as a function of module efficiency and cost under two different cost assumptions: (a) BOS costs of $2/Wp; (b) BOS costs of $1/Wp. The inner box represents mainstream modules available on the market and their costs to the installers. LCOE calculations were performed using the system advisor model (SAM) program from NREL [22] with the following parameters: system lifetime = 30 years; performance derate = 20%; average inflation = 2.5%; real discount = 8%; loan term = 10 years; weighted average cost of capital (WACC) = 7.69%; no investment tax credits (ITC), with 50% of the total BOS costs scaled with efficiency.

Today, most companies in this industry use a loose-abrasive/slurry-based slicing process as opposed to the promising fixed-abrasive diamond wire approach. However, most industry roadmaps predict an increase in market share for diamond wire sawing for both mono- and multicrystalline silicon. For diamond wire sawing to overtake loose-abrasive/slurry-based sawing, short- and long-term challenges need to be successfully addressed. Moreover, the interdependency of the challenges dictates a resolution through a collaborative methodology and industry consensus.

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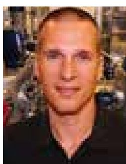

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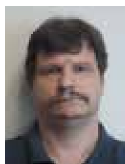

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