Achievements and challenges in crystalline silicon back-contact module technology

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ABSTRACT

The main goal of the solar industry is to reach grid parity as soon as possible. This can be achieved by reducing the manufacturing costs, by increasing conversion efficiencies and/or by improving the lifetime of solar modules. Driving down the cost of modules is not straightforward. Commercially available PV modules are typically sold with 20-year warranties, and changing these materials for economic reasons requires extensive material testing and recertification of the new module design. In the following sections, we will focus on the cost drivers of module manufacturing processes and how that could evolve into new module designs.

Introduction

Potential problems that may ensue from attempts at lowering costs in module manufacturing include yield problems, for example when thinning wafers down to below 160µm. During cell manufacture, handling of thin wafers and the impact of the various process steps such as wet chemistry, printing of metallization and high-temperature firing processes have to be reconsidered. During module manufacture, the standard soldering techniques applied to large and thin silicon solar cells can lead to cell breakage due to mechanical stresses. Therefore, innovative module design strategies have to be developed that can cope with the material properties of thin silicon wafers. Meanwhile, novel designs of the solar cells are needed to further boost the module output power. On top of that, there is little science available to assess the performance and reliability of solar modules for field operation over 20 years.

Costs

Technology advances and upscaling were the main contributors to an average module price reduction of about 10% per year in the past three decades. In the past, a main component in the module cost structure was attributed to the making of solar cells owing to large equipment costs and the considerable manpower needed to make high quality solar cells. This approach is undergoing changes now as throughputs in advanced process tools increase rapidly. This is clearly visible from Fig. 1, which shows the cost structure of crystalline silicon modules broken down for the different aspects of the value chain. The costs of solar cells were responsible for 35-40% of the total module costs in 2005, but that fraction will decrease to an estimated 25% in 2015. Material costs will become the determining cost factor throughout the value chain in the near future. In a crystalline silicon module, the main material contributions are silicon, metals and encapsulation materials.

Following the targets for cost reduction implies that crystalline silicon modules that are sold in the range of 1.7-2€/Wp today need to be in the range of 1-1.2€/Wp in five years' time. This means that a cost reduction of roughly 40-50% must be realised, but how can we achieve that? Increasing the cell efficiency from 15-16.5% today to 18%-20% five years from now will account for 50% of the targeted 'cost reduction.' These efficiencies apply to crystalline wafer-based cells that are mass-produced. The question, and the ultimate challenge for module technology, is how to achieve the other 50%.

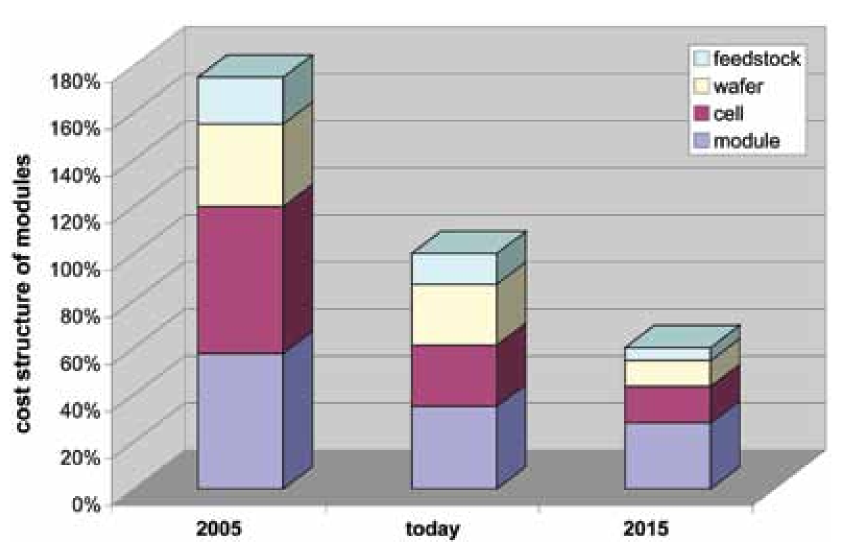

Figure 1. Past, present and prediction of the cost structure of crystalline silicon modules broken down according to the different parts of the value chain. The module manufacturing costs have been calculated relative to today's module manufacturing costs.

Thinner and larger solar cells

Mechanical considerations

It is clear that wafers need to get thinner. The efficiency of solar cells is only slightly affected when the wafer thickness is reduced from 200µm to 120µm [1], which proves that there is still a lot to be gained in the cost-performance ratio of wafers and cells. The wafer manufacturer's aim is to produce as many wafers as possible per kilogramme of silicon. Reducing wafer thickness and reducing kerf losses are two ways in which this can be achieved. In the past five years, wafer thicknesses have dropped from 300µm to 160µm in production, with wafers of a thickness of below 100µm being studied in R&D demonstrations [2-4]. Such extremely thin solar cells have to be fabricated in alternative ways. For instance, a full-size aluminium rear-side is no longer possible as it leads to excessive bowing of cells. Also, aluminium no longer provides adequate passivation for high-efficiency solar cell concepts, which has resulted in several research routes towards open-rear side cell concepts [5]. Improved passivation will lead to a higher current, but will be somewhat compensated by additional resistive losses from the rear side. The net result is a higher cell efficiency and a cell with low-bow properties.

The combination of thin and highly efficient cells poses problems for the interconnection process. More efficient cells produce higher currents, which means that wider and/or thicker interconnects, better known as tabs, are necessary to keep electrical losses at an acceptably low level. However, when exposed to high temperatures (>250°C) during the solder process, thin cells tend to break much more easily. This is caused by differences in the thermal expansion coefficient between silicon and the copper tabs. In addition, substituting lead in solder pastes will lead to an additional increase in process temperature of 40-50°C. This will obviously lead to further yield problems during module manufacturing. During field operation, the temperature cycles seen by the interconnection will result in damage to the silicon. The interconnection will result in (micro-) cracking of silicon and eventually pull-out of silicon from the cell, leading to a decrease in module efficiency and ultimately failure. Alternatively, cracks can develop in the solder itself resulting in an increase in electrical resistance through the interconnection [6].

Figure 2. Picture of a open rear-side solar cell. The rear-side is shown on the left and the front side on the right.

Low-stress interconnection technologies have been developed based on conductive adhesives in order to facilitate the manufacture of modules using thin cells with a large surface area [4]. The lower processing temperature of these adhesives, as compared to soldering, results in a lower residual stress after cooling to room temperature. Adhesives can be formulated to be snap-cured which results in a processing speed that is comparable to the time necessary for making soldered interconnections. The greater elasticity of interconnections made with conductive adhesive and a lower processing temperature as compared with soldering has proven to be functional on cells with a thickness of 100µm. The durability of the interconnection was tested in full-size modules according to IEC61215 standards and has been found to be as suitable as for soldered modules using similar cells. Conductive adhesives also have the advantage over traditional solders of being lead-free.

Electrical considerations

With the exception of a few high-efficiency concepts that are based on monocrystalline silicon Cz wafers, most solar cells are designed and manufactured as vertical devices. This means that the emitter is located on one side of the cell and the base on the opposite side. Metal structures are applied to both sides of the cell to form base and emitter terminals and to drain the current off in a lateral way to facilitate interconnection of neighbouring cells. The front-side metal structure of a cell is designed as a set of fingers and busbars. The fingers are needed to collect the current, but also cause shading. Therefore, the front-grid design is the result of optimization between shading losses and resistive losses.

> "Applying metallization to a solar cell is roughly two orders of magnitude more expensive than using metal foils in a module."

Electrical losses caused by series resistance of the front-grid metallization are typically in the range of several percent. Electrical losses due to rear-side metallization are generally very low for cells with a full-size aluminium rear side. In a module, resistive losses due to interconnection of cells, known as tabbing and bussing, can add up to several percent. As a net result, industrial cells with full aluminium rear side typically leave the cell manufacturing company with 77-79% fill factor, while the module fill factor is typically in the range of 72-74%. Hence, it is worthwhile looking into combined cell-module concepts for lowering these resistive losses. Lowering ohmic losses in solar cells is not straightforward, and will lead to additional costs [7].

Electrical conductors can be applied to the solar cell via printing or plating technologies, or can be applied in the module by metal tabs or foils. Applying metallization to a solar cell is roughly two orders of magnitude more expensive than using metal foils. Therefore it is our strategy to reduce the resistive losses at the module level, not at the cell level.

Figure 3. Picture of the front-side (left) and rear-side (right) of an ASPIRE MWT solar cell. The front-side design is registered as the industrial design Sunweb and owned by Solland Solar Energy Holding BV. The open rear-side design follows from an optimization between passivation requirements and resistive losses.

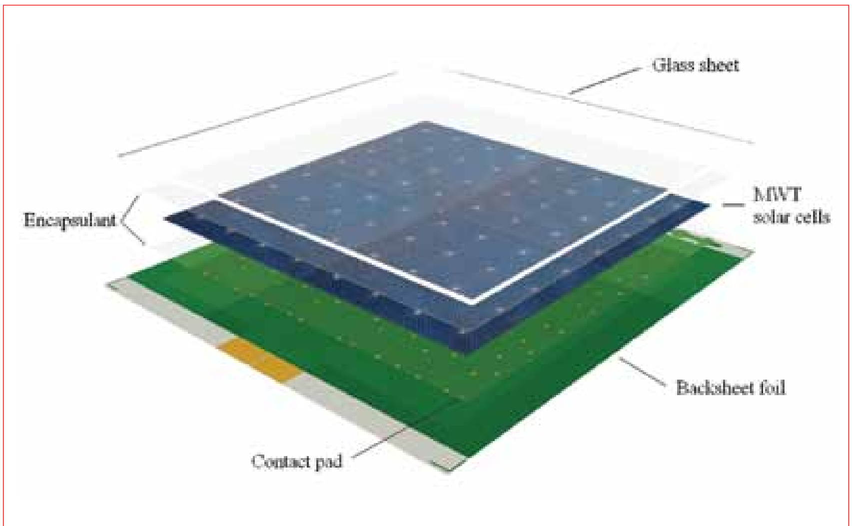

Figure 4. Back-contact module assembly using MWT solar cells.

The module concept is based on draining the current underneath the cell at multiple locations, for example as shown in Fig. 3. The solar cell design is a metal-wrap through (MWT) cell with open rear side. The front-side metallization pattern has been optimized to minimize shading and resistance losses. The front-side metal coverage is typically 2% less in comparison with conventional cells, leading to 2% higher currents. Busbars are no longer necessary because the current is drained through 16 holes in the wafer and appear as 16 contact points on the rear side of the solar cell. Resistive losses due to front-side metallization are also smaller in comparison with conventional solar cells because the effective finger length is smaller. The rear-side design is the result of a trade-off between passivation and resistive losses, i.e., metal coverage. The net result is a premium cell efficiency and a cell concept that has the mechanical properties to survive the subsequent module processing steps.

Back-contact module concept

In order to fully benefit from the advantages of back-contact cells such as MWT cells, an alternative module manufacturing technology is required. At ECN, a method using a patterned conductive back-sheet foil as the module substrate was developed. The foil is similar to a standard Tedlar-PET-Tedlar back-sheet foil with an additional layer consisting of a metal sheet. The conductive sheet is patterned to match the contact points on the rear of the back-contact cell, resulting in a series interconnection of the cells on the foil. Cells are placed on the foil using a method analogous with pick-and-place technology used for surface-mount devices in the electronics industry. This reduces cell handling to just one pick-and-place step and therefore reduces the likelihood of damaging the cells. Since the front contacts and tabs are no longer required, the cells can be placed closer together in the module, which leads to an improved packing density. There is also no need for string interconnections at the top and bottom of the module, which also increases the effective area of the module. The cell-to-cell interconnection takes place during lamination, resulting in a single-shot interconnection and lamination technology.

The temperatures at which the connections are established are identical to the lamination temperature of approximately 150ºC. An electrically conductive adhesive that is cured during lamination establishes the electrical connections between the MWT cells and the conductive back-sheet foil, as shown in Fig. 5.

Since shadowing losses no longer play a role, the metal layer in the back-sheet foil can be designed to be much wider than the width of a busbar in conventional cells. The cell design and module layout can be optimized simultaneously with respect to module output and total costs. For example, the number of contacts between the rear of the cell and the conductive components of the module can be optimized for both cell and module efficiency. An important parameter that affects module performance is thickness of the conductive layer. The costs of the metal sheet, e.g., copper and the processes used to create the specific design pattern, will increase with increasing layer thickness. Likewise, the resistive losses in the module will reduce with increasing layer thickness. This will lead to an economic optimum. An example of module fill factor calculations based on an MWT cell with a fill factor of 77.0% is shown in Fig. 6. When the thickness of the copper layer increases, the fill factor of the module starts approaching the fill factor of the MWT cell, for which several data points were verified by measurements. In comparison with conventional modules, module fill factors will be significantly higher. Several side-by-side comparisons on neighbouring wafers, cells and modules have been performed [9], showing consistently that MWT modules produce 2% more output current and module fill factors are 3% higher than modules fabricated with H-pattern cells.

Pilot line for manufacturing back-contact modules

Fig. 7 shows the pilot line for assembling back-contact modules [10], which was developed together with Eurotron [11]. This assembly line consists of five stations performing the following steps. **Station 1**: Patterned conductive foil is placed on a carrier plate that transports the foil through the module build process. The foil is held in place by vacuum support. **Station 2**: The conductive adhesive is printed on the foil. The complete foil is printed in less than 60 seconds. A 60-cell module requires about 2000 dots of conductive adhesive to be printed. **Station 3**: The first sheet of encapsulant needs to be perforated at the positions where the conductive adhesive has been printed to allow contact with the cells. This station can perforate and place a complete encapsulant sheet in less than one minute. The foil is then automatically placed over the conductive foil without damaging or smearing the conductive adhesive dots. **Station 4**: Cells are individually picked from a stack by a robot and placed at pre-programmed positions on foil with the contacts on the cell making contact with the conductive adhesive (Fig. 8). A vision system checks the integrity of the cell and its orientation. The module assembly is then returned to Station 3 for a second sheet of encapsulant (without holes) and a sheet of glass. In a production line, additional in-line stations would be included for these operations. **Station 5**: For the lamination process, the glass sheet needs to be at the bottom of the module stack. A conveyer belt attached to a pneumatic arm is used to invert the carrier with the module stack in place. The module is then fed out of the pilot line to be placed into the laminator. Lamination is subsequently performed to create the monolithic module, during which process both the encapsulant and the conductive adhesive are cured.

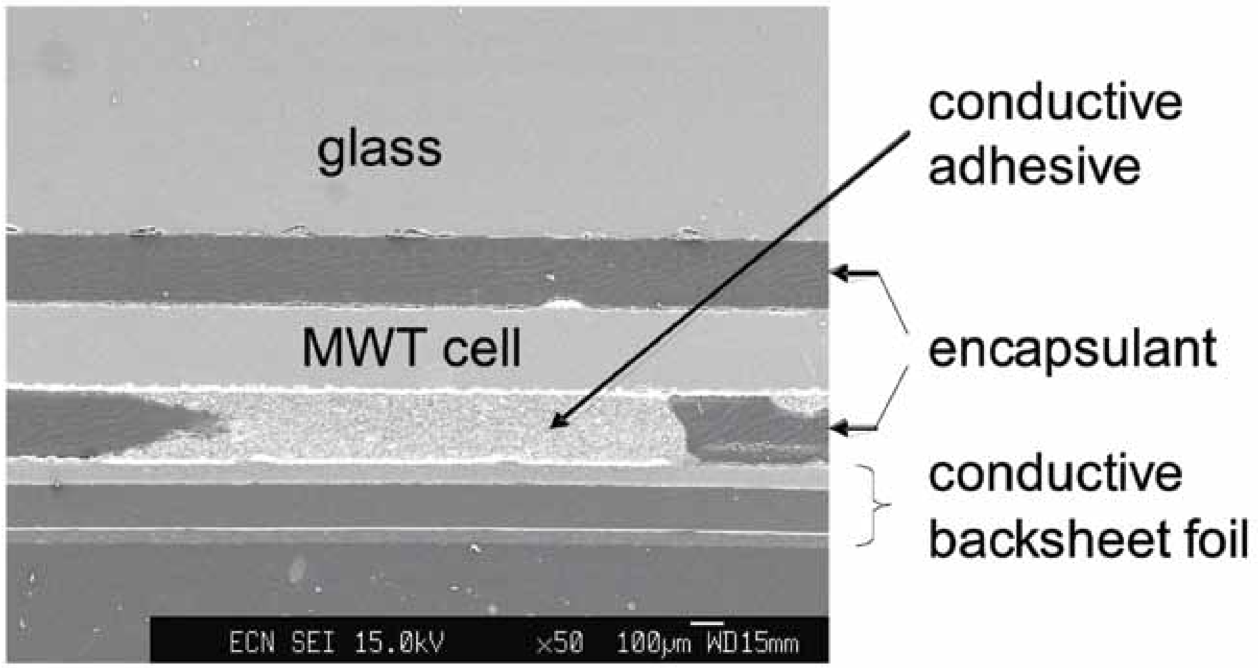

Figure 5. Cross-sectional view of the module.

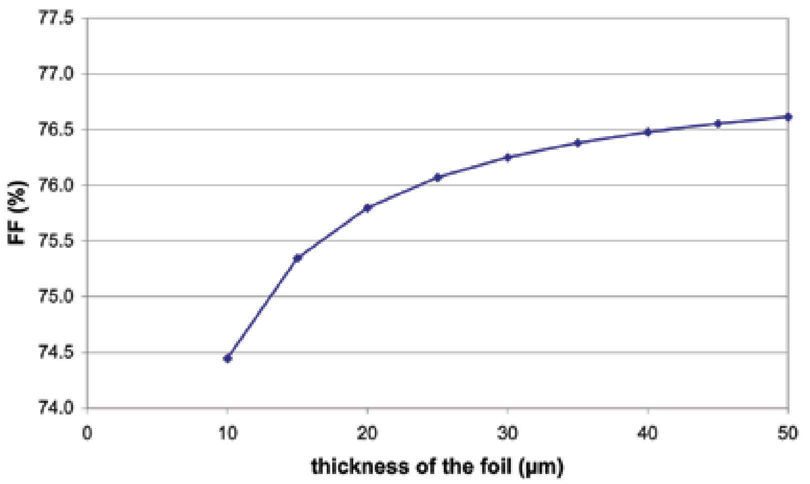

Figure 6. Results of fill factor calculations of the MWT module as a function of copper layer thickness in the back-sheet foil.

Figure 7. Picture of the pilot line at ECN for manufacturing back-contact modules.

Further automation can be implemented in production, such as automatic feed-in of materials. A production line will also be fitted with a number of carriers with a return system taking a carrier back to the start of the line after module build-up is complete. A production line has a potential throughput rate of one module well within a minute for 60 cell modules, which is equivalent to 150MWp using 16% solar cells.

Premium efficiency MWT modules

As a demonstration of the capabilities of MWT cells and modules, we recently manufactured high-efficiency MWT cells and modules in 2009. High-quality multicrystalline wafers with a thickness of 160μm were obtained from REC. Several improvements in texturization, emitter formation and metallization were implemented. A batch of 80 wafers was used to result in an average cell efficiency of 17.6%, of which the best 36 cells had an average efficiency of 17.8% with a highest efficiency of 17.9%.

The 36 best cells were used to manufacture a module with the pilot line at ECN. Improvements in processing of the module were made to ensure improved deposition of conductive adhesive and better settings for combined lamination and curing. The performance of the finished module was measured at ECN and this measurement was confirmed by measurement at JRC-ESTI. Aperture area efficiency was 17.0%. The processes used for manufacture of the cells and ultimately the module are industrially applicable and not restricted to the laboratory.

Figure 8. Close-up view of the pick-and-place robots.

	I_{SC} (A)	V_{OC} (V)	FF (-)	Efficiency (%)
Premium cell	8.86	0.632	77.8	17.9
Average 36 cells before encapsulation	8.85	0.631	77.4	17.8
Module (aperture area = 8885cm^2)	8.86	22.67	75.0	**17.0**

Table 1. Overview of premium cell and module efficiencies achieved in 2009. Cell efficiencies were measured with a class A solar simulator at ECN; module efficiency was independently verified by JRC-ESTI.

Outlook and conclusions

The single-shot interconnection and encapsulation process proves an effective route towards reduction of the cost-performance ratio of crystalline silicon modules. Two main questions remain, however. The potential for module performance increase is definitely there, but how about the manufacturing costs of this module technology? The second is whether this technology will survive the required 20-25 years' operation in the field. Clearly, the back-contact module assembly method is ideal for working with very thin silicon wafers. This means that the costs targets for 2015 for feedstock and wafers (Fig. 1) seem to be very well within range. Furthermore, the cell cost and efficiency targets seem to be in range. Material costs in the cell will be reduced when transforming existing cell production lines from conventional H-pattern cells to MWT cells, while efficiencies increase. Applying MWT cell strategies to monocrystalline wafers will further reduce the gap towards the 20% target. But at the module level, there are still some items to be resolved. Conductive back-sheet foils will be more expensive than standard TPT foils, and conductive adhesive is also an additional cost item. At present there is no commercial party producing conductive back-sheet foils in high volume. However,

Figure 9. Picture of the finished MWT module. All of the conductive back-sheet is within the active area of the cells. There is no need for bussing at the top and bottom of the module resulting in optimum packing density.

following the line of reasoning that the ultimate limit of what can be achieved by upscaling will be determined by the material costs, the conductive back-sheet foil will eventually be not much more costly than a TPT foil. Therefore, we believe that it is more important to show that the lifetime expectancy of the back-contact module concept is at least as good as conventional module technology. This is where our present focus is, and laboratory tests have so far shown to give very promising results.

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