The solar cell wafering process

Mark Schumann, **Teresa Orellana Pérez** & **Stephan Riepe**, Fraunhofer Institute for Solar Energy Systems (ISE) Freiburg, Germany

This paper first appeared in the fifth print edition of *Photovoltaics International* journal.

ABSTRACT

The process of wafering silicon bricks represents about 22% of the entire production cost of crystalline silicon solar cells. In this paper, the basic principles and challenges of the wafering process are discussed. The multi-wire sawing technique used to manufacture wafers for crystalline silicon solar cells, with the reduction of kerf loss currently representing about 50% of the silicon, presents a major challenge for further research efforts. Another relevant field of research is the reduction of wafer thickness in order to obtain more wafers per millimetre of brick length. The last subject that is addressed in this paper is the general optimization of the wafer surface and geometry, as the multi-wire saw cutting process influences the mechanical properties of the wafers and can have further effects on subsequent process steps.

Motivation

Crystalline silicon is currently the principal material used to manufacture solar cells, and is likely to remain so for the foreseeable future. Thus, it is of utmost importance to improve the currently available process technologies in order to lower the overall costs for silicon solar cells. In this paper we focus on the wafering process, as it has a comparatively large cost contribution of about 22% in the silicon solar cell manufacturing value chain [1].

Fig. 1 summarizes the process steps that form the front-end of the solar cell value chain. The silicon feedstock material is crystallized as either monocrystalline or multicrystalline ingots by various methods. These ingots are then cut into bricks with the footprint area of the silicon wafers. The bricks are mechanically or chemically ground and polished, a process that has been introduced to improve the edge quality on the final wafers and reduce the breakage rate in the subsequent cell processing steps. A multi-wire saw is used to cut the silicon brick into wafers independent of its crystalline structure. Finally, the wafers are cleaned and guided to the next production steps to become solar cells and photovoltaic modules.

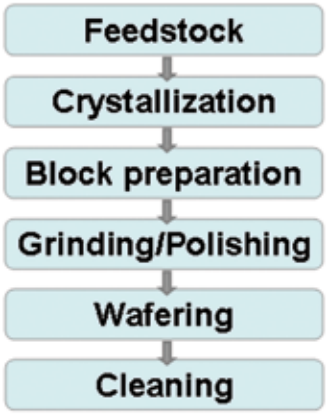

Figure 1. Process steps from silicon chunks to clean silicon wafers.

In order to intensify its activities in front-end processes, Fraunhofer ISE founded the Silicon Materials Technology and Evaluation Center (SIMTEC) as a research laboratory within ISE in Freiburg in 2008.

> "The most important motivation for research is the fact that during cutting, about 50% of the expensive solar-grade silicon is lost as kerf."

The following section will focus on the research activities in the field of multi-wire sawing justified by the potential cost reduction in this process. The most important motivation for research is the fact that during cutting, about 50% of the expensive solar-grade silicon is lost as kerf. Another relevant field of research is the reduction of the wafer thickness in order to produce more wafers per kilogram silicon.

Finally, the wafering process step, in combination with the material quality, defines the mechanical properties of the final solar cell, as the wafering process can damage the wafer's surface. This damage has to be etched not only to increase the mechanical stability but also to obtain good cell efficiencies.

Principle of wafering

Fig. 2 shows a schematic of a multi-wire saw. A wire is taken from a delivery spool and guided by rolls/pulleys that are in place to give the wire the desired tension. From these rolls the wire is led to the wire guidance rolls, which are coated with a polymer and feature grooves with defined spaces, commonly known as 'pitch'. The wire is wound as many times as there are grooves on the wire guidance roll, and at the last groove point, the wire is again guided by pulleys to a collector spool.

The wire on the wire guidance rolls forms the so-called wire web, i.e., many segments of the wire are laid parallel to each other, as shown in Fig. 2. The silicon brick is glued on a glass plate before being cut. This glass plate is glued on a metal holder placed above the wire web. During the cutting process, the silicon brick is pushed towards the wire. A slurry is homogenously applied to the wire web via a nozzle. The slurry performs the cutting process on the wire web and consists of silicon carbide (SiC) particles in a solution with polyethylene glycol (PEG).

The silicon carbide particles indent the silicon surface as the wire's movement drags them. Fig. 3 shows an illustration of the cutting process in one sawing channel. The slurry is recollected and driven back in the slurry circuit. By this process, all the wire segments are wetted and form many sawing channels in the silicon brick.

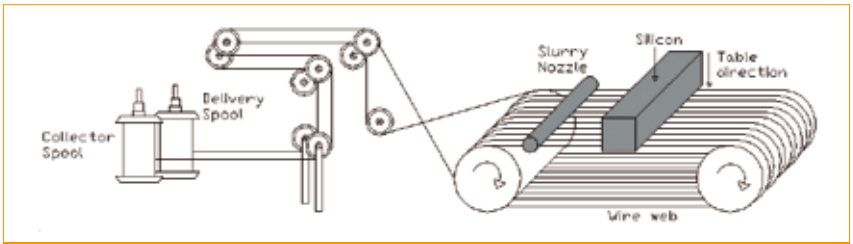

Figure 2. Schematic drawing of multi-wire saw. For industrial use, up to two silicon bricks can be cut in parallel or on the upper and lower part of the web.

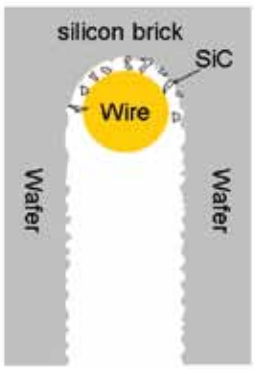

Figure 3. Schematic illustration of the cutting process in one sawing channel. Silicon carbide particles, dragged by the motion of the wire, indent the silicon surface, thus enabling the cutting of a silicon brick into hundreds of wafers.

Figure 4. A silicon brick after the cutting process showing the wire web in the foreground of the photo. The glue on the wafers causes them to stick to the glass plate.

At the end of the cutting process, the wafers are hanging on the glass plate which has been partially cut and is only used once (see Fig. 4). The glue is dissolved in order to remove the wafers from the glass plate.

The following sections discuss some important parameters of the cutting process in more detail.

Wire

Multi-wire sawing uses a brass-coating steel wire. The tensile strength of the wire is approximately 4000N/mm^2 and the standard thickness is between 120 and 140µm for photovoltaic applications. In experimental research wires as thin as 100µm have being tested [2].

Fig. 5 shows a 120µm wire before (left) and after the cutting process (right). Before cutting, the wire has a smooth surface, while after the cut the brass coat is removed, the surface is rougher and scratches occur. The wire is also slightly thinner, leading one to conclude that iron and brass from the wire have been transferred into the slurry. Most of the removed wire material is composed of iron, since the brass coat has a thickness of only a few hundred nanometres. After the cutting process, slurry can also stick to the wafers. Consequently, it is very important to clean the wafers carefully in order to remove the iron, which could cause problems in the subsequent cell processing.

Slurry

Silicon carbide with a defined grain size is the abrasive used. The grain size distributions used for silicon carbide are defined by the FEPA [2]; F600, which has a mean grain size of 9.3µm, is considered the standard grain size. Kerf reduction can be achieved using smaller grains.

SiC particles indent the silicon material and damage the wafer surfaces. This damaged layer has to be removed, which is usually done by wet chemical etching [4]. To reduce the thickness of this layer, experiments with smaller grain size distributions have been performed, resulting in significant improvements [2].

Two different polyethylene glycols, PEG 200 or PEG 300, are commonly used as

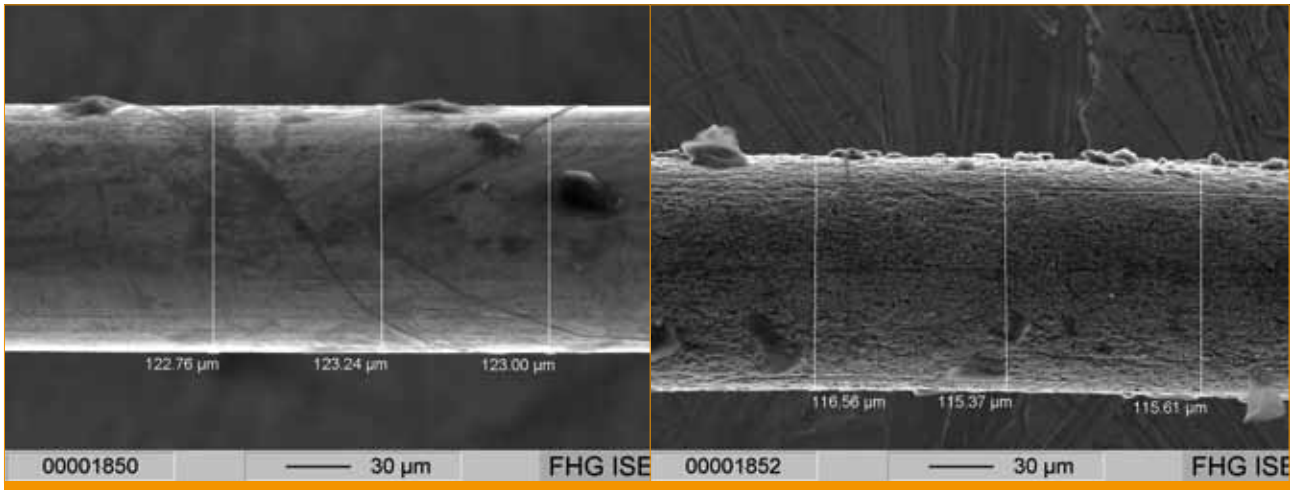

Figure 5. SEM images of a wire of 120µm diameter before (left) and after (right) the cutting process. The post-cutting wire shows some SiC particles on the surface and is scratched and rough in appearance.

carrier fluids. Different carrier fluids, e.g. water, have been investigated by some research groups [5], but PEG remains the dominant carrier fluid.

Another approach for advancing the multi-wire sawing process is the omission of slurry, which is only possible if wires with fixed abrasives are used. For this purpose, diamond wire with small diamond particles attached to the wire is mainly used. Successful cutting has been reported [6]; however, the high price of this type of wire has hindered a wider acceptance of this method for photovoltaic applications.

Machine parameters

The machine parameters for the cutting process depend on many factors such as wire thickness, machine type, wafer thickness, brick length and grain size, among others. The machine parameters that must be chosen are the table and wire speed, the tension of the wire and the flow and temperature of the slurry.

While slurry flow (4000kg/h used at SIMTEC) and slurry temperature (25°C) for standard cuts remain almost always constant, other parameters can vary. The wire tension depends on the chosen wire thickness. For example, the tension for a 140µm wire at SIMTEC is 27N while for a 120µm wire the tension is 22N. The table speed (the velocity under which the silicon moves into the wire web) ranges between 0.3mm/min and 0.5mm/min.

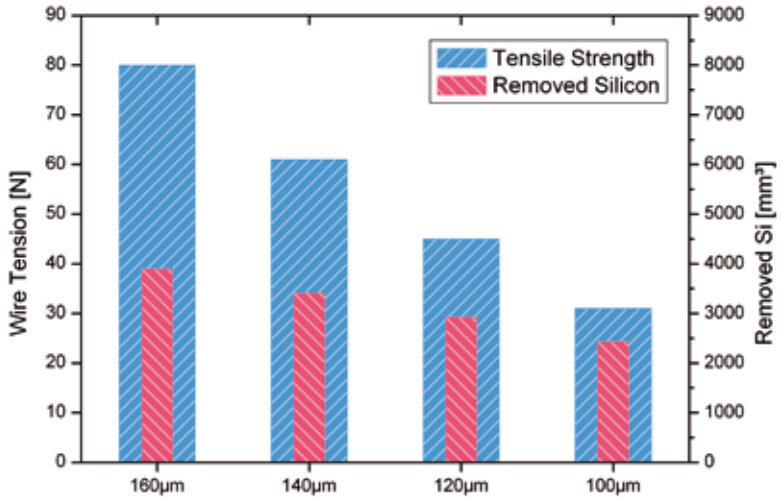

Figure 6. The graph shows the possible wire tension for different wires and the amount of silicon that is removed per kerf for different wire diameters.

This results in a cutting duration between five and eight hours for a silicon block with a 156 x 156mm^2 footprint. The velocity with which the wire moves from one spool to the other is between 720m/min and 900m/min; hence the necessary wire length for one single cut can be more than 400km.

The setup of the machine as well as the chosen material has an influence on the resulting cutting parameters, which include the viscosity of the slurry, the temperature of the silicon and the bow of the wire. In-depth descriptions of these parameters can be found in the relevant literature [7,8].

Wafering problems and solutions

Kerf

Even though efforts have been made to recycle lost silicon, there has been no

established industrial standard process until recently [9]. While the silicon carbide particles are routinely recycled, the reduction of the kerf loss remains an important topic for research. The link between the kerf (which is approximately represented by the sum of double the grain size and the wire thickness) and the resulting wafer thickness can be expressed as illustrated in Equation 1.

Wafer thickness = Pitch – (Wire thickness + 2x Grain size of the SiC) Eq. 1

Potential methods of achieving a kerf reduction are to use either thinner wire and/or smaller abrasive grain sizes. Both approaches are being investigated at SIMTEC.

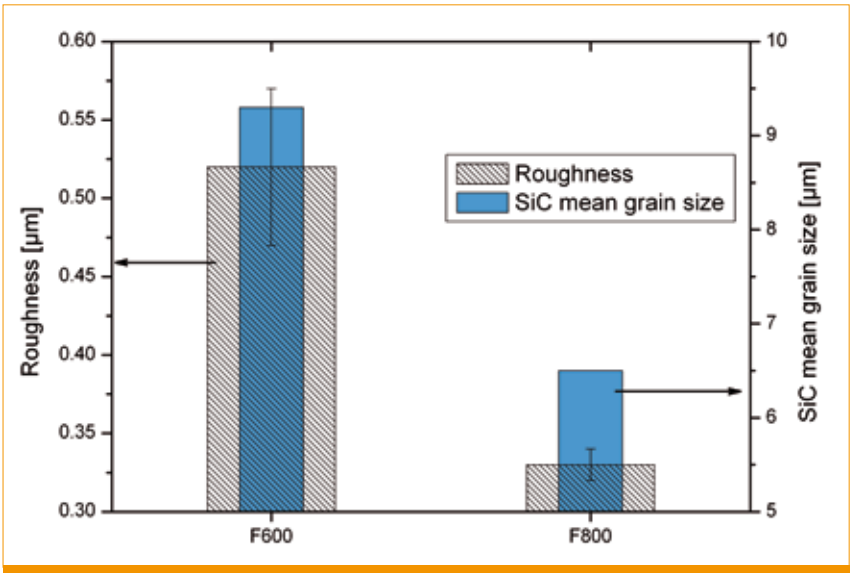

Figure 7. Mean grain size for two different SiC types and resulting wafer roughness.

"While the silicon carbide particles are routinely recycled, the reduction of the kerf loss remains an important topic for research."

Wire thickness

Wire thickness is the most obvious option for kerf reduction. A wire thickness of 160µm was standard in the photovoltaics industry until 2007. In order to reduce the cost for silicon photovoltaics, this thickness has since been decreased to 100µm. This represents a kerf reduction of about 37%, which is equivalent to about 13kg of silicon considering a standard industrial wafer size of 156 x 156mm^2.

Reducing the wire thickness is a straightforward process but only to a certain degree. The disadvantage of reducing the wire thickness is the restriction to lower wire tensions to ensure cutting without wire breakage. In Fig. 6, the wire tension of four different wires is compared with removed silicon per kerf for a 156 x 156mm^2 brick.

Thinner wires also experience a larger percentage decrease in tensile strength due to the erosion of the wire surface caused by the indentation of the SiC, because the removal is independent of the wire's thickness. Some improvements on wire have been carried out recently, mostly with regard to tensile strength of the steel. To further reduce wire thickness, it will be necessary to increase the tensile strength even further. Another possibility is to find alternative materials that could serve as a substitute for steel in this application.

"The disadvantage of reducing the wire thickness is the restriction to lower wire tensions to ensure cutting without wire breakage."

Grain size

Equation 1 shows that another method for kerf reduction is changing the grain size of the abrasive. This has a smaller impact on the kerf due to the used grain size distributions. Currently, a common

Figure 8. Photo of a 70µm multi-crystalline wafer, which demonstrates the flexibility of thin wafers.

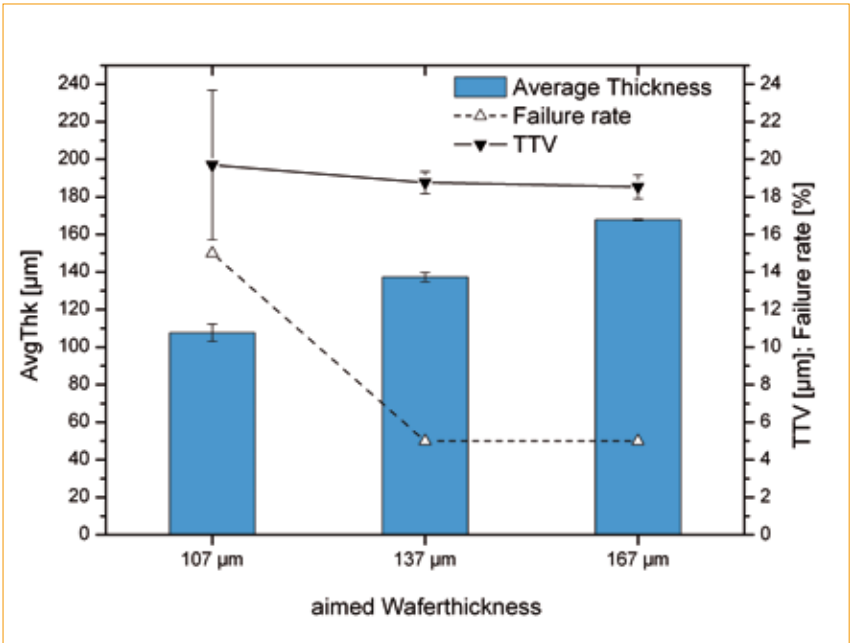

Figure 9. Wafer geometry parameters (AvgThk = average thickness; TTV = total thickness variation) and failure rate for wafers of different thicknesses.

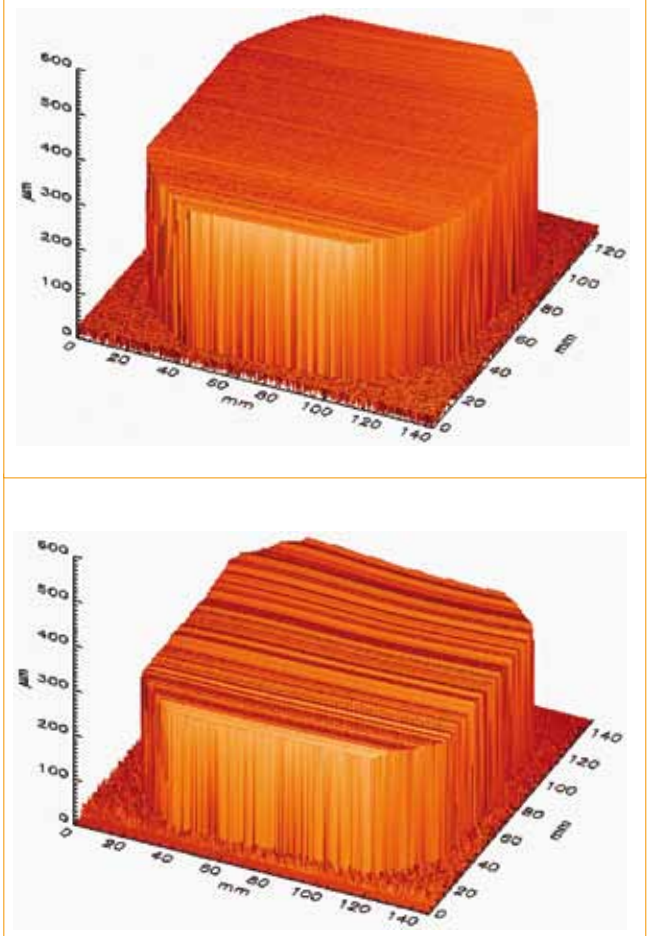

Figure 10. Different wafer surfaces measured with a surface profilometer. Cutting parameters have a strong influence on the resulting wafer surface.

grain size distribution is F600, with a mean grain size of 9.3µm. If this is changed to F800 with mean grain size of 6.5µm, the kerf will be reduced by about 10µm. In calculating the kerf, it must be taken into account that particles larger than the mean grain size also exist. These larger particles are important during the cutting process and are the reason why the kerf caused by the SiC is higher than twice the mean grain size [11]. Another advantage of smaller grain size distribution is that the surface roughness is reduced (see Fig. 7).

Wafer thickness

Another option to get more wafers per millimetre brick length is to cut thinner wafers, an area that has been the focus of quite a large amount of research. Throughout the last five years, the industry has seen a decrease in wafer thickness from 325µm down to 200µm or, in some cases, even as narrow as 180µm. Another advantage of thinner wafers is their improved flexibility; however, this improvement is only a feature of wafers thinner than 130µm, which have low values of breaking strength (see Fig. 8).

Fig. 9 shows the results of an experiment where wafers of three different thicknesses were cut. The thinnest wafers had an average thickness of 107µm, while the thickest wafer was 167µm. As the graph shows, the failure rate decreases with increasing wafer thickness, which was expected due to the reduced breaking strength of thinner wafers. The medium value of the total thickness variation (TTV) increases only slightly for thinner wafers but shows a much larger spread. Thinner wafers inflict less force on the wire, which allows the wire to move more freely in the sawing channel, resulting in an increased TTV. However, this feature could only be seen for the thinnest wafers, and no trend was apparent in this case.

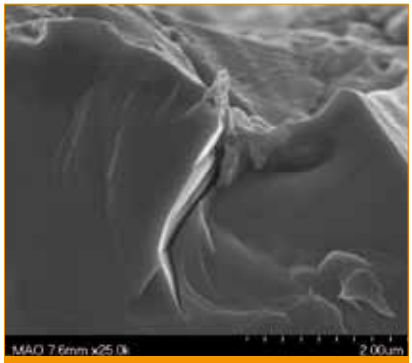

Figure 11. Groove on the surface of a monocrystalline silicon wafer featuring a micro-crack developed under the groove due to the indentation of a silicon carbide particle during multi-wire sawing.

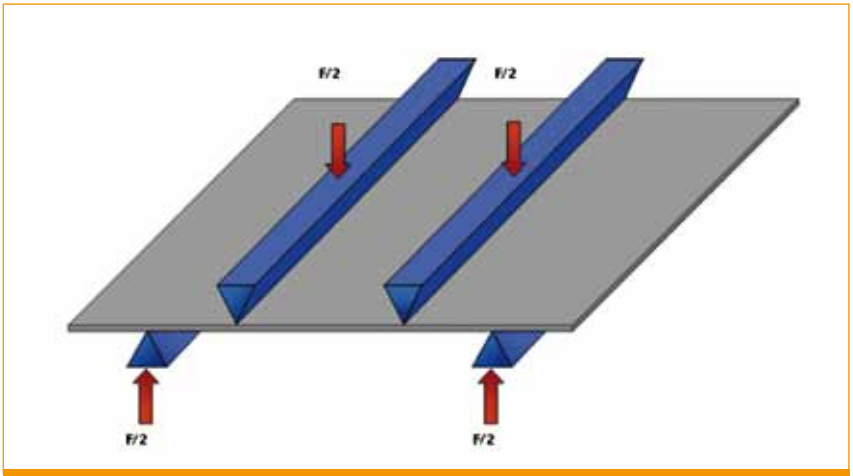

Figure 12. 4-line bending test scheme for testing cracks on the wafer surface and at the edges [1].

Wafer quality

Fig. 3 clearly shows how the cutting process's indenting abrasive has a strong influence on the surface quality of the wafers. The main mechanical properties influenced by the sawing process are wafer surface and geometry.

In the photovoltaics industry, cost is a preventative factor in the decision not to grind and polish wafers to obtain desired wafer geometry. Therefore, as-cut wafers already must fulfil the necessary wafer geometry after multi-wire sawing and should adhere to controlled parameters – like those followed at SIMTEC – such as thickness, total thickness variation and bow.

Fig. 10 shows as-cut wafers cut with different parameters. Obviously, the chosen cutting parameters have a large influence on the wafers' roughness. Furthermore, wafering not only causes surface roughness but also damage below the surface, referred to as sub-surface damage [12]. Much research has gone into eliminating all damage; as a rule, a damaged wafer will lead to a poorly performing solar cell. However, sub-surface damage has yet to be decreased to sufficiently low levels. Today its removal still demands a step involving a wet chemical process.

Mechanical properties

Sub-surface damage has a huge effect on the mechanical stability of the wafers. The indentation of abrasive SiC particles in the silicon crystal yield a distinct pattern on the wafer's surface as well as the sub-surface layer a few microns deep where the presence of micro-cracks is dominant (see Fig. 11) [13].

Silicon wafers behave as brittle materials at room temperature and are thus very sensitive to defects. Under loading conditions, any mechanical stress applied to the silicon wafer is intensified at the cracks' tips. Given that cracks are expected on the surface and at the edges of the wafers (due to the multi-wire saw cutting), the 4-line bending test (see Fig. 12) can be selected to characterize the mechanical properties of the wafers [14].

The probability of failure of a wafer is a function of the stress level, distribution of micro-cracks and volume of silicon subjected to stress. Weibull statistics analytically describe the dependency of fracture probability on these factors.

$$S(\sigma) = 1 - \exp\left(-V_E\left(\frac{\sigma}{\sigma_0}\right)^m\right)$$

Eq. 2

The parameter m in Equation 2 is the Weibull modulus and describes the width of the distribution of crack lengths. A high m-value means that the crack lengths and thus the failure stresses are within a narrow scattering band and vice versa. σ is the applied load on the wafer and σ_0 is the fracture strength of the wafers, usually given as the load level at which 63% of the tested wafers have failed. Finally, V_E is the effective loaded volume.

Weibull parameters m, σ_0 and V_E are estimated by the least square fitting of a linearized form of the Weibull distribution [15].

Weibull graphs plotting the probability of wafer breakage against the applied stress are depicted in Fig. 13. A significant increase in mechanical resistance can be observed for silicon wafers when the micro-cracks on

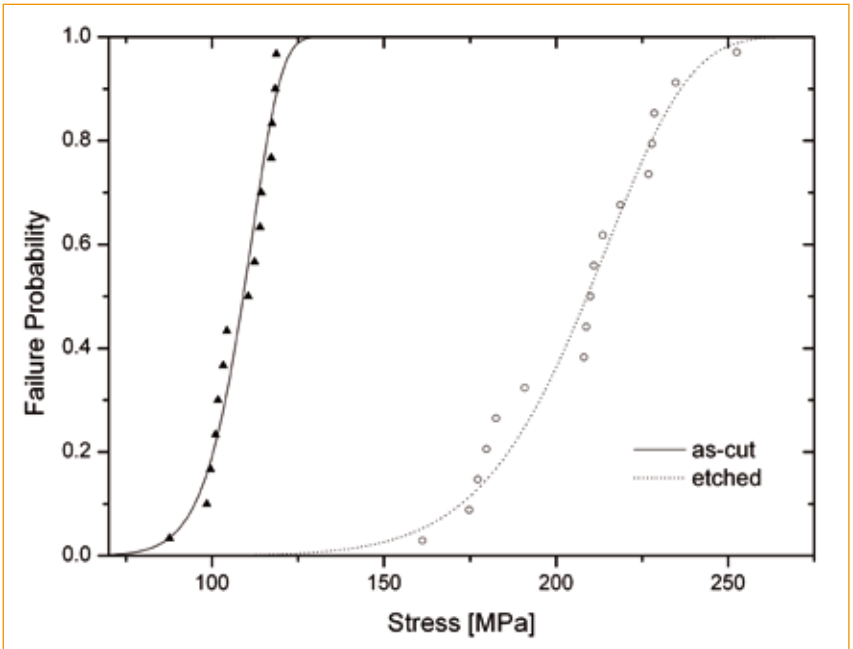

Figure 13. A Weibull graph shows the failure probability versus bending stress applied during the 4-line bending test of two sets of monocrystalline silicon wafers. The black triangles correspond to the experimental data obtained with as-cut wafers; the open circles guide the (dotted) line representing the experimental data obtained with alkaline etched wafers. The continuous line represents the Weibull functions best fitting the experimental data.

their surface and at the wafer edges are removed by a standard alkaline etching solution. An experiment taking 17 wafers per group gave a characteristic stress of 112Mpa for as-cut wafers, while etched wafers had a characteristic stress of 217MPa. These results highlight the importance of a micro-crack-free wafer surface for providing the most stress-resistant wafers.

Summary

Wire sawing will remain the dominant method of producing crystalline wafers for solar cells, at least for the near future. Recent research efforts have kept their focus on reducing the wafer thickness and kerf, with both approaches aiming to produce the same amount of solar cells with less silicon material usage. There have been successful outcomes in the recent past: where kerf reductions of close to 50% have been achieved using smaller-grained abrasive particles and thinner wires. Wafers with a thickness of 100µm have been cut and processed to solar cells.

The wire saw wafering process is determined by a variety of factors. In order to optimize the wafering process, a large number of tests are necessary; Those presented in this paper illustrate that multi-crystalline wafers can be cut with a thickness down to 70µm while maintaining high quality.

In the future, the multi-wire sawing technique will be further optimized, but alternatives to the wafering process need to be investigated. Although some new promising alternatives have been introduced recently, all of them have yet to prove their industrial feasibility and relevance.

Acknowledgements

The authors would like to thank **Matthias Singh**, **Markus Bergmann** and **Fridolin Haas** and all other former colleagues for their invaluable efforts developing wire sawing at Fraunhofer ISE.

The authors would also like to thank the **German Federal Ministry for the Environment Nature Conservation and Nuclear Safety** (BMU) for funding (contract No. 0327601E).

References

[1] Kreutzmann, A. & Schmela, M. 2008, "Emancipation from Subsidy programs", *Photon International*, Vol. 12, pp. 84-92.

[2] Weber, B., Bierwisch C, Kübler, R. & Kleer, G. 2008, "Investigation on the Sawing of Solar Silicon by Application of Wires of 100µm Diameter", *Proceedings of the 23rd European PVSEC*, pp. 1285-1288.

[3] *Shapes and Dimensions for Precision Superabrasives*. FEPA Standard 2006, 42-2.

[4] Mayer, K., Kray, D., Orellana, T., Schumann, M., Glunz, S. 2008, "New Surfactants for Combined Cleaning and Texturing of Mono-Crystalline Wafers after Wire-Sawing", *Proceedings of the 23rd European PVSEC*, pp. 1109-1113.

[5] Anspach, O., Stabel, A., Lawrenz, A., Riesner, S., Porytskyy, R. & Schulze, F.W. 2008, "Investigations on Single Wire Cuts in Silicon", *Proceedings of the 23rd European PVSEC*, pp. 1098-1103.

[6] Kray, D., Schumann, M., Eyer, A., Willeke, G.P., Kübler. R., Beinert, J. & Kleer, G. 2006, "Solar Wafer Slicing with Loose and Fixed Grains", *Proceedings of the 4th World WCPEC*, pp. 948-951.

[7] Rietzschel, R., Wagner, T., Funke, C. & Möller, H.J. 2008, "Optimization of the Wire Sawing Process using Force- and Temperature Measurements", *Proceedings of the 23rd European PVSEC*, pp. 1301-1304.

[8] Nasch, P.M. & Schneeberger, S. 2005, "A Theoretical Modelling of Consumables Usage as a Tool for Cost Reduction in silicon Wafering using Multi-Wire Slurry Saw", *Proceedings of the 20th European PVSEC*, pp.1139-1144.

[9] Wang, T.Y., Lin, Y.C., Tai, C.Y., Fei, C.C., Tseng, M.Y. & Lan, C.W. 2009, "Recovery of Silicon from Kerf Loss Slurry Waste for Photovoltaic Applications", *Progress in Photovoltaics: Research and Applications*, Vol. 17, pp. 155-163.

[10] Kray, D., Schumann, M., Schultz, O., Bergmann, M., Ettle, P., Rentsch, J., Eyer, A., Willeke, G.P. 2006, "Experimental Investigation of Wire Sawing Thin Multicrystalline Wafers", *Proceedings of the 21st European PVSEC*, pp. 885-888.

[11] Beesley, J.G. & Schönholzer, U. 2007, "Slicing 80 Micrometer Wafers-Process Parameters in the Lower Dimensions", *Proceedings of the 22nd European PVSEC*, pp. 956-962.

[12] Hadamovsky, H.F. 1990, "Werkstoffe der Halbleitertechnik", *VEB Deutscher Verlag für Grundstoffindustrie*.

[13] Möller, H.J. 2004, "Basic Mechanisms and Model of Multi-Wire Sawing", *Advanced Engineering Materials*, Vol. 6, No. 7, pp. 502-513.

[14] Behnken, H., Apel, M. & Franke, D. 2003, "Simulation of Mechanical Stress during Bending Tests for Crystalline Wafers", *Proceedings of the 3rd World WCPEC*, pp.1308-1311.

[15] Wachtman, J.B. 1996, *Mechanical Properties of ceramics*. John Wiley & Sons.

About the Authors

Mark Schumann studied process engineering at the University of Applied Sciences, Wildau and received his degree in 2005. His diploma thesis at Fraunhofer ISE was concerned with wire sawing for PV applications. He is currently doing research on wire sawing and writing his Ph.D. thesis.

Teresa Orellana Pérez received her degree in materials engineering from the Polytechnique University of Madrid in June 2008. She has been working on the cleaning of as-cut wafers at Fraunhofer ISE since October 2006, and since February 2009 has been working on a Ph.D. thesis in the field of mechanical characterization of wafers.

Stephan Riepe studied physics at the University of Freiburg and the University of Sydney. He received his Ph.D. degree in 2008 from the University of Constance. He has been working at Fraunhofer ISE for the past nine years in the field of characterization of silicon materials, and is currently leading the crystallization and wafering activities at the SIMTEC laboratory.

Enquiries

Fraunhofer Institute for Solar Energy Systems (ISE)
Heidenhofstrasse 2
79110 Freiburg
Germany

Email: mark.schumann@ise.fraunhofer.de
Website: www.ise.fraunhofer.de