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Ramping a novel cadmium telluride thin-film solar photovoltaic module production process

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ABSTRACT

Thin-film solar photovoltaic technology offers the benefits of low-cost and high-volume production. Yet numerous thin-film PV startups have struggled in their efforts to commercialize complex, expensive production technologies, as production ramps have taken longer than expected, and venture capital and other sources of funding have run dry. This article describes a proprietary cadmium telluride (CdTe) thin-film module production process commercialized by Abound Solar: heated-pocket deposition (HPD) of the semiconductor layer, and the replacement of a traditional lamination process with a novel edge seal. The simple production process has resulted in a fast ramp of module efficiency and throughput. The paper also describes how the process can result in fast throughput, high yields, and low manufacturing and capital equipment costs.

Abound Solar manufactures photovoltaic modules utilizing thin films of cadmium telluride (CdTe) as the main semiconductor layer. The company began in 2007 as AVA Solar with the goal of significantly reducing the cost of solar-generated electricity. The core technologies were developed during 15 years of research and development at Colorado State University (CSU). The efforts focused specifically on developing high-volume production processes with low manufacturing costs.

Automated manufacturing

Abound's advanced production facility is fully automated with production lines laid out in a linear manner to optimize workflow. In order to balance production cycles of all the different tools, equipment within the line 'pull' materials and work-in-progress from the preceding tool. Strategically placed queues help facilitate materials replenishment and minor maintenance, minimizing production disruption. Based on comments from program managers at the U.S. National Renewable Energy Laboratory (NREL), the plant may be one of the most highly automated PV manufacturing facilities in the world.

Figure 2. Automated back-end module assembly tools at the Longmont, Colorado manufacturing facility. These fully-automated systems have a throughput of approximately 65MW per annum.

In order to create a balanced production line, multiple pieces of equipment are used, in parallel, to perform processes with slower cycle times. This balanced production line forms what is referred to as a manufacturing 'cell', which has a nameplate capacity of 65MW, equivalent to a throughput of approximately 900,000 modules per year. Fig. 1 is a block diagram schematic of the manufacturing processes in each cell, while Fig. 2 shows a picture of the back portion of the manufacturing cell from bus car to back-box application tools. Module fabrication time, covering the time it takes to convert the incoming glass sheet to a packaged product ready to ship, is approximately 2.5 hours. The manufacturing cell will be the building block used for the company's upcoming expansion plans.

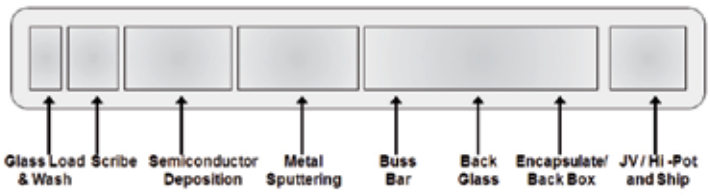

Figure 1. Overview of complete Abound Solar PV module manufacturing process, with glass entering on left and modules crated for shipment on right. The entire line forms one manufacturing cell with approximately 65MW annual capacity. Total product cycle time, end to end, is 2.5 hours.

Technology foundation

Semiconductor processing is the most critical aspect of thin-film PV

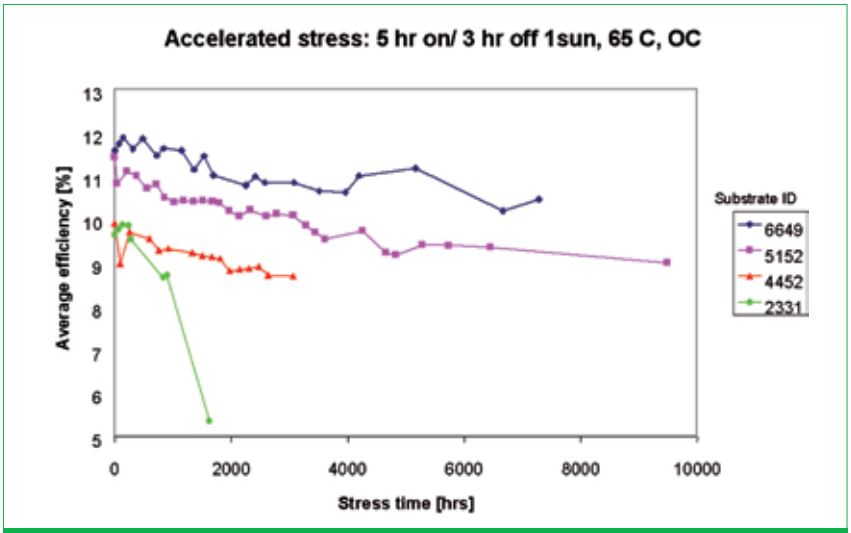

Figure 3. Effect of $CdCl_2$ treatment on stability, with each line an average of at least eight cells all with the same back contact; stress condition: 1000W/m² (five hours on out of an eight-hour cycle) illumination; open circuit bias; temperature 65°C [4].

manufacturing. Before the incorporation of the company, a 15-year process development program was conducted at CSU [1, 2] where a pilot-scale semiconductor manufacturing process was demonstrated for 8 × 9cm size substrates. PV device efficiencies of 11 to 12% [1] were routinely obtained while developing an understanding of how process conditions have an impact on device performance and stability (resistance to performance degradation under stress) [2,3]. Optimization of process conditions, particularly the cadmium-chloride ($CdCl_2$) treatment [1,4], was required to achieve good initial performance with excellent stability [3].

Fig. 3 shows the variation in stability with intentional changes in the $CdCl_2$ process. Copper doping at the back of the device was found to increase performance by reducing the device series resistance. When processed with optimal quantities and annealing temperatures, no significant variation in the copper depth profile was seen after stress when devices were analyzed by secondary ion mass spectrometry (SIMS), as shown in Fig. 4. Process repeatability over multiple runs and controlled operation over relatively long duration operation were also demonstrated [4]. The pilot-scale effort successfully proved the feasibility and capability of the inline semiconductor deposition process and enabled the formation of the company [5,6].

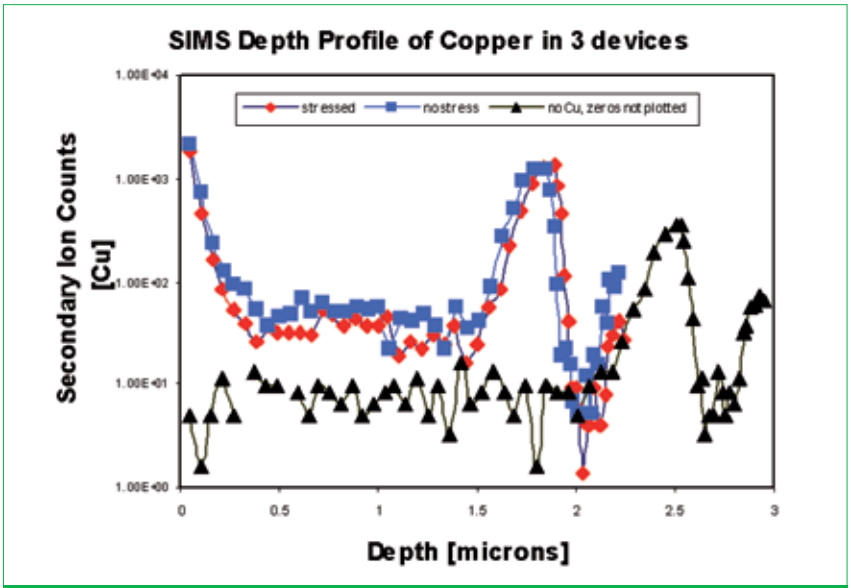

Figure 4. SIMS depth profile of nearly identical devices with and without stress. Stress condition: 3300 hours at 1000W/m² illumination (five hours on out of an eight-hour cycle); open circuit bias; 65°C temperature.

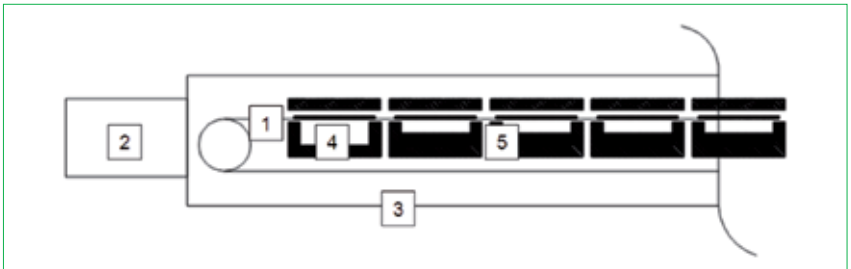

Figure 5. Schematic cutaway detail view of a portion of the semiconductor deposition system showing: (1) the substrate transport belt; (2) the entry loadlock; (3) the vacuum chamber; (4) the substrate heater; and (5) the series of HPD sources for sequential processing. The substrate is positioned between the upper and lower sections of the HPD sources on the belt conveyor.

Semiconductor processing

The heart of Abound's semiconductor processing toolset is the heated-pocket deposition (HPD) technology developed by the founding team at CSU [7]. The HPD technology can be configured to perform substrate heating, thin-film deposition, or chemical heat treating (such as the $CdCl_2$ treatment) and can operate in modest vacuum (~10^{-2} Torr) conditions. The HPD process head is comprised of a thermally conducive crucible with recesses or 'pockets' positioned under the substrate. A thermally active element that provides either heating or cooling is aligned over the substrate to further control temperature. When the crucible is heated above the sublimation point of the materials in the pocket, a vapour flux is generated. There is a separation distance between the substrate and the surface of the subliming material. Collisions between the sublimed species and the background gas (predominantly nitrogen) result in scattering, which facilitates vapour-flux uniformity. The pockets can be left empty for substrate heating processes. Substrates are transferred into the HPD unit on a conveyor belt.

A number of these HPD process heads are laid out in series to perform all semiconductor processes needed to fabricate the CdTe device. In this manner, a manufacturing system has been developed in which cleaned glass substrates enter on one side, and devices with all semiconductor processes completed emerge from the other end of the system. Fig. 5 shows a schematic illustrating some of the major components of the process tool.

The design for this semiconductor tool, including the HPD process heads, has been

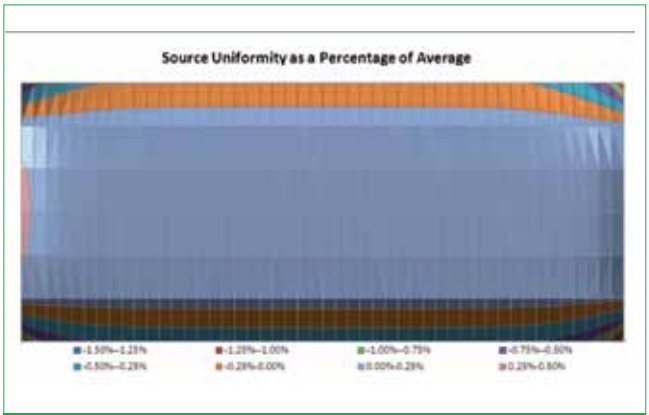

Figure 6. Finite element heat transfer computer model showing relative thermal uniformity of the HPD vapour source at operating temperatures.

optimized using finite element heat transfer and computational fluid dynamics modelling methods. Fig. 6 shows the numeric modelling results of thermal uniformity for a sample HPD vapour source; the pocket region of the process head is modelled here. Relative temperature variation would impact the vapour-flux emission uniformity in the HPD source, which ultimately affects module performance. Models such as this are used to optimize heater location and radiation shielding to minimize thermal gradients.

One design criterion for the HPD process head involved the maximization of the interval of operation before replenishment, since the maintenance frequency is different for different process heads, depending on the process and materials being vaporized. In the current-generation semiconductor tool, copper and cadmium-sulphide (CdS) process heads are run about four weeks and six months respectively, before replenishment. The latest production plan calls for the weekly replenishment of the CdTe and $CdCl_2$ process heads, after continuous operation and prior to chemical depletion.

The production tools are completely automated, with manual intervention needed only for servicing. Substrate loading, loadlock operation, belt indexing, HPD operation, and completed semiconductor plate unloading are also fully automated. Multiple tools operate simultaneously, with both upstream and downstream automated glass-handling systems in the factory. Tools are serviced sequentially, with all equipment operational or only one tool offline for replenishment at any given time.

Development speed

On a number of levels, Abound has developed at a rapid clip. The company has progressed from its initial formation to large-scale commercial shipment of Underwriters Laboratories- and IEC-certified products in less than 36 months. The semiconductor processing technology was taken from a pilot-scale demonstration for 8 × 9cm substrates to encapsulated prototype 120 × 60cm modules in under 24 months. The Longmont manufacturing line development took 17 months to progress from the signing of a lease on an empty building to automated fabrication of commercial modules.

Yields have increased through a consistent effort to identify, understand, and address root cause issues. Three processes – patterned laser scribing, perimeter deletion of semiconductor films, and encapsulation edge-seal application – were key targets of yield improvement efforts.

Patterned laser scribing of the semiconductor films is used for module series interconnection. Incomplete scribe lines can reduce the module power through a decrease in the shunt resistance or an increase in the series resistance. Process tuning and revisions to the laser optics cleaning have led to yield enhancements. The perimeter deletion of the semiconductor films removes any coatings around the edge of the module. High pot yield losses were significantly diminished through revisions to the edge-delete process,

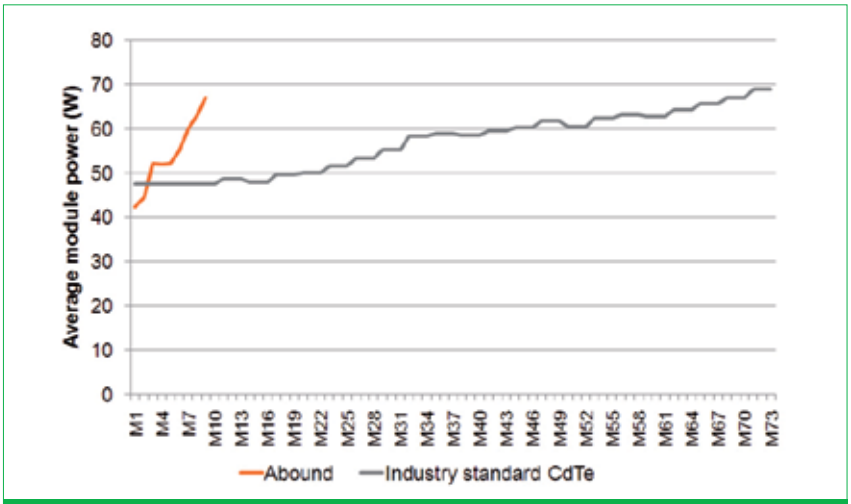

Figure 7. Module power output compared to a leading CdTe vendor.

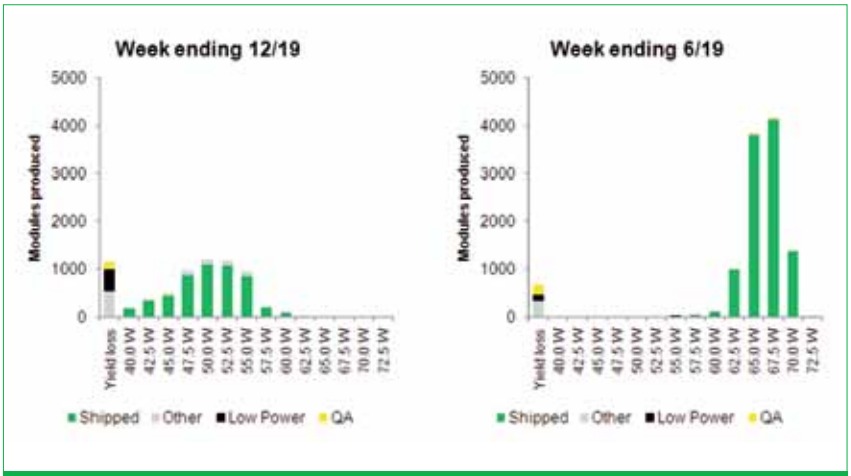

Figure 8. Representative production yield and efficiency improvements for the first half of 2010.

specifically the motion control software. Yield losses from the encapsulation edge-seal application processes were significantly reduced with the design and implementation of a new injector nozzle to apply silicone compounds without gaps.

At time of writing, the company produces approximately 9.5% (total-area) efficient modules. The initial production efficiencies were approximately 6% but were improved to the current levels in approximately nine months. A leading CdTe module manufacturer required approximately 65 months to achieve 9.5% modules (Fig. 7). It is believed that this relatively rapid improvement has been facilitated by the well-developed, automated HPD semiconductor process.

Average module efficiency has also improved rapidly through the optimization of semiconductor deposition. The CdS deposition and $CdCl_2$ heat treatment process were investigated for performance gains. Thinning the CdS layer is a well-known path to improved module current, as the increased current results from the improved blue light response with less absorption by the CdS window layer [8]. However, insufficient CdS leads to decreased device voltage, and it is difficult to directly measure the relatively thin CdS thickness (~60–120nm) once the CdTe film (~2 micron) is deposited over the previous layer.

> "Process tuning and revisions to the laser optics cleaning have led to yield enhancements."

A design of experiments approach was used to understand the effects of intentional process variation on module performance. Successful reductions in CdS thickness were accomplished by optimizing the substrate temperature both immediately preceding and during deposition of the film layer, while enhancements in HPD thermal uniformity, aided by the finite element modelling methods, improved CdS uniformity. These upgrades enabled reductions in the overall film thickness, while minimizing thin, low-voltage regions.

Optimal substrate processing temperatures were also developed for the $CdCl_2$ treatment. Treatment temperatures were generally increased, which resulted in higher device voltages while providing excellent device stability under accelerated stress. As with CdS, relatively minor enhancements in the $CdCl_2$ process station's thermal uniformity fostered more uniform properties across the module.

With the improvements in the overall module performance, the distribution of product performance has also narrowed (see Fig. 8). In addition to being a metric for manufacturing process capability, a narrow performance distribution benefits customers by reducing performance variation and facilitating PV system design.

Module encapsulation

The company has developed a proprietary module encapsulation design (shown in Fig. 9) that is optimized for the specific characteristics of the CdTe thin-film semiconductor deployed in

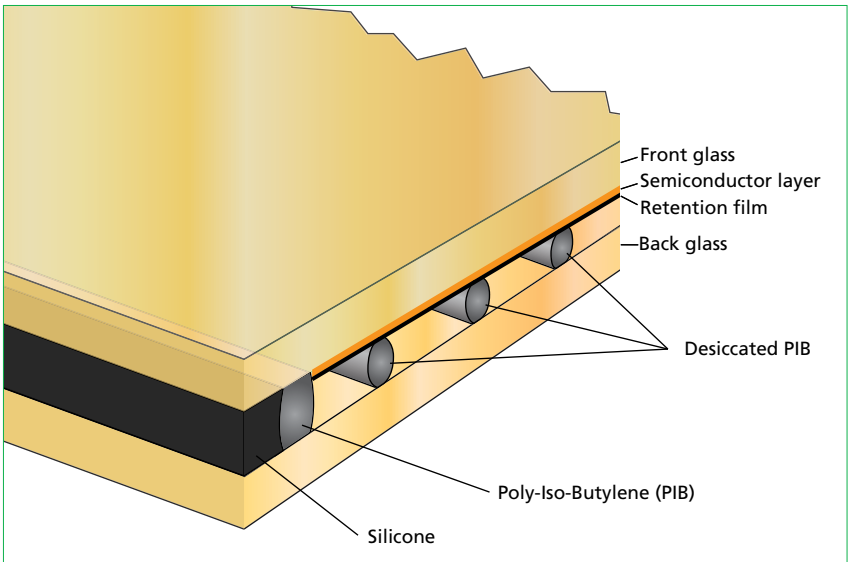

Figure 9. Diagram of module encapsulation design.

Figure 10. Desiccated PIB dispense station on a manufacturing line.

production. The objective of this design innovation was to improve reliability and manufacturability compared to existing module packaging methods.

The frameless module is constructed with two glass pieces. The heat-strengthened front glass contains the semiconductor films and faces the sun when the module is installed. A tempered back glass provides mechanical strength and is affixed to the front glass with a silicon edge seal. The silicone materials impede liquid water penetration and a poly-isobutylene (PIB) seal inboard of the silicone resists moisture-vapour ingress. Additional desiccant containing PIB bridges between the two glass plates, further improving mechanical strength (see Fig. 10). The desiccant captures any moisture that may penetrate the edge seal and will maintain low moisture-vapour levels suitable for the 30+ years of field exposure. The semiconductor material on the front glass is coated with a 'retention film', which provides an additional level of encapsulation and retains glass pieces in the unlikely event of module breakage.

The addition of the desiccated PIB inside the module structure has improved reliability and enabled the moisture level near the film to be maintained at a consistently low level during the module lifetime. Alternate encapsulation systems without internal desiccation schemes will likely see moisture levels increase as the encapsulate materials saturate with water over time. The IEC and UL certification standards require that modules pass 1,000 hours of damp-heat testing at 85°C and 85% relative humidity, widely considered a very rigorous test for thin-film modules. Modules with the novel encapsulation method and the internal desiccant have been damp-heat stressed for about 4,500 hours (Fig. 11) with no evidence of moisture ingress or significant performance degradation.

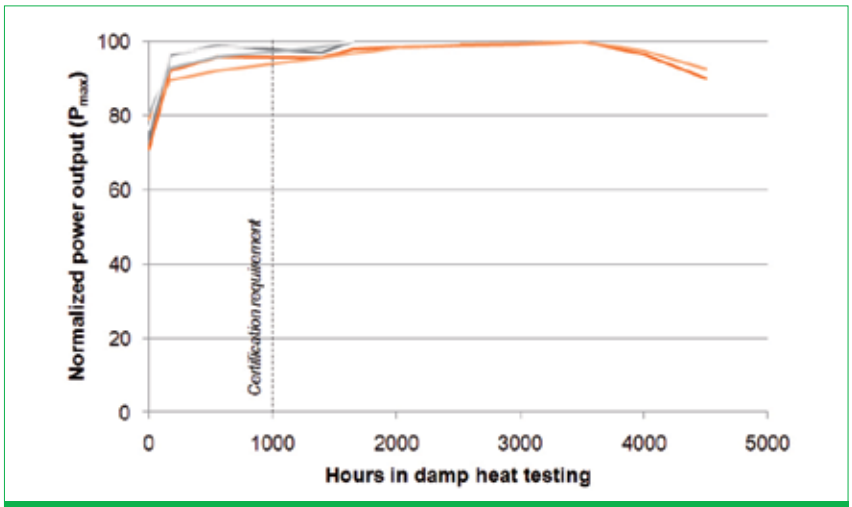

Figure 11. Performance of multiple modules in damp heat.

> "The addition of the desiccated PIB inside the module structure has improved reliability."

This module design has enabled the development of a streamlined synchronous manufacturing process, partially shown in Fig. 12. In a similar manner to the semiconductor processing tools, all module encapsulation, busbar, back-box application and potting processes are performed on automated inline equipment. The silicone/PIB edge-seal applications processes can each be performed in approximately 20 seconds per panel, in contrast to the traditional EVA lamination process cycle time of 10–15 minutes.

Capital expenditures and manufacturing costs

The company presented a detailed review of the factory construction, manufacturing equipment layout and production capacity to NREL managers to verify capital equipment costs. The review included categories such as hardware, equipment installation, building costs, and facility improvements/upgrades. When appropriate, purchase orders or quotes were used to ensure accuracy for the vendor-supplied hardware. Capital equipment costs significantly below US$1.50 per watt were demonstrated for the full build-out of the existing Longmont manufacturing facility to 200MW/year [9]. These results are among the lowest capital equipment costs reported for any PV manufacturing technology.

Module manufacturing costs are calculated to be less than US$1 per watt in the existing Longmont manufacturing facility, figures that were reviewed by NREL managers. Module manufacturing costs were demonstrated as the total manufacturing cost of sales of the modules produced in a given period divided by the total cumulative wattage output of the module produced in that same period. Direct material, variable costs including direct labour, yield losses, glass recycling, and freight costs, overhead and manufacturing equipment depreciation, were categories included

in the analysis. Manufacturing costs below US$1 per watt for the initial manufacturing facility were calculated [9], also among the lowest reported in the PV industry, particularly for an initial factory.

Summary and future challenges

A manufacturing-centric approach was taken to design the production process and product at Abound Solar. The focus on minimizing capital expense while optimizing throughput has enabled the development of a robust CdTe production platform that has demonstrated low capital and operating costs and a fast ramp of throughput and efficiency. Future developments will be focused on continuing the pace of improvements in production volumes and product conversion efficiencies to meet customer demand and to be more competitive with crystalline-silicon PV products. Once key milestones have been achieved on throughput and efficiency, the company will begin the replication of the production line to expand capacity at its existing Colorado facility as well as at the Indiana manufacturing site to be developed. The addition of numerous lines across multiple sites will test the company's ability to maintain consistency across deployment teams and equipment fabricators. Ongoing R&D activities continue to refine semiconductor deposition parameters. The company believes that the original manufacturing platform will continue to be significantly robust to accommodate such refinement and widespread deployment, but only time will tell if the strong progress of performance will continue under such conditions.

Figure 12. Module fabrication back end and binned product.

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Kurt Barth is a founder of Abound Solar and an inventor of the company's proprietary thin-film solar manufacturing technology. He is Abound's senior technologist and has also been VP of product development, on the board of directors, and corporate secretary. Barth directed the company's Solar America Initiative project with NREL and has served as project director on many federally sponsored programs. He has over 17 years' experience in photovoltaics research and manufacturing process development. In addition to eight patents in the solar field, Barth has published more than 70 refereed papers and presentations focussed on thin-film solar. He holds a B.S. and M.S. in mechanical engineering from Colorado State University.

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