Influence of wafer quality on cell performance

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ABSTRACT

An improved understanding of multicrystalline wafer quality can explain variations in cell performance across multicrystalline silicon blocks. Infrared scanning can detect precipitates in a silicon block, while photoluminescence combined with defect etching can reveal needle-like precipitates along the grain boundaries. Such precipitates typically lead to reduced shunt resistance. Crystallographic defects that lower the current collection and the final cell efficiency can also be identified. Understanding the influence of these defects is important for the development of a crystallization technology that results in a substantially better cell efficiency. The use of the improved material quality in an innovative cell and module technology have led to the world record module efficiency of 17%. This paper will illustrate one example of how an improved understanding of multicrystalline wafer quality can explain the variations in cell performance.

Introduction

In order to make solar energy a viable energy source, it is important to decrease the cost per Watt peak. The use of multicrystalline instead of monocrystalline silicon for solar cell production substantially lowers the cost, but also results in a lower cell efficiency potential. REC's presence along the entire value chain allows the company to better optimize the quality of silicon ingots for solar cell purposes and in this way decrease the cost of solar energy.

Experiment & results

Experimental procedure

A lower quality silicon block was taken from normal production and wafers from bottom to top were processed into solar cells. The blocks and wafers were characterized using lifetime measurements (Semilab WT-2000-PV); photoluminescence (PL; LIS-R1 BT Imaging); IR scanning (Intego) and defect etching. Lifetime values were measured on wafers that were passivated with an a-Si:H layer. The finished cells were characterized using IV, LBIC and PL.

Fig. 1 shows the relative cell efficiency from bottom to top of the selected block, the same block as is referred to throughout this paper. As can be seen, the efficiency changes by as much as 5% relative throughout the block. In the same graph the lifetimes are shown from the as-cut wafers and from neighbouring phosphorous-gettered wafers (using standard diffusion process). As outlined in the literature [1], P gettering leads to large increases in the minority carrier lifetime across the entire block with the largest increase occurring in the bottom and top regions, a characteristic that has been illustrated by the gettering efficiency of a highly phosphorous-doped layer on mobile metal impurities such as iron. These metals are present mostly in the bottom and top part of the ingot which explains the largest lifetime increase in that area [2]; however, the lifetime in the bottom of the ingot stays relatively low due to the high oxygen level [3]. The lifetime profile along the block after gettering coincides well with the overall efficiency profile.

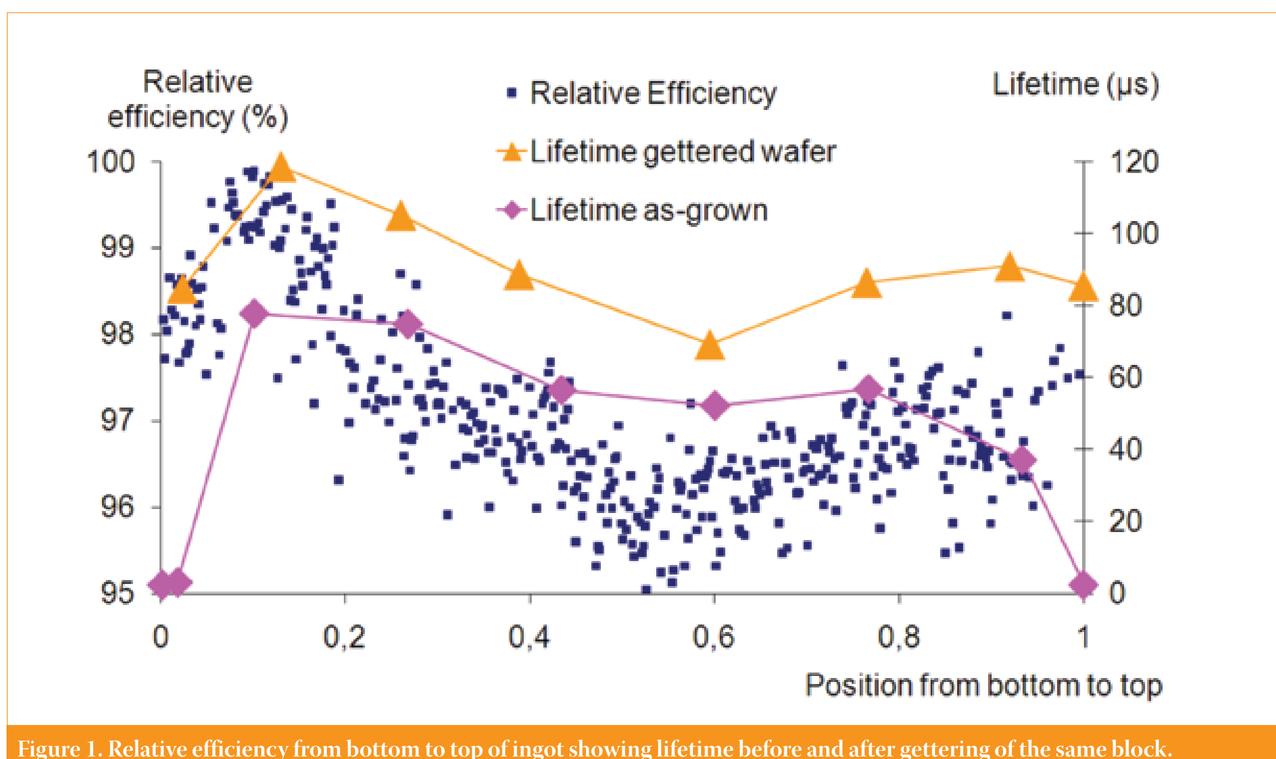

Figure 1. Relative efficiency from bottom to top of ingot showing lifetime before and after gettering of the same block.

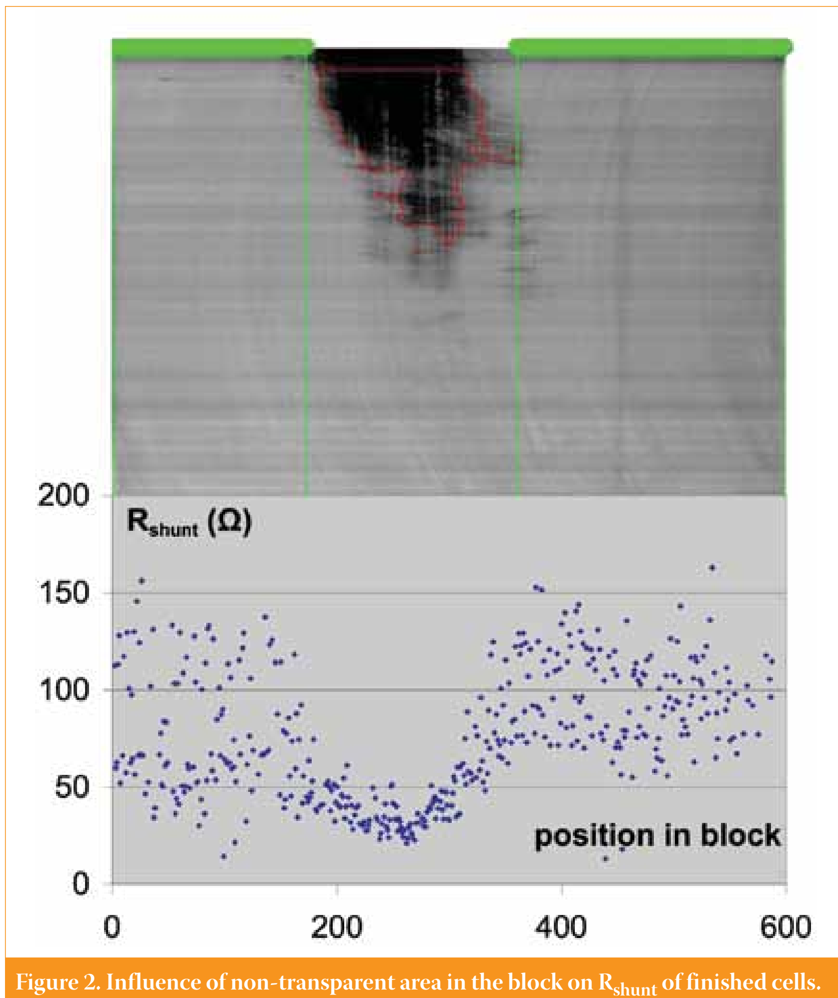

Figure 2. Influence of non-transparent area in the block on R_{shunt} of finished cells.

The lifetime of as-grown material has a less clear correlation to cell efficiency and thus has limited value for sorting purposes of initial material, as good cell performance can be obtained in low-lifetime regions of the block (e.g. the bottom and top).

Influence of inclusions

Using IR transmission, a significant non-transparent ('black') region showed in the middle of this block, as illustrated in Fig. 2. The image also shows the shunt resistance values of cells from the same position of the above block. These black areas lead to cells with a reduced shunt resistance, which led to the black areas being investigated in more detail on wafers that were cut out from this position. Fig. 3 shows the photoluminescence image of such a wafer, where the red circle corresponds with the black area of Fig. 2. The grain boundaries in that region have a low luminescence signal indicating their high activity [4].

Further analysis was carried out on these wafers using a silicon etch followed by SEM. The right-hand image of Fig. 3 zooms in on a grain boundary in that black region. One can clearly recognize the precipitate formation along the grain boundaries that reduced the shunt resistance of the cells. The nature of such precipitates has been investigated in detail by several groups [5]. It is worth noting that the reduction in R_{shunt} and the large presence of inclusions appear to begin (as crystallization starts from the bottom) roughly at the same place or slightly earlier than the drop in cell efficiency. Furthermore, the lowest cell efficiencies appear to continue for some time after the presence of inclusions has dropped, indicating that additional crystal defects may form around the inclusions and continue for some time after their disappearance.

> "The lifetime of as-grown material has a less clear correlation to cell efficiency and thus has limited value for sorting purposes of initial material."

Influence of dislocations

The orange circles in Fig. 3 show regions with high dislocation density and increased recombination activity. Many investigations into this phenomenon in the past have concluded that this kind of defect originates from the metal

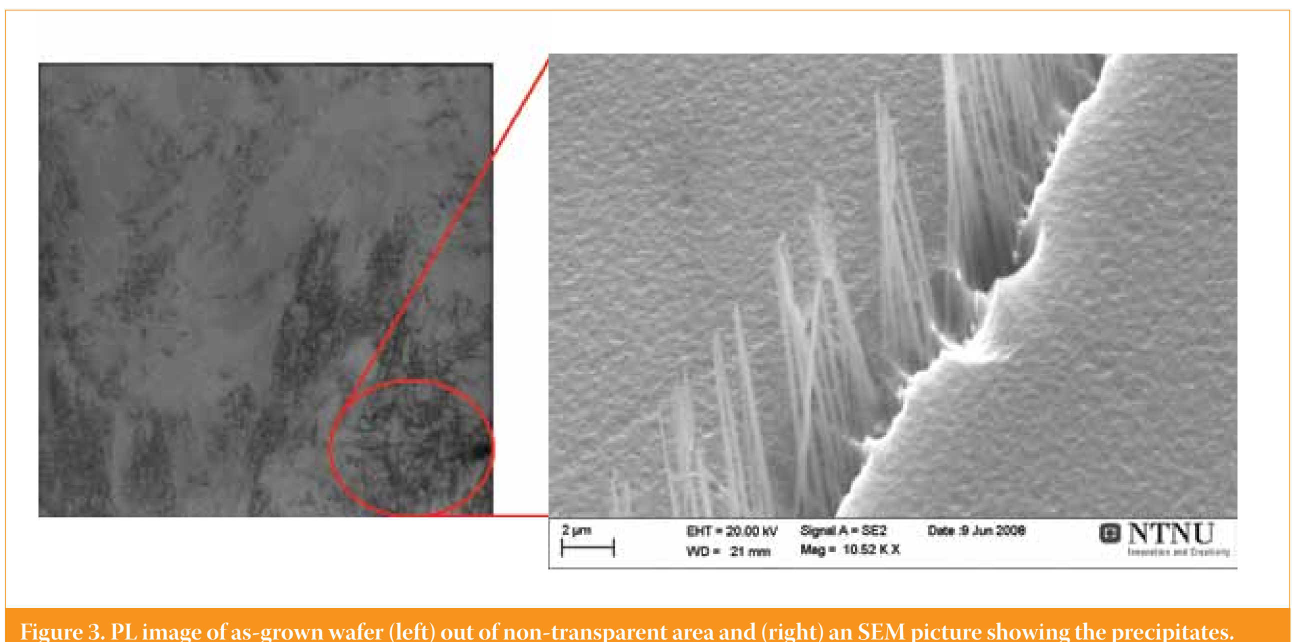

Figure 3. PL image of as-grown wafer (left) out of non-transparent area and (right) an SEM picture showing the precipitates.

decoration [6]. Fig. 4 shows the LBIC scan of a cell neighbouring the wafer shown in Fig. 3. Clearly, the dislocated areas strongly reduce the current collection [7]. It was found that the drop in efficiency in the middle of the block (Fig. 1) was mainly caused by the increasing amount of dislocated areas rather than the areas containing the precipitates [8], as explained before on the correlation between the two types of defects.

Cell results

A new crystallization technology has been developed by REC in order to minimize the influence of inclusions, metallic and crystallographic defects [9]. Fig. 5 shows the average efficiency from bottom to top for both the old and the new technology. The new technology leads to a large increase in efficiency, mainly in the bottom of the block. Towards the top of the block the efficiency decreases due to increased amounts of crystallographic defects that multiply from the bottom towards the top. Further development is carried out to reach similar efficiencies throughout the entire ingot and to align the efficiencies of all REC furnaces.

Table 1 shows the best or average cell efficiency for different multicrystalline silicon quality ranges. In industrial lines, the highest efficiencies on the best multicrystalline material are currently yielding similar efficiencies as standard monocrystalline silicon material in the same lines. This best material is taken from the bottom part of the new ingots. Using an advanced cell design, a maximum cell efficiency of 17.9% was obtained [10] and a world record module was made with 17% module efficiency [11].

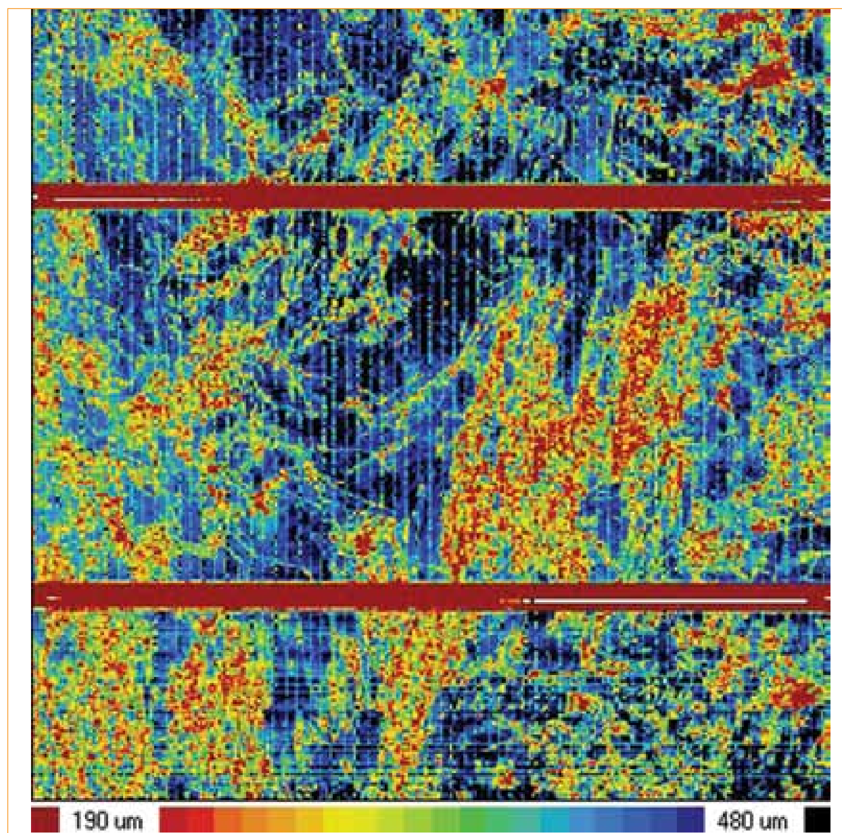

Figure 4. LBIC scan of a neighbouring cell to that shown in Figure 3.

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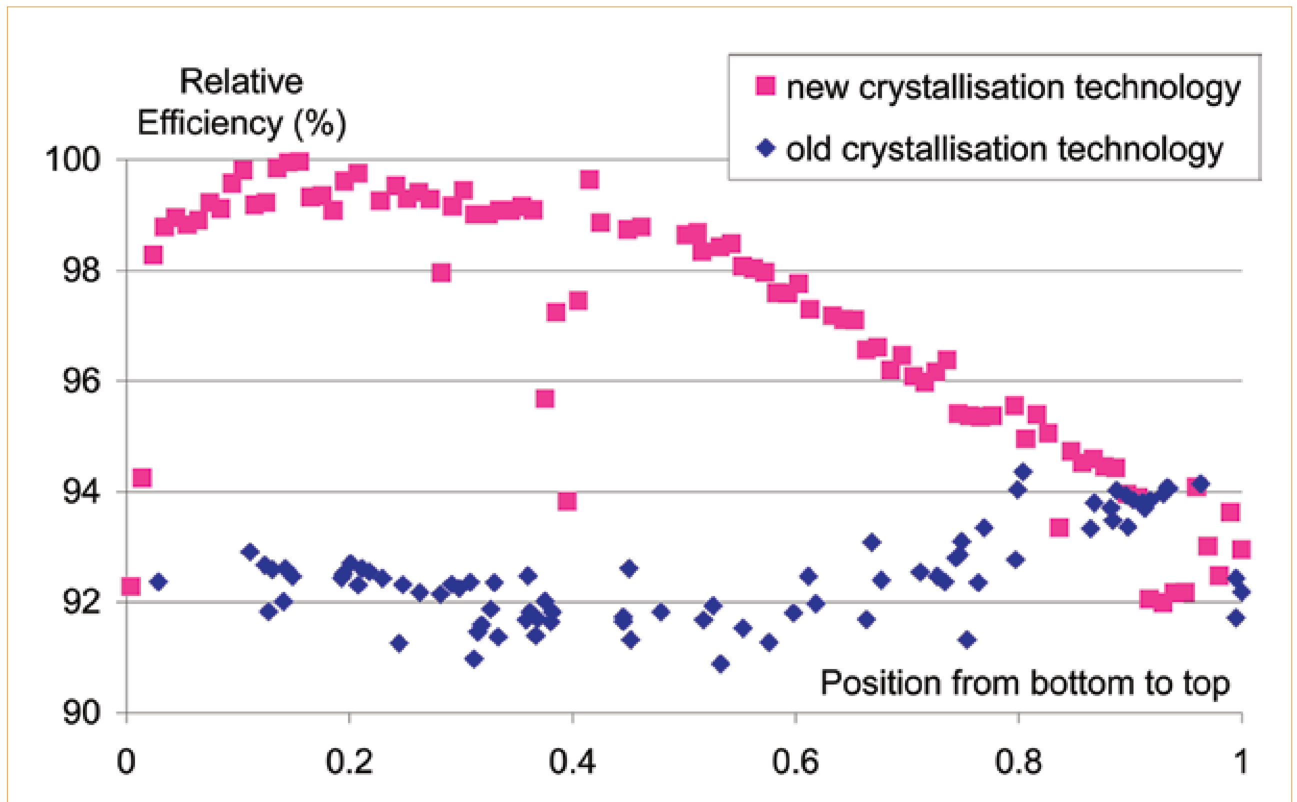

Figure 5. Relative efficiency profile from bottom to top for the old and new crystallization technologies.

Conclusions

Extensive characterization during wafer production and subsequent cell processing demonstrates the significant effect of precipitates, impurities and crystallographic defects. These are elements that limit the performance of mc-Si and are challenges in the long-term development of technology. Using an internally developed crystallization technology, a large increase in cell efficiency could be obtained, initially mainly in the bottom part of the ingots.

Quality	Cell Process	Efficiency (%)
Average multi	Industrial	15-16.5
Best multi*	Industrial	16.9
Average p-mono	Industrial	16.5-17.5
Best multi*	Advanced front side	17.9

*internally developed crystallization technology.

Table 1. Cell efficiency as function of crystalline quality and cell process type.

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