Solutions to realizing LID-controlled multi-PERC cells and modules

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Abstract

State-of-the-art black-silicon texturing technology has been successfully implemented in all of the 4.5GW multi-Si cell production lines at Canadian Solar (CSI). With a combination of black-silicon texturing and diamond-wire-sawn wafers, it has been possible to increase cell efficiency and wattage, while significantly reducing the cost. To further improve CSI's multi-Si product performance and cost, multi-Si passivated emitter rear contact (multi-PERC) technology has been developed to achieve a mass production cell efficiency of more than 20% on average, and a module power exceeding 300W. By the end of 2017, a production capacity of over 1GW had been established, and CSI's majority multi-Si cell capacity will be upgraded to PERC in 2018. This paper will introduce the solutions to realizing light-induced degradation (LID)-controlled multi-PERC cells and modules, as well as offering a discussion of the degradation performance. In addition, the technology evolution of CSI's high-efficiency multi-Si products and a roadmap for 22%-efficiency multi-Si cells are presented.

Background

For the past few years, multi-Si has been the mainstream technology, holding a majority market share. However, multi-Si's leadership of the market is facing a serious challenge from mono-Si, which is demonstrating inherently higher efficiencies and whose wafer costs are rapidly decreasing. It is therefore critically important to implement promising technologies such as diamond-wire sawing, black-silicon texturing and PERC in the mass production of multi-Si cells in order to improve efficiencies and further reduce costs.

By Q3 of 2017, CSI had successfully implemented diamond-wire sawing and state-of-the-art black-silicon texturing in all its multi-Si cell production lines, with a total capacity of 4.5GW and a mass production efficiency exceeding 19.2% [1]. The integration of PERC technology in multi-Si cells, however, is much more challenging, particularly because of light-induced degradation (LID) and light- and elevated-temperature-induced degradation (LeTID) issues [2–6]. It has been reported by UNSW and other institutes that two degradation modes exist in multi-PERC: 1) the fast degradation mode, which occurs within 100 hours and is caused by Type 1 defects; and 2) the slow degradation mode, which occurs over a period of up to one thousand hours and is caused by Type 2 defects [3]. Nevertheless, the LeTID effect reported by Hanwha Q-CELLS in multi-PERC is a cause of great concern for this technology [5,6].

By combining technical innovations throughout ingot material control, cell process optimization, advanced regeneration and intensified inline process control, CSI realized a mass production of LID-controlled multi-PERC cells and modules with a total capacity of over 1GW by the end of 2017; this capacity will be ramped up to more than 4GW by the end of 2018. In this paper, the performance of CSI's multi-PERC cells and modules will be presented, and the solutions to realizing LID-controlled multi-PERC cells and modules will be introduced.

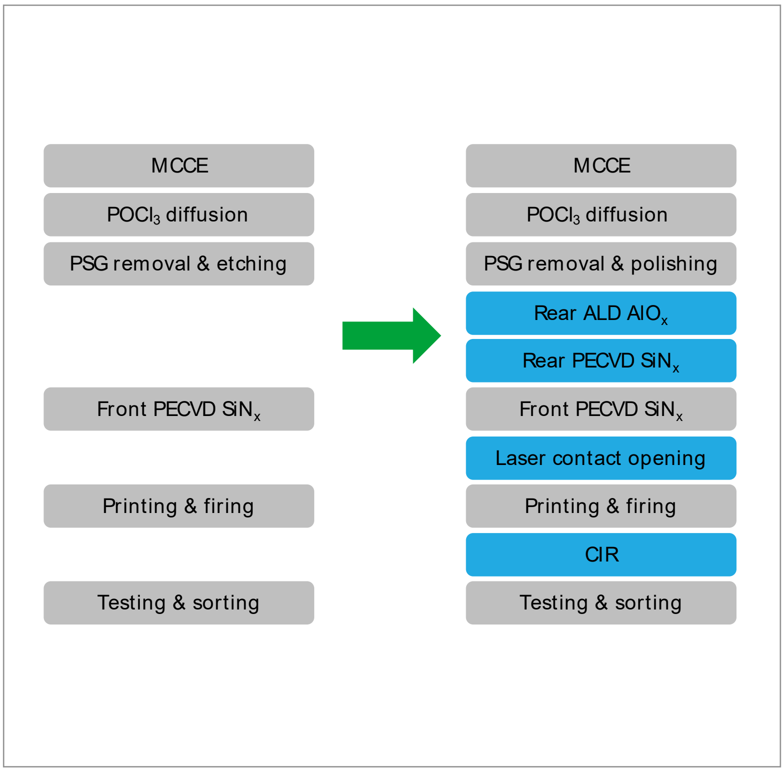

Figure 1. Process flows for conventional multi-Si cells (left), and CSI's high-efficiency multi-PERC cells (right).

Performance of multi-PERC cells and modules

Fig. 1 shows the process flow for CSI's high-efficiency multi-PERC cells; the process flow for non-PERC cells is also shown for comparison purposes. After CSI's proprietary state-of-the-art black-silicon texturing (metal-catalysed chemical etching – MCCE), an n^+-Si emitter is formed by

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low-pressure $POCl_3$ diffusion in the tube furnace. The next step is phosphosilicate glass (PSG) removal and rear-side polishing.

Al_2O_3 layers deposited by the atomic layer deposition (ALD) technique are used to passivate the rear surfaces. The post-deposition annealing of as-deposited Al_2O_3 layers is integrated in the subsequent rear-side SiN_x anti-reflection coating (ARC) deposition by a tube plasma-enhanced chemical vapour deposition (PECVD) process. The front-side SiN_x ARC is also deposited by the tube PECVD process.

Following laser contact opening, the metallization is performed by screen printing and a co-firing process. All the as-fired multi-PERC cells then go through a current-induced regeneration (CIR) process, before the final testing and sorting.

The efficiency distribution of CSI's multi-PERC cells is shown in Fig. 2; the average efficiency of the cells exceeds 20%, which equates to a 0.9% efficiency gain compared with conventional multi-Si cells based on diamond-wire-sawn (DWS) wafers.

A comparison of the *I–V* parameters for multi-PERC and conventional black-silicon multi-Si cells is given in Table 1. The open-circuit voltage V_{oc} is boosted by 13.6mV, and the short-circuit current I_{sc} is increased by 320mA, by employing multi-PERC technology.

As regards module performance, as shown in Fig. 2(a), the average wattage of standard 60-cell multi-PERC modules exceeds 287W, which is comparable to that achieved by mono-Si modules. In combination with the use of module technologies such as half-cut and multi-busbar, the average wattage of 120-cell multi-PERC modules exceeds 300W, as shown in Fig. 2(b); this is again comparable to that for mono-PERC modules. Clearly, the implementation of multi-PERC enhances the competitiveness in terms of performance of multi-Si compared with mono-Si, but at a lower cost.

Solutions to controlling LID

LID issues are much more challenging for multi-PERC than for mono-PERC. Direct evidence of this is that there are many manufacturers who can produce quality reliable mono-PERC modules, but only a few who are able to produce multi-PERC modules [7].

UNSW and other research institutes have proposed the existence of both a fast degradation mode, occurring within 100 hours and caused by so-called *Type 1 defects*, and a slow degradation mode, lasting up to one thousand hours and caused by so-called *Type 2 defects*. The Type 1 defects have been identified as being B–O defect complexes, whereas the Type 2 defects are not yet fully explained. Hydrogen [8] or metal impurities such as Fe, Co and Ni [9] are the most likely suspects for Type 2 defects. UNSW recently

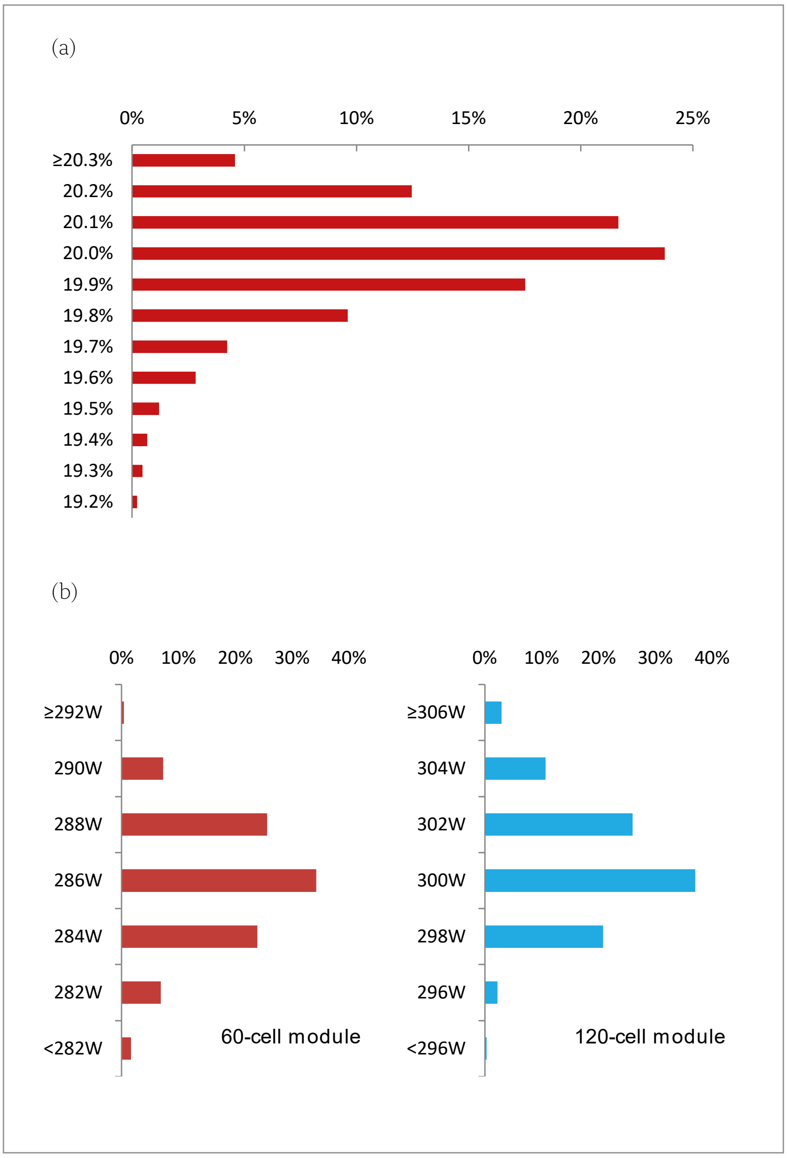

Figure 2. (a) Efficiency distribution of multi-PERC cells. (b) Wattage distribution of 60-cell and 120-cell multi-PERC modules.

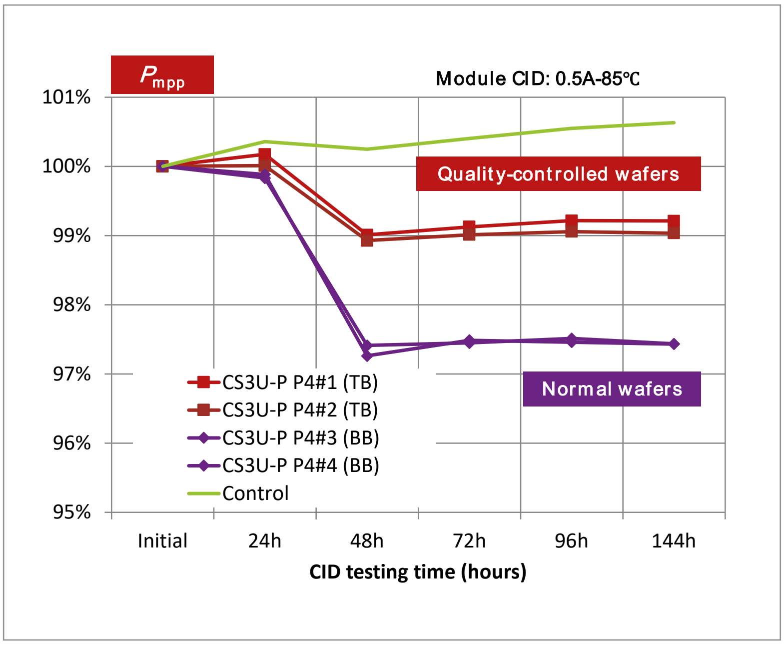

Figure 3. Effect of wafer quality on degradation performance of multi-PERC modules.

ΔV_{oc} [mV]	ΔI_{sc} [mA]	ΔFF [%]	$\Delta\eta$ [%]
+13.6	+320	−0.77	+0.90

Table 1. *I–V* parameter differences between multi-PERC cells and conventional black-silicon multi-Si cells.

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reported that these Type 1 and Type 2 defects are also present in p-type mono-Si and n-type mono-Si [10].

To solve the most challenging LID issues for multi-PERC, CSI has implemented several technical innovations:

1. A unique ingot-casting process to control the impurity content within multi-Si wafer materials.

2. An optimized cell process, especially with regard to the metallization, in order to suppress defect-complex formation and to enhance hydrogen passivation of the multi-Si bulk.

3. An advanced regeneration process to deactivate the defects that cause LID.

4. An intensified inline process control to create reliable LID-controlled multi-Si PERC cells and modules.

The degradation rate for multi-PERC is dependent on the ingot and wafer material quality. For multi-Si ingots, the trend generally seen is that the degradation rate increases from the top part of the ingot to the bottom part. Additionally, there are various effects on the degradation rate arising from resistivity or doping concentration, oxygen content and structural defect density. The degradation rate is also sensitive to the dopant – B or Ga or a mixture of B and Ga; the beneficial effect of Ga doping, or partial Ga doping, is widely accepted. Fig. 3 shows the notable differences in multi-PERC module degradation, tested by current-induced degradation (CID), between quality-controlled and normal multi-Si wafers.

The significant impact of the firing temperature on degradation has been widely investigated [11,12]. Either lowering the peak temperature or lowering the cooling rate in the firing process will help to reduce the degradation rate considerably. Many theories to explain these findings have been proposed [11–14]; possible explanations are that a reduced firing temperature will suppress defect formation and/or change the hydrogen content in the multi-Si bulk.

The key to reducing the degradation rate of multi-PERC is the advanced regeneration process. The regeneration process to address the defect complexes causing LID consists of excess carrier injection, and adequate temperature and duration time [15]. Generally, for mono-PERC a light-induced regeneration (LIR) process using a halogen lamp, LED or laser is used [15]; however, the industrial LIR process is not adequate for use with multi-PERC. CSI uses a proprietary CIR process; compared with LIR, there are many advantages of CIR, such as a broader process window, higher throughput, lower electricity consumption and lower cost. By using the CIR process, the degradation rate can be reduced by up to 80%.

Fig. 4 shows the correlation between the reduced degradation rate after CIR treatment and the degradation rate without CIR treatment, tested by CID. It can be seen that the higher the degradation rate for multi-PERC cells without CIR treatment $CID_{w/o\ CIR}$, the greater the mitigation coefficient $CID_{w/o\ CIR}$-CID_{CIR} reflected in the reduced degradation rate. Interestingly, there is a quasi-linear correlation between $CID_{w/o\ CIR}$-CID_{CIR} and $CID_{w/o\ CIR}$, indicating that the CIR process effectively passivates the defect complexes causing LID. Moreover, it can be seen that the quality of the wafers from some suppliers (suppliers 1 to 4) is not satisfactory, showing a very high degradation rate without CIR treatment. This again reflects the importance of controlling the quality of the ingot and wafer materials in order to produce multi-PERC cells with controlled LID.

The reason why it is much more challenging to control the LID with multi-PERC than with mono-PERC is primarily the wide variation in quality of multi-Si wafers [6]. Even though innovative steps have been taken to control the impurity concentration of multi-Si ingots, it is still essential to reinforce the inline process control; in particular, a more exhaustive monitoring of degradation rate at the cell level is necessary, in addition to prompt process optimization in response to fluctuations.

Normally the LID of Si solar cells is tested by light-soaking; however, this technique has some drawbacks, such as a test time that is too long (typically 24–72 hours), imprecise control of the wafer temperature, and limited sample volume. To test the LID performance of multi-PERC cells, CSI uses the CID method, which offers several advantages, as listed in Table 2.

The set-up of the CID method is also illustrated in Table 2. The parameters for the CID method are forward-biased injection current, wafer temperature and duration. These parameters are

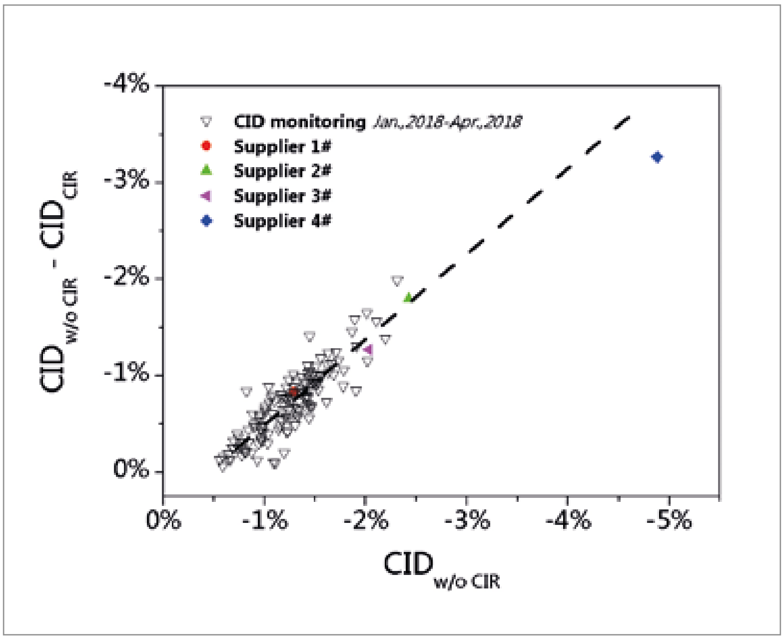


Figure 4. LID mitigation coefficient of the CIR process, reflected in the reduced degradation rate.

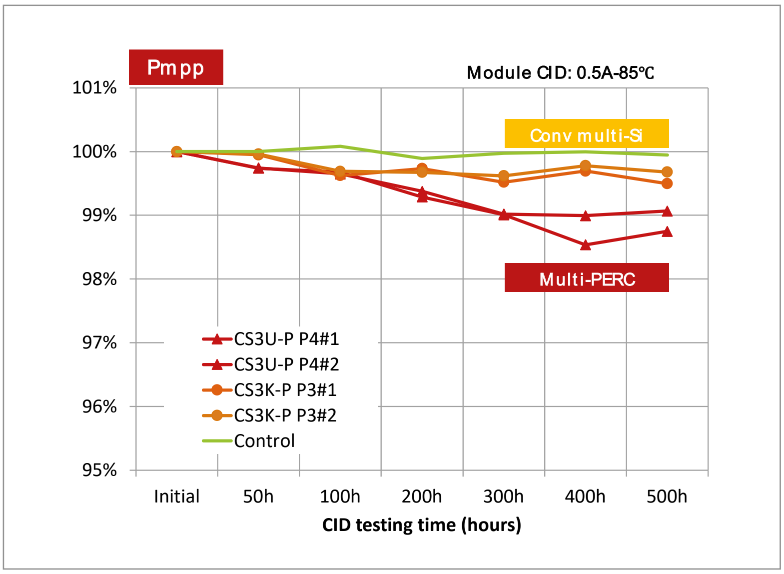


Figure 5. Module performance of CSI's multi-PERC modules undergoing CID testing.

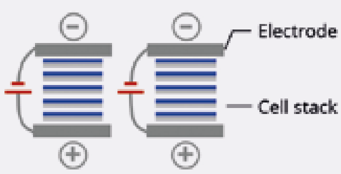
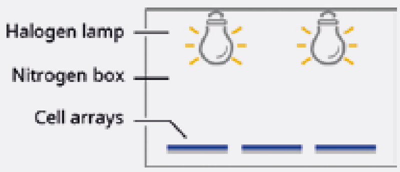
	CID (typical conditions: 3.5A-105°C-4h)	LID (typical conditions: 1,000W/m²-65°C-24h)
Injection intensity	Controlled by forward-biased current (0–10A)	Controlled by light intensity (0–1 sun)
Cell temperature control	50–150°C adjustable, accuracy <5°C	Not easy to control, sensitive to light intensity
Batch capacity	Up to 80 cells per stack, with small footprint	10–100 cells per tiled array, with large footprint
LeTID correlation	Higher temperature higher correlation	Not easy to control temperature above 75
Schematic set-up		

Table 2. Advantages of CID over LID in testing the degradation behaviour of multi-PERC cells.

> "The next step will be an integration of advanced technologies to upgrade to P4+, with an efficiency of up to 20.6%."

carefully selected after extensive experimental studies to reflect the degradation rate of multi-PERC cells as much as possible. In fact, if setting the injection current and wafer temperature parameters to certain values results in a regeneration-dominant effect, it is a CIR process; on the other hand, if lower values for the injection current and wafer temperature result in a degradation-dominant effect, it is a CID process. The chosen CID parameters are 3.5A, 105℃ and 4 hours, which is equivalent to testing LID by light-soaking with the parameters 1,000W/m^2, 65℃ and 24 hours; in addition, the sampling rate used is 0.08% of the total number of cells produced for each cell line. The use of this strategy results in excellent control of the CID of multi-PERC cells, to less than 1%.

For the module degradation test, the CID method is also used instead of indoor or outdoor light-soaking methods, with the set-up and parameters suggested by Hanwha Q-CELLS. Fig. 5 shows the comparison of CID degradation between multi-PERC modules and conventional multi-Si modules. The figure highlights that there is an increase in the module degradation rate of multi-PERC modules, as compared to conventional multi-Si modules. After 300 hours, however, the degradation rate of multi-PERC modules stabilizes, and proves to be less than 1.5% for up to 500 hours of testing; this is equivalent to two years of hot climate outdoor exposure, as proposed by Hanwha Q-CELLS [16].

All the cell and module degradation results demonstrate that, after taking several technical innovative steps, the LID of CSI's multi-PERC cells and modules can be successfully controlled.

Future roadmap

CSI specializes in producing high-efficiency multi-Si cell and modules. In 2017 there was a rapid evolution of technology and products, and this is expected to continue in 2018, as shown in Fig. 6. By Q3 of 2017, conventional P2 (slurry wafer and acid texturing) was phased out and fully upgraded to P3 (DWS wafer and black-silicon texturing), in a total capacity of 4.5GW. Additionally, starting from Q3 of 2017, P4 (DWS wafer, black-silicon texturing and multi-PERC) was phased in, and the capacity will be more than 4GW by the end of 2018. The next-generation high-efficiency multi-Si product P5 will begin to be phased in from Q3 of 2018 and will gradually gain more share.

On the basis of the current P4 product with an efficiency of greater than 20%, the next step will be an integration of advanced technologies (including bifacial, selective emitter, multi-busbar, paste optimization) to upgrade to P4+, with an efficiency of up to 20.6%. Further down the line, the goal is to upgrade to the next-generation wafer technology P5, with an efficiency of up to 21.5%, and eventually to P5+, approaching an efficiency of 22%.

Figure 6. Technology evolution of CSI's high-efficiency multi-Si product: P2 (conventional slurry), P3 (MCCE+DWS), P4 (multi-PERC), P5 (next-generation multi-Si).

Conclusion

Through innovations in materials, cell processing, advanced regeneration and enhanced inline process control, CSI has successfully demonstrated LID-controlled multi-PERC cells and modules in GW capacity. Multi-PERC technology is a must for high-efficiency multi-Si products to compete with upcoming high-volume mono-Si products. In order to further improve competitiveness, the fabrication of bifacial multi-PERC and an integration of advanced technologies to push efficiencies even higher will be essential.

References

[1] Wang, X. et al. 2017, *Photovoltaics International*, 35th edn, pp. 67–72.

[2] Ramspeck, K. et al. 2012, *Proc. 27th EU PVSEC*, Frankfurt, Germany, pp. 861–865.

[3] Hallam, B. et al. 2016, *physica status solidi (RRL)*, Vol. 10, No. 7, pp. 520–524.

[4] Luka, T. et al. 2016, *Photovoltaics International*, 32nd edn, pp. 43–48.

[5] Fertig, F. et al. 2015, *physica status solidi (RRL)*, Vol. 9, No. 1, pp. 41–46.

[6] Kersten, F. et al. 2015, *Sol. Energy Mater. Sol. Cells*, Vol. 142, pp. 83–86.

[7] Fertig, F. et al. 2017, *Energy Procedia*, Vol. 124, pp. 338–345.

[8] Wilking, S. et al. 2014, *Sol. Energy Mater. Sol. Cells*, Vol. 131, pp. 2–8.

[9] Luka, T. et al. 2017, *Proc. 33rd EU PVSEC*, Amsterdam, The Netherlands, pp. 413–417.

[10] Niewelt, T. et al. 2017, *J. Appl. Phys.*, Vol. 121, p. 185702.

[11] Glunz, S. et al. 2001, *J. Appl. Phys.*, Vol. 90, pp. 2397–2404.

[12] Bothe, K. et al. 2002, *Proc. 29th IEEE PVSC*, New Orleans, Louisiana, USA, pp. 194–197.

[13] Unsur, V. et al. 2016, *Proc. 43rd IEEE PVSC*, Portland, Oregon, USA, pp. 717–719.

[14] Kouhlane, Y. et al. 2016, *J. Electron. Mater.*, Vol. 45, pp. 5621–5625.

[15] Herguth, A. et al. 2009, *Proc. 24th EU PVSEC*, Hamburg, Germany, pp. 974–976.

[16] Kersten, F. et al. 2017, *Proc. 33rd EU PVSEC*, Amsterdam, The Netherlands, pp. 1418–1421.

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