Increasing the efficiency of multicrystalline silicon solar cells

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ABSTRACT

Standard solar cell technology nowadays offers a variety of measures – some linked, some not – to continuously improve conversion efficiency. The starting point for considering the different improvement steps is a kind of standard cell as produced on most current production lines. The main elements of this cell are diffused junction, aluminium back-surface field and screen-print metallization. This type of cell suffers losses from different sources like optics, recombination and resistance that can be considerably lowered to obtain higher cell efficiency. This paper will describe improvement steps on the standard type of multi-crystalline cell before addressing cell concepts that open further potential.

Introduction

Over the last couple of years photovoltaics has grown into a respectable sized industry. An enormous pull from the market has brought an average annual growth rate of more than 30% as the whole industry scaled up production across the value chain. This extraordinary growth fired by an enormous amount of equity money also allowed some big players in the industry to put huge efforts into R&D of crystalline cell technology.

Since the financial crisis also hit the solar industry, the solar cell market has been faced with new challenges. As with volumes, the prices for solar cells dropped dramatically. With further decreases anticipated, it all comes down to whether or not manufacturers can be competitive in terms of €/Wp. As Fig. 1 shows, there are different factors that can influence how best to reach that goal. Based on an internal Q-Cells analysis, cost reduction potential for multi-crystalline silicon is up between 40 and 50% from today's cost levels. Technology is a key driver to reach this cost reduction by 2015.

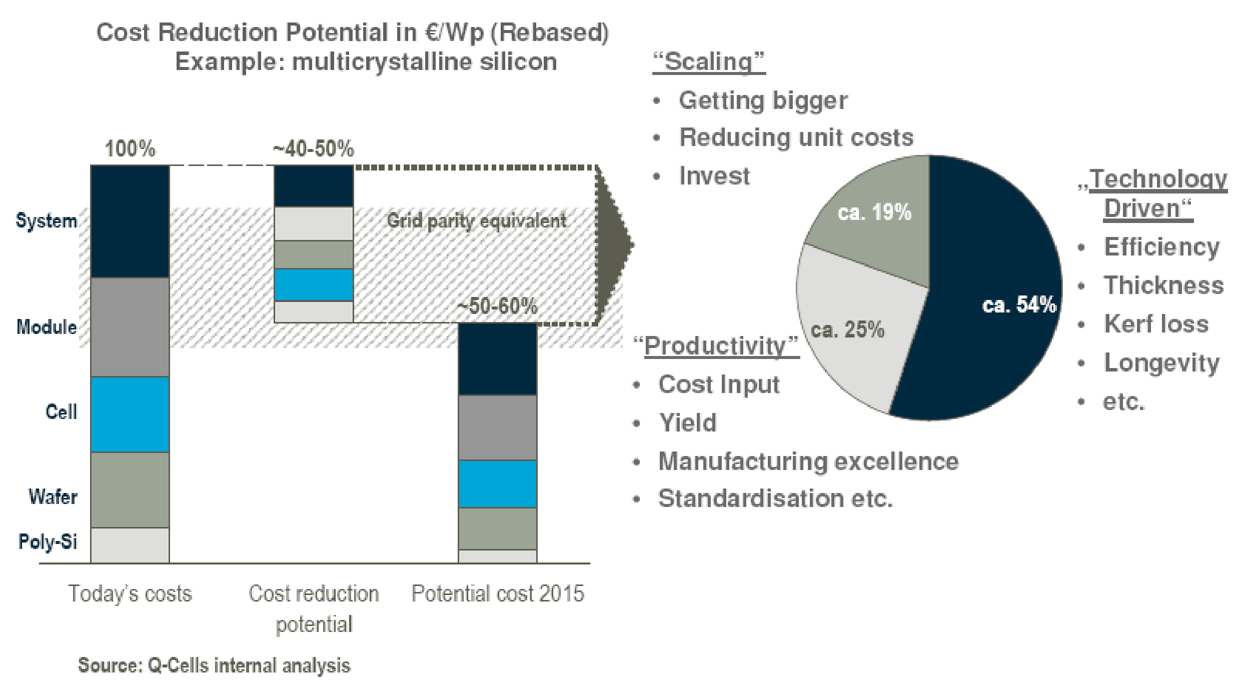
This article focuses on how to drive efficiencies of multicrystalline cells even further upwards. For a standard multicrystalline cell, improvements on the front and back surface will enhance the cell's overall efficiency output. A bundle of measures consistently linked to each other demonstrate how the front and back surface will be modified.

In the medium term, new cell concepts will play an increasing role in driving multicrystalline cell efficiencies beyond 18% in mass production at a very competitive cost basis. Further reduction of shading and a new approach to back contact cells can lead the way.

The multi-crystalline standard cell and its potential

Fig. 2 provides an overview of crystalline silicon solar cell efficiency for both multi- and monocrystalline cells. Standard multicrystalline silicon solar cells have evolved from having conversion efficiencies slightly above 14% around 2002 to today's scenario where efficiencies range typically from 15.0% to 16.6% depending on materials and processes. Over the last few years, the increase in efficiency was clearly visible but not extensive. Modern production techniques give access to improvements that allow for more distinct steps in raising cell efficiency into the region of 18% for multicrystalline material.

The starting point for considering the different improvement steps is a kind of standard cell as produced on most current production lines. While this



Source: Q-Cells internal analysis

Figure 1. Cost reduction analysis illustrating the contribution of technology-driven factors to cost reduction potential.

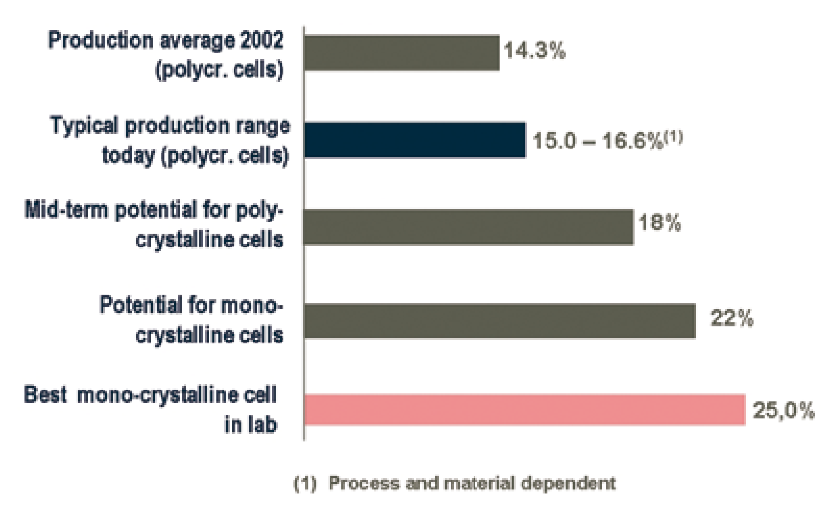


Figure 2. Overview of silicon cell efficiency potential.

cell type is still subject to losses from sources such as optics, recombination and resistance, these losses can be considerably lowered to obtain higher cell efficiency. The following section describes steps that could be taken on the standard type of cell to improve efficiency and also addresses cell concepts that could provide further improvements.

Development steps at the cell front surface

A first set of measures addresses the blue response of the cell. The standard cell suffers recombination in the blue part of the light spectrum that is absorbed near the surface. The main origin is in the doping profile of a typical 55Ω/sq emitter which uses surface doping well above 10^20 cm^{-3} leading to Auger-induced recombination. In order to lower this contribution to recombination, an emitter profile with lower surface doping concentration is desired. Fig. 3 shows internal quantum efficiencies with a standard and a low-doped emitter. The lower contribution of Auger recombination resulting in higher quantum efficiency in the blue spectral range is clearly visible in the left-hand side of the graph.

However, some boundary conditions and additional changes are needed to make a change in the emitter profile a real contribution to cell efficiency:

1. Good contact with the lower doped emitter needs to be achieved with metallization.
2. The distance of metallization fingers should be lowered using higher emitter sheet resistance of the emitter profile in order to limit resistive losses.
3. To avoid higher shading losses each finger needs to be printed in a more narrow fashion.
4. To avoid higher emitter saturation current the front surface needs better passivation since the emitter profile is less efficient in repelling holes from the surface to prevent recombination.

Consequently, concurrent advances in fine line print and surface passivation are required in conjunction with the emitter profile modification. The following section describes possible approaches to achieve these goals, addressing formation of the emitter itself as well as adaptation of metallization and passivation.

> “Higher doping beneath the metallization facilitates the creation of a contact to the emitter, while the area in between the fingers can be set to the profile desired for low recombination losses.”

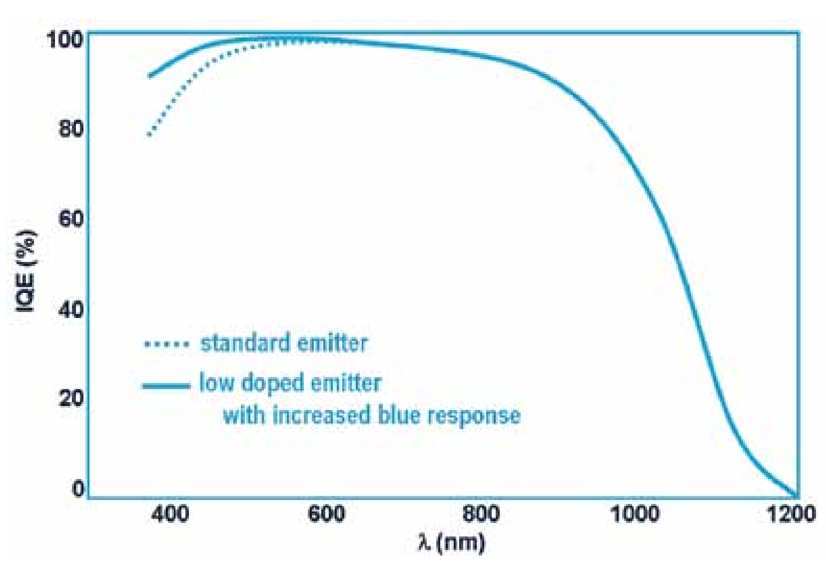


Figure 3. Internal quantum efficiency improvement of a multicrystalline cell in the blue spectral range showing optimized emitter profile.

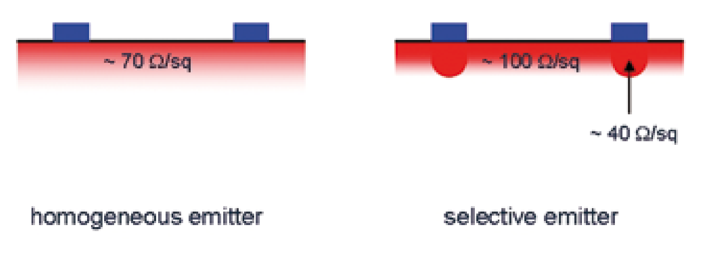
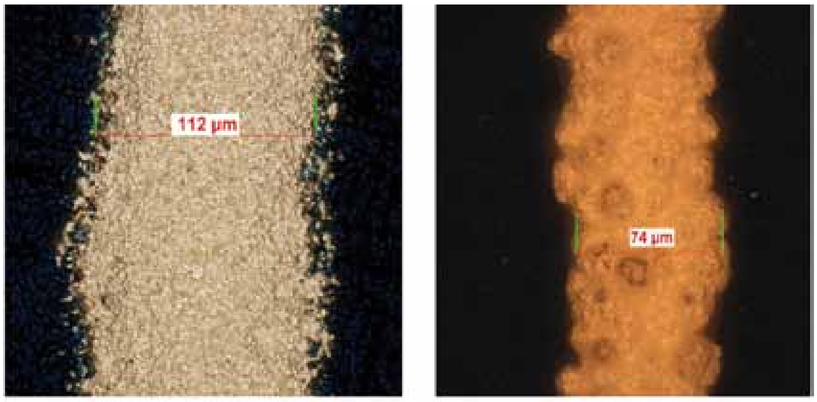


Figure 4. Schematic drawing of homogeneous emitter (left) and selective emitter (right).

Two fundamental approaches exist for creating the emitter profile, as shown in the schematic in Fig. 4. Staying ahead of the technology curve involves maintaining a homogeneous emitter structure (Fig. 4, left). This entails making sure that the silver paste can form good ohmic contact with the emitter despite this process becoming more and more difficult as a result of the lower surface doping concentration. Efforts in paste development are currently under way to achieve this goal. The plating type of metallization is also a help in this case, as the metallization seed layer can be optimized for contact resistance while



	w_f [µm]	V_{oc} [mV]	j_{sc} [mA cm^{-2}]	FF [%]	η [%]
standard	110 – 120	618	34.3	78.5	16.7%
seed & plate	70 – 80	621	34.9	78.3	17.0%

**Figure 5. Print line width reduction by using conventional screen print (left) compared to seed and plate techniques (right).
A contribution to efficiency increase of about 0.3% can be achieved [3].**

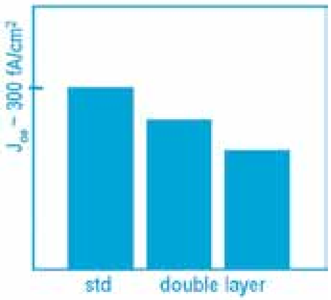


Figure 6. Schematic showing necessary evolution of surface passivation (with emitter optimization) at the cell's front surface.

plating provides the finger conductivity as an independent and decoupled step. Contact formation itself is less critical using the selective emitter approach (Fig. 4, right). In this case, two different doping concentrations are used: low doping in between the metallization fingers and high doping below the fingers. This higher doping beneath the metallization facilitates the creation of a contact to the emitter, while the area in between the fingers can be set to the profile desired for low recombination losses. However, this is usually at the expense of a more complex process, since alignment between the highly doped area and the metallization has to be maintained. As a result, historically this approach has only been seen on a few cells, but progress in equipment leads to constant re-assessment to find the best-suited approach for the industry. More detailed considerations on emitter profiles can be found in [1].

The high emitter resistivity between the fingers in both emitter approaches requires metallization using fine line printing. In order to keep losses caused by series resistance low, the emitter requires a denser grid of fingers and thus the individual finger needs to be printed narrower to avoid an increase of shading losses. This will lead to enhancements in screen printing and

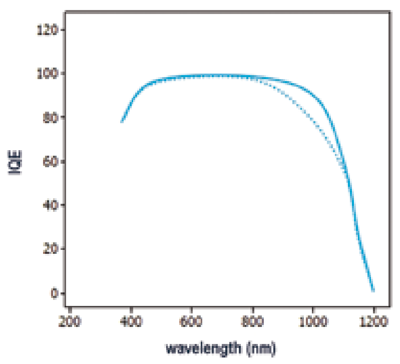


Figure 7. Internal quantum efficiency improvement of a multicrystalline cell in the infrared spectral range bringing optimization of the cell's rear side.

Material	Pros and Cons
SiO_2 – thermal	Proven material from semiconductor industry, high quality interface, limited growth rate.
SiO_2 – PECVD	Passivation properties under evaluation, attractive deposition rate.
SiN_x – CVD	Established in front optics and passivation
a-Si – CVD	Technically proven in PV, limited thermal stability.
Al_2O_3 – ALD	Dielectric with charges, good lab results, industrial feasibility questionable due to low dep rate.

Table 1. Materials candidates for rear-surface passivation of silicon solar cells.

use of metallization techniques allowing for significantly reduced lateral finger dimensions as well as high aspect ratio of the finger metallization to keep finger conductivity on a comparable level. One approach that showed high potential uses a two-step metallization process. A thin seed layer is printed followed by a light-induced silver-plating step [2]. Fig. 5 shows an example of reduced line width resulting from the seed and plate technique [3].

In addition, front-side passivation requires the reduction of the typical emitter saturation current density of 300fA/cm^2 to significantly lower values (Fig. 6). After optimization of the nitride itself, two-layer passivation consisting e.g. of a thin oxide under the more classical nitride layer will be considered as a candidate for achieving this goal. Double-layer dielectrics target the separation of the passivation layer from the antireflection layer. In this way, an independent optimization of the interface properties responsible for passivation and the refractive index of a thicker anti-reflective coating is possible.

In summary, the front surface is modified by an array of measures consistently linked to each other for suppressing recombination without suffering disadvantage from resistive and shading losses.

Development steps at the cell rear side

As with the front side, the rear side of the cell is also a candidate for lowering losses. The two major items addressed on the rear side are rear passivation and rear reflection.

The rear passivation of the standard cell has to date consisted of an Al back-surface field. Depending on the resistivity of the silicon and the BSF quality, this leads to a recombination velocity of around 600cm/s and a reflection of around 67%. Improvement of the passivation requires reduction of the contact area and covering major part of the rear surface by a passivating dielectric layer. For passivation itself this layer can be rather thin; a layer thickness less than 10nm can be sufficient. Combination with optical mirror properties needs higher thicknesses of around 200nm. The alternative to a single layer is a stack system to combine passivation and optical properties from two layers. Optical improvement can result from using an improved mirror as the rear surface, leading to rear reflection values up to 95% using optimized layers. The infrared part of the light spectrum is used more efficiently as it is reflected from the rear side, instead of being absorbed in the Al rear metallization as with a conventional cell (Fig. 7). In addition, this improved light trapping is a necessary step for cell thickness reduction while avoiding large losses in efficiency.

> "Improvement of the passivation requires reduction of the contact area and covering major part of the rear surface by a passivating dielectric layer."

There is a substantial number of candidates for use as rear passivation layers (Table 1), ranging from proven materials to promising candidates on the laboratory scale. Materials comprise thermally-grown silicon dioxide (well established in the semiconductor industry as a gate dielectric); silicon nitride (a standard material in the photovoltaic industry for front passivation); amorphous silicon (as used within the HIT cell concept); and some rather new candidates such as aluminium oxide [4,5]. Some issues arising from these different materials include, for example, limited growth rates or restrictions in process temperature budget. Several candidates are undergoing a more thorough investigation for possible application to the mass production of solar cells.

For the subsequent metallization step, again there are different approaches, such as adapting pastes for use on dielectrics, to more advanced schemes that attempt to replace pastes, which are costly, with PVD deposition of aluminium, for example. In both cases, contact with silicon has to be established by using laser-based techniques like laser-fired contacts (LFC) [6] or alternatively by patterning contact openings into the rear dielectric. LFC is an attractive approach for high throughput in production as it saves patterning effort – always critical from a cost perspective. On the other hand, patterning provides a higher degree of process freedom. It gives access to under-diffusion of contacts, which is another contributor to driving the cell in the direction of record-type PERL [7] cell structures.

With a rear passivation implemented, there will be a readjustment of the doping level of the p-type wafers used. The link that exists between doping level and surface recombination velocity for an aluminium back-surface field due to band bending is no longer valid in the same format with a dielectric interface. The doping level for optimum cell efficiency will shift to higher levels, i.e. lower resistivities of the wafer.

As with the front side, the cell rear benefits from reduced recombination, which allows the cell to attain a new optimum with respect to wafer doping. In addition, the rear mirror increases the optical path especially for infrared light and prepares for cell thickness reduction.

New cell concepts

New cell concepts need to incorporate higher efficiencies. Steps being taken in this direction are further reduction of shading along with exploiting possibilities originating from back-contact cells. Back-contact cells can be interconnected in a rather standard way on module level [8], but also offer new opportunities in connecting cells with less resistive losses [9]. Candidates for such developments are cell types like the MWT (metal wrap through) [10,11] and EWT (emitter wrap through) [12,13] cell.

In the case of the MWT, cell finger metallization is still on the front side while bus bar metallization is moved to the back side of the cell. The connectivity

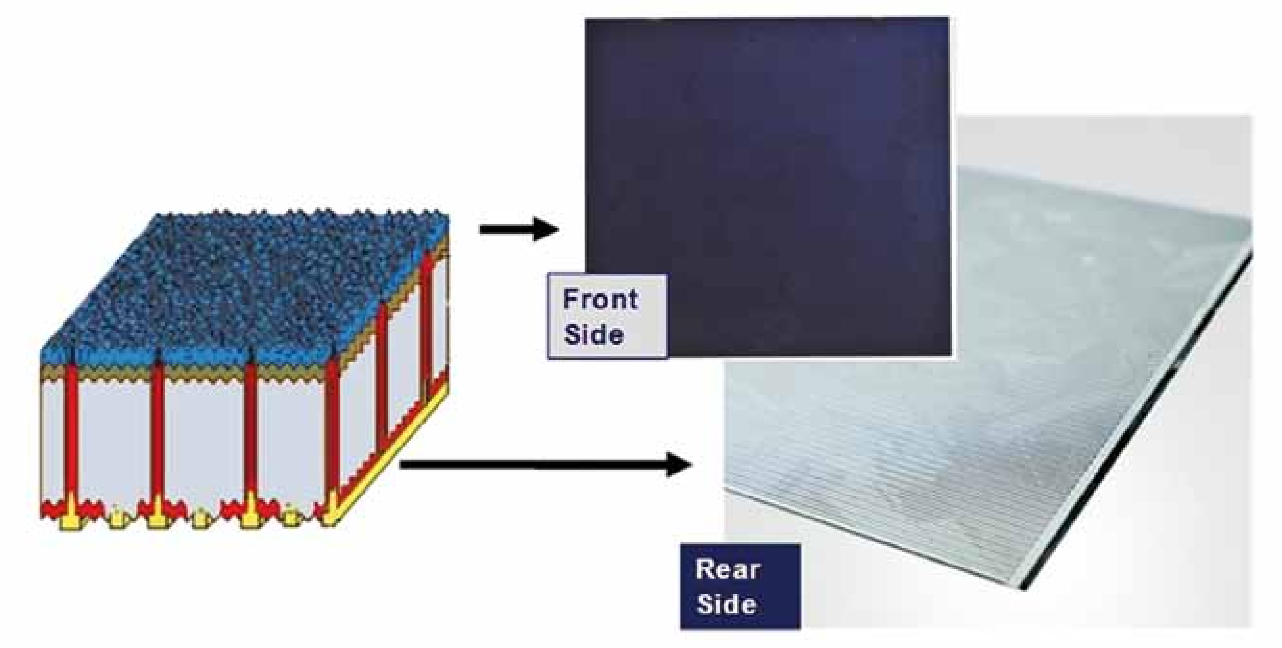


Figure 8. EWT (emitter wrap-through) schematic drawing and photograph of cells as produced within Q-Cells' R&D and research co-operations. The front side does not carry any metallization; emitter contacts to rear-side metal stripes are visible on the rear-side photo.

between front fingers and rear bus bars is via a few (< 1/cm^2) holes drilled with laser techniques and filled with metal paste.

The EWT concept as shown in Fig. 8 consequently moves all metallization to the back side with the emitter diffusion providing contact between the front and the rear side of the cell. Due to the lower conductivity of the emitter as compared to finger metallization, this requires a much higher hole density than does the MWT concept. The emitter extends from the cell front around many (> 20/cm^2) holes to its back-side contact and consequently, a large part of the rear cell surface is emitter. This leads to high efficiency in current collection and large immunity against the minority carrier lifetime variation of the wafer used for cell production. For this reason, the EWT cell type is well suited for application with multicrystalline silicon.

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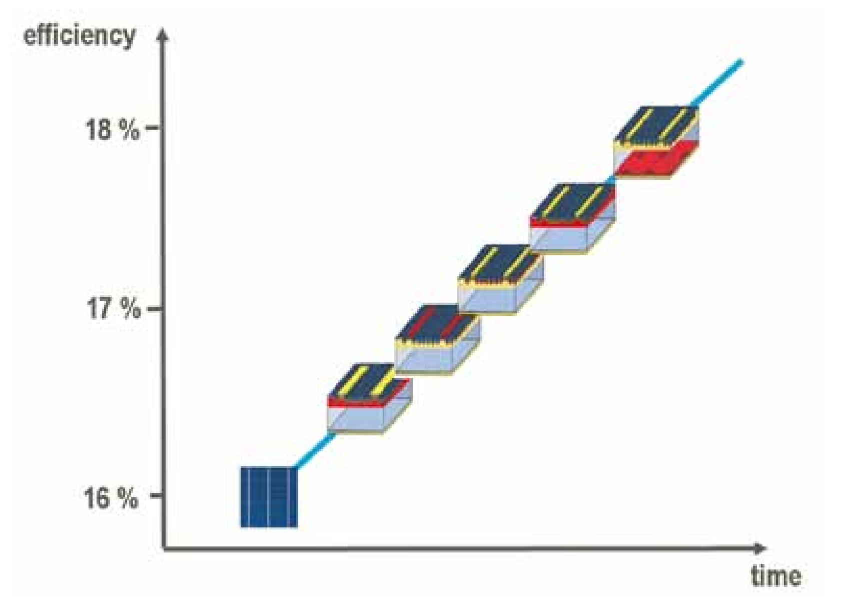

Figure 9. Overview of cell efficiency increase over time (steps not drawn to scale). Starting from the standard cell, changes refer to emitter, metallization and surface passivation before addressing the cell rear side. New concepts must also be taken into consideration towards the end of the process.

The EWT cell concept is still the subject of further investigations. A high conductivity of the diffusion area inside the holes connecting front and rear must be maintained in order to ensure high fill factors necessary for optimum cell efficiency [14].

Summary

We will see development of the classical screen-printed cell that addresses loss reduction in different parts of the cell. Major packages address cell front and rear sides before moving to new concepts. The contributing steps in this process are represented schematically in Fig. 9.

The front side will see a move to emitters, reducing Auger recombination along with the measures that are necessary as a direct consequence, i.e., an improved surface passivation and an adapted metal grid for contacting the emitter with low resistive losses. From a spectral point of view, this results in improved blue response.

The rear side will also move towards improved passivation and implement a mirror affecting mostly the infrared part of the spectrum. This will pave the way for reducing wafer thickness and silicon consumption as a significant contribution to cost reduction. These steps will enable multicrystalline cells to reach efficiency ranges of about 18% for efficient cell classes (Fig. 9). Improvements can be carried to a subsequent cell concept that also eliminates further losses like metallization shading.

With this high contribution of efficiency to the overall cost of energy generation, we expect a significant contribution to lowering the levelized cost of electricity (LCOE) of photovoltaics, and, depending on the regional boundary conditions, reaching the goal of grid parity in the near future.

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Dr. Andreas Kux studied physics at the Technical University of Munich, going on to receive a Ph.D. in 1994 on light emission from porous silicon. He has 13 years' development experience in the semiconductor industry, mostly in the field of non-volatile memories within the R&D departments of Siemens Semiconductor, Infineon and Qimonda. He has worked since 2008 for the Technology Screening and Roadmap of Crystalline Silicon Technology at Q-Cells SE.

Dr. Jörg Müller received his diploma degree in physics from the Ludwig-Maximilians-University in Munich in 2000. He did his Ph.D. research in the field of rear contacted and bifacial sensitive solar cells at ISFH in Hamlin and obtained his Ph.D degree from Hannover University in 2005. He joined the technology devision at Q-Cells in 2004. Since 2007 he is leading the crystalline silicon cell and module development at Q-Cells SE.

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