

Challenges for single-side chemical processing

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ABSTRACT

Wet chemical process equipment is widely used in industrial solar cell production, and inline etching systems in particular have attracted more and more attention since their introduction 10 years ago. The horizontal wafer transport within these systems has made it possible to think about single-side wafer treatments even for wet chemical process applications. Since its market introduction in 2004, the chemical edge isolation process based on the single-side removal of the parasitic emitter at the rear side of the solar cells has gained an increasing share of the market in comparison to competing technologies that use laser techniques. However, stabilization and control of such a process under mass production conditions remains challenging. The introduction of new high-efficiency cell concepts involving passivated rear sides will increase the importance of single-side wafer treatments, as the final solar cell performance is significantly affected not only by the complete removal of the parasitic emitter but also by an ideally polished surface on the rear side of the wafer.

Introduction

Single-side wet chemical processing techniques are gaining importance in industrial solar cell manufacturing as they increasingly replace the once widely used laser technologies, especially for edge isolation [1,2]. Performed directly after emitter diffusion, the wet chemical process completely or partly removes the parasitic emitter from the wafer's rear side and edges. For standard screen-printed solar cells, this means that the aluminium-alloyed rear no longer has to overcome the phosphorus diffusion on the rear of the solar cell in order to create an alloyed aluminium/silicon back-surface field (BSF) layer, which is the requirement for plasma or laser-edge junction isolation. A higher quality BSF can therefore be obtained, leading to higher efficiencies. By removing the emitter from the rear of the cell, chemical edge isolation is compatible with the development of future cell technologies that do not utilize screen-printed contacts and require single-sided diffusions. Inline etching systems with acidic etch chemistry based on HF/HNO₃ are typically used, resulting in a surface that is still rough [3]. An industrially applicable etching process for single-side emitter removal must therefore fulfil several requirements:

- Etch back of the emitter layer at the cell's rear side is homogeneous
- The process is completely single sided
- Process conditions are stable in order to create a robust process

Because of the use of thinner wafers and the goal of achieving higher conversion efficiencies, future industrial solar cell concepts are mainly based on the use of rear passivation concepts and local rear contacts (PERC) [4–6]. Besides

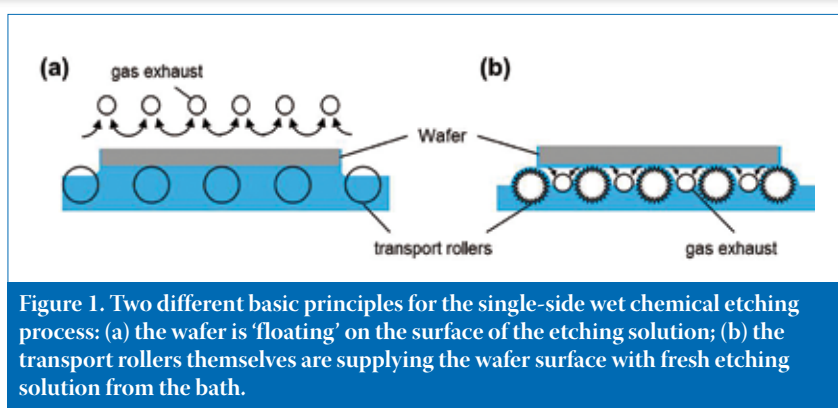


Figure 1. Two different basic principles for the single-side wet chemical etching process: (a) the wafer is 'floating' on the surface of the etching solution; (b) the transport rollers themselves are supplying the wafer surface with fresh etching solution from the bath.

the different passivation and metallization techniques used, single-side removal of the parasitic emitter layer, as well as surface cleaning issues at the cell's rear, turns out to be a key technology step for an industrial realization. Depending on the actual process scheme, dry or wet chemical etching and conditioning approaches might be preferable. In high-efficiency laboratory processes, the solar cell's rear is usually polished to reach optimum passivation quality; the polishing itself, however, is often achieved by additional masking of the non-etched wafer side. Transferring such a polishing process into mass production is a very challenging proposition, as will be discussed in the following sections.

This paper reviews different possibilities for the technical realization of single-side wet chemical etching processes, as well as summarizing the challenges for implementation and quality assurance of wet chemical edge isolation and chemical polishing processes.

Technical realization of single-side processes

On the equipment market today, it is mainly horizontal processing solutions

within industrially suitable inline etching systems that are available for single-side wet chemical etching applications. As etching solutions, diluted acidic chemicals with the main components hydrogen fluoride (HF) and nitric acid are commonly used. To suppress the strong etching reaction, as well controlling the viscosity of the solution, additives such as sulphuric or acetic acid might be added. As the etching in those acidic mixtures is strongly exothermic, constant cooling of the overall etching bath has to be ensured in order to control the process and to minimize the resulting reaction gases. To implement the etching sequence within these inline systems and to maintain the single-sidedness, two basic etching principles can be distinguished (see Fig. 1):

- (a) The silicon wafer is transported on the surface of an etching bath. The liquid surface of the etching bath is regulated in such a way that a small gap of a few millimetres is formed between the wafer and the liquid surface. With the correct distance attained, the wafer itself enables the adhesion of the liquid to the wafer. The resulting meniscus of the solution towards the wafer surface should not

collapse during the etching process; on the other hand, dipping of the wafer into the solution has to be avoided. In order to avoid a wrap-around of reaction gases (HF, nitrous oxides), gas exhaust lines are typically installed above the wafer surface.

- (b) The wafer is transported via 'wetted' transport rollers. In this case a homogeneous liquid film on the rollers has to be ensured in order to enable sufficient fresh media supply to the wafer's surface. The amount of etching solution that can be brought to the wafer surface by this method typically depends on, for example, the transport velocity, the viscosity of the etching solution and the overall liquid surface level in which the rollers are immersed. The resulting reaction gases can be drawn off between the rollers, directly at the wafer surface.

Most existing etching systems on the market rely on one of the above-mentioned etching principles, and often the available systems can only be distinguished by the types of roller material, different transport mechanisms or gas exhaust set-ups.

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Chemical edge isolation

A major challenge of the chemical edge isolation process is ensuring that the front emitter remains dry throughout the process while the rear is etched. This requirement is even more challenging due to the fact that, typically, the chemical etch is done directly after emitter diffusion, with the phosphorus silicate glass layer still present on all wafer surfaces. That results in an overall hydrophilic surface, which, on the one hand, alleviates the homogeneous distribution of the etching solution on the rear side, but, on the other hand, also promotes a wrap-around of the etching solution towards the front-emitter side of the wafer. The latter effect is even more critical because the emitter has to be properly removed not only on the rear side but also on the wafer edges; this is illustrated in Fig. 2. In the case when the emitter is not sufficiently removed from the wafer edge, potential edge disturbances, already caused during wafering, are not separated from the front-

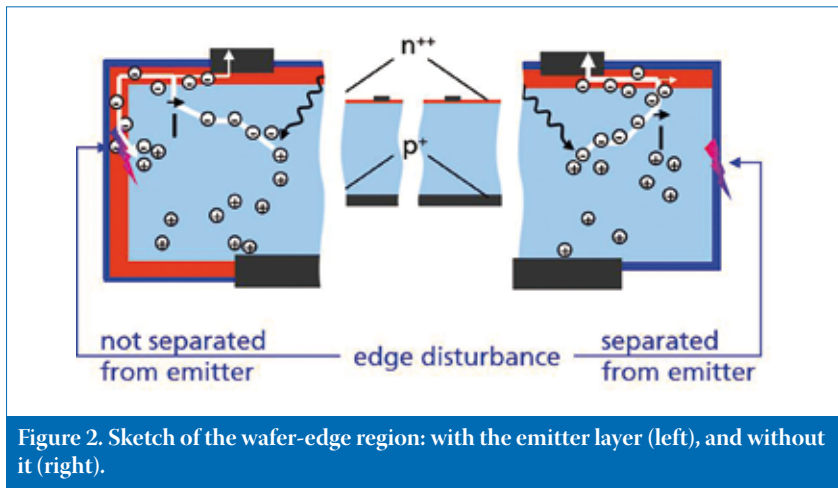


Figure 2. Sketch of the wafer-edge region: with the emitter layer (left), and without it (right).

side emitter. Minority charge carriers which are generated near the wafer edge are therefore more likely to recombine at these recombination centres than to be collected from the front emitter. Total removal of the emitter layer from the wafer edge, together with an effective SiN_x anti-reflection and passivation layer, suppresses such an effect.

For the implementation of the chemical edge isolation process, a number of parameters have to be optimized in order to obtain a robust production process. Many process settings are closely related to each other: for example, in general an etch depth of around 0.6µm should be sufficient for the removal of a standard industrial emitter layer. However, that would assume a totally homogeneous etch rate throughout the whole wafer surface. As this is not typically achieved, the etch depth has to be slightly increased to a value of around 1µm. Increasing the etch depth can usually be realized by extending the etching time. The easiest method of controlling the etch depth, however, is changing the transport speed, but this does not work for single-side etching processes. Owing to the etching mechanisms discussed earlier, the transport speed might already influence the formation of the liquid meniscus towards the wafer

surface in the case of principle (a), or affect the amount of etching solution transported via the rollers in the case of principle (b). Moreover, the overall transport speed typically represents a fixed parameter in an industrial production line; the variation of the etch depth, therefore, has to be adjusted either by the temperature or by the composition of the etching solution itself.

Besides the challenges of establishing and controlling the etching process itself, quality assessment as process control also tends to be critical. To decide whether the process has been carried out successfully, the corresponding sheet-resistance distributions at the wafer's front emitter side as well as at the rear side have to be controlled. As mentioned earlier, for chemical edge isolation, it is important to characterize in particular the wafer-edge regions. However, to characterize the sheet resistance in the near-edge region (e.g. using the well-known 4-point probe measurement technique), the edge itself has a highly detrimental effect on the results. Fig. 3 shows 4-point probe track measurements of the front side of a wafer after chemical edge isolation. The measurements were carried out on all four sides of the wafer by measuring a track of 30mm towards the wafer edge. In all cases,

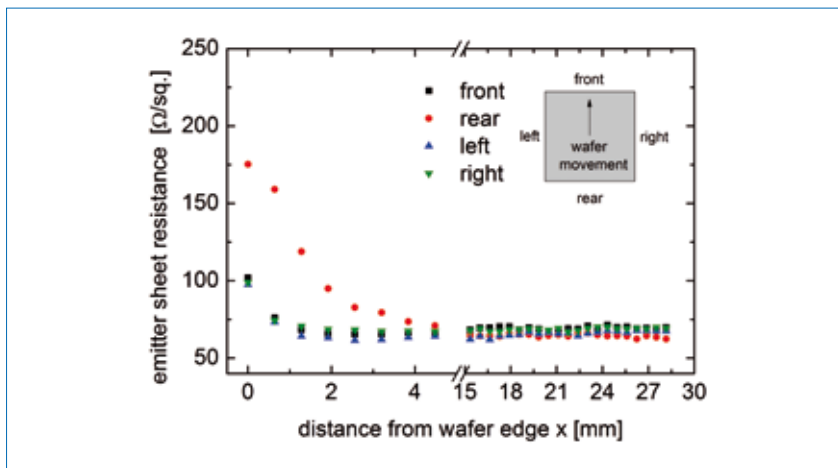


Figure 3. 4-point probe line scan measurements, taken on the four different sides of the wafer, of the front emitter after chemical edge isolation.

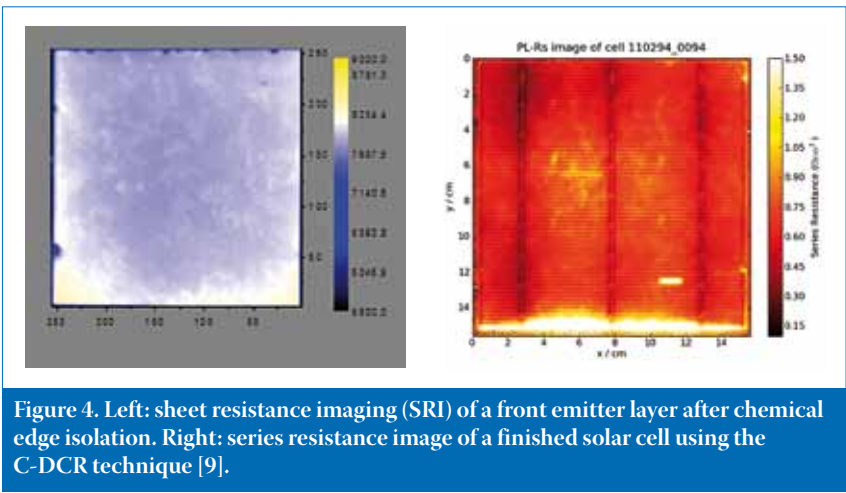


Figure 4. Left: sheet resistance imaging (SRI) of a front emitter layer after chemical edge isolation. Right: series resistance image of a finished solar cell using the C-DCR technique [9].

an increase in emitter sheet resistance was observed when approaching the edge.

In order to understand such an increase in sheet resistance, the basic principles of a 4-point probe measurement technique have to be kept in mind. This technique is typically used for homogeneous layers, as the assumed geometrical current distribution underneath the contacts only holds true in that particular case. However, as one approaches a non-conducting wafer-edge region, this assumption is no longer valid. The current distribution is confined by the edge itself, and the measured voltage (and therefore the resulting resistance) is significantly increased because of the smaller available area. In the case of a conducting wafer edge (i.e. where an emitter layer still exists on the wafer edge), current might also flow around the edge, resulting in an actual lower voltage and therefore in a lower sheet resistance. It is possible to show that, up to a distance of about 3mm from the wafer edge, sheet resistance values can be determined with sufficient measurement accuracy.

For the measurement example in Fig. 3, the observed increase of the emitter sheet resistance on all four wafer sides

therefore demonstrates the removal of the emitter from the wafer edge (i.e. the case of a non-conducting wafer edge). On the other hand, there are differences in the increases in sheet resistance between the wafer sides. Whereas the front, as well as the left and right sides of the wafer's front emitter (in the direction of the wafer movement through the etching bath), seems to be undisturbed in terms of resistance, there is a significant increase in sheet resistance observable at the rear side of the wafer. Such an increase is often observed and can be attributed either to an actual etching media wrap-around (in the case of a textured front side, often capillary forces alleviate such a wrap-around) or to reaction gases that are concentrated especially at the wafer's rear side. In both cases, the phosphorus silicate glass layer still present on the front surface is no longer able to sufficiently protect the emitter layer. In order to analyze these effects further, spatially resolved measurement techniques are necessary to localize the affected wafer areas.

Fig. 4 presents two different possible inline-capable measurement techniques.

The first method (Fig. 4, left) is the so-called sheet resistance imaging (SRI) [7], which can be carried out directly after the etching process. This method gives an initial overview of the homogeneity of the resulting emitter sheet resistance; unfortunately, no calibration is as yet available between the measurement signal and the real sheet resistance, so only quantitative information can be extracted. The measurement clearly indicates areas of higher emitter sheet-resistance (darker blue regions) and can therefore help to localize areas of stronger etch attack during chemical edge isolation.

For a final cell analysis, luminescence images of silicon solar cells are useful, since they contain information about local recombination properties and local series resistance. The increase in series resistance due to the detrimental effect of the etch attack on the front-side emitter can be visualized and qualitatively evaluated (Fig. 4, right) using a fast method based on photoluminescence imaging for a spatially resolved coupled determination of the dark saturation current and series resistance (C-DCR) [8].

In principle, all the measurement techniques presented could also be realized as inline measurements; however, only sheet resistance measurements are widely accepted as a quality assurance tool in standard industrial production lines. Imaging methods such as SRI or luminescence methods may provide a much more detailed data set of the process outcome, but further research in this area is needed to extract more quantitative information.

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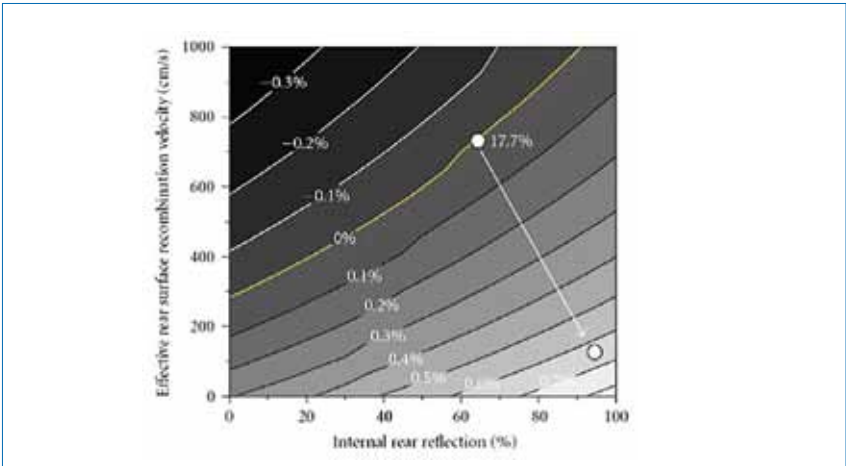


Figure 5. Changes in efficiency due to variation of the surface recombination at the rear surface S_{rear} and the internal reflection R_{back} . The point marked on the 0% isoline (yellow) represents a 220 μm -thick industrial solar cell with 60 Ω/sq emitter and Al-BSF on 1 Ωcm monocrystalline silicon. The second point relates to a rear-passivated and locally contacted (PERC) solar cell with the same front side.

Rear-side polishing

For high-efficiency, all-side-passivated solar cell concepts, not only is the removal of the parasitic emitter layer at the rear side necessary, but also the rear surface of the wafer must be polished in order to optimize the electrical quality of the rear passivation layer and to facilitate effective light trapping within the solar cell bulk [10]. Such an approach is becoming even more important as wafer thicknesses decrease, since the passivation quality needs to be improved because of the increased surface-to-volume ratio. Additionally, the path length of the light inside the wafer is shortened for thinner

Credit: Glunz [11].

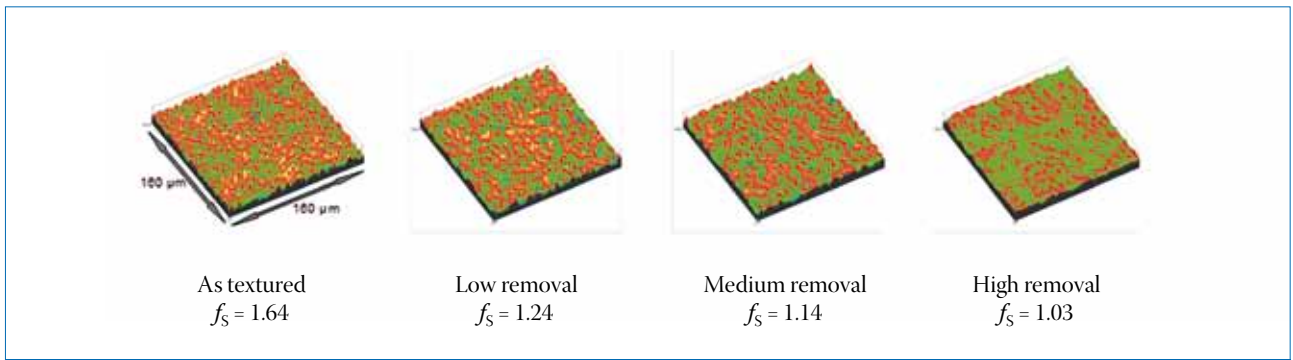


Figure 6. Resulting surface topography and surface enlargement factor f_s measured by confocal microscopy after different polishing processes with increasing amount of etch (from left to right), starting from a surface that was originally alkaline textured [13].

wafers, so out-coupling of light at the rear interface needs to be minimized. The influence of the corresponding physical parameters of the solar cell – the surface recombination velocity S_{rear} (electrical quality of the passivated surface) and the internal reflection R_{back} (optical quality of the rear interface) to the conversion efficiency – is shown in Fig. 5 [11].

The implementation of a polishing process for the wafer's rear side would ideally be combined with the single-side chemical edge isolation step to remove the parasitic emitter on the rear surface. Etching mixtures for polishing purposes, although also mostly acidic, usually have a much higher concentration of HF and HNO_3 than typical mixtures used for chemical edge isolation. The challenges concerning etch media and reaction gas wrap-around effects that were mentioned earlier are therefore even more distinctive for the polishing process. For that reason, at the moment the polishing can only be implemented in a solar cell process sequence before emitter diffusion, directly after texturing [12]. But, as the parasitic emitter removal at the rear side would still be necessary for the production of a rear-passivated and locally contacted (PERC) solar cell, two single-side process steps are currently still required.

The polishing, however, entails different requirements for the etching process when the original texture (either alkaline or acidic for a typical two-sided texturing process) needs to be flattened. In order to obtain a truly polished surface from an originally alkaline-textured surface, it is necessary to etch off almost $20\mu\text{m}$ of silicon (see Fig. 6). The decrease in the surface enlargement factor f_s with increasing etch depth is clearly demonstrated in Fig. 6 for surfaces that have been pre-textured differently. Due to the variation in morphology of acidic- and alkaline-textured surfaces, the required amount of silicon to be removed differs: $3\text{--}5\mu\text{m}$ silicon removal should be sufficient to polish the rear of an acidic-textured surface; in the case of alkaline-textured surfaces, $10\mu\text{m}$ or more will be necessary in order to achieve a target of around 10% surface area enlargement (medium removal in Fig. 6).

A major drawback of implementing such a process step, especially with monocrystalline silicon wafers, is the fact that such an etch depth results in a significant thinning of the overall wafer. Nevertheless, $I\text{-}V$ data of PERC type solar cells, when a rear polish process is applied with different silicon removal rates, demonstrate the efficiency

improvement potential of such a process (see Table 1). An overall efficiency gain of more than 2% absolute could be realized by implementing the rear polishing process. The large increases in V_{oc} and J_{sc} demonstrate the improved electrical (low S_{rear}) and optical (high R_{back}) performance of the solar cell's rear side, independent of the choice of passivation layer (the same results were obtained with either thermal oxidation or PECVD AlO_x passivation).

These results provide initial evidence that a polished rear surface yields a high passivation quality for PERC-type solar cells. Further progress in process optimization (particularly by technologically solving the detrimental wrap-around effects) might also allow a future combination of rear polishing and chemical edge isolation within one process step.

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Conclusion

Single-side wet chemical etching processes are increasingly being utilized in industrial manufacturing of crystalline silicon solar cells, mainly for chemical edge isolation. Independent of the individual technological realization, keeping the single-sidedness of the process remains the major challenge of this approach. Liquid media and/or reaction gas wrap-around effects have a strong influence on the performance of the front-side emitter layer and have to be strictly avoided. Common measurement techniques need to be adapted in order to correctly interpret the measurement results. The challenge becomes even greater when the single-side etching process must not only remove the parasitic emitter layer at the rear surface, but also provide an effective polishing of the surface. These processes, mandatory for many rear-passivated and locally

Si removal (no. of cells)	Passivation	f_s	V_{oc} [mV]	J_{sc} [mA/cm ²]	FF [%]	η [%]
As textured (6)	SiO_2	1.64	618	36.9	75.4	17.2*
Low removal (5)	SiO_2	1.24	646	38.5	74.9	18.6*
Medium removal (5)	SiO_2	1.14	646	38.7	76.2	19.0*
Medium removal (7)	AlO_x	1.14	644	38.7	76.0	19.0*
High removal (6)	SiO_2	1.03	649	39.0	76.7	19.4*
Best cell, stabilized	SiO_2	1.03	646	38.6	77.2	19.3**

*Measured on an industrial cell tester after processing.
**Confirmed by Fraunhofer Callab.

Table 1. Surface enlargement factor f_s extracted from confocal microscopy measurements, and the median values of the $I\text{-}V$ parameters of the best firing group as a function of the Si removal. Total cell area is $\sim 239\text{cm}^2$. The best cell after degradation for 24 hours under illumination of approximately 0.6 suns is indicated. (The highest efficiencies achieved are highlighted in bold.)

contacted high-efficiency cell concepts, represent a key factor in improving the electrical and optical qualities of the rear side of a solar cell.

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